Chapter 1

Introduction

1.1 Motivation

1.2 Objective

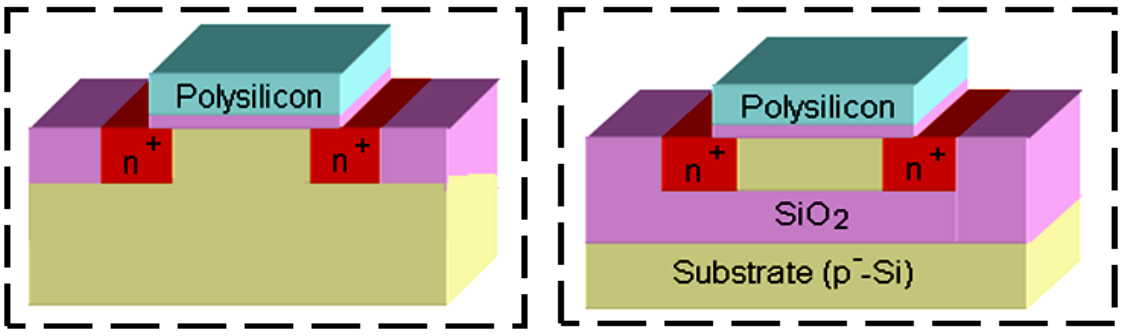
1.3 Literature Review

1.4 Thesis Organization

1.1 MOTIVATION

With the emergence of mobile computing and communication, low power device design and implementation have got a significant role to play in VLSI circuit design. Continuous device performance improvement is possible only through a combination of device scaling, new device structures and material property improvement to its fundamental limits. The down-scaling of MOSFETs has been the most important and effective way for achieving device performance improvement for VLSI circuits. However, the performance requirement in these advanced technologies couldn't be achieved with conventional bulk CMOS process leading to an alternative, Silicon-on-Insulator (SOI) technology. The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronic devices, colloquially referred to as extending Moore's Law. Reported benefits of SOI technology relative to conventional silicon (bulk CMOS) processing includes:

- Lower parasitic capacitance due to isolation from the bulk silicon, which improves power consumption at matched performance.
- Resistance to latch up due to complete isolation of the n- and p-well structures.



(a) (b)

Figure 1: (a) Bulk MOSFET, (b) SOI MOSFET

Figure 1 shows the structural differences between conventional bulk MOSFETs and SOI MOSFETs. From a manufacturing perspective, SOI substrates are compatible with most conventional fabrication processes. In general, an SOI-based process may be

implemented without special equipment or significant retooling of an existing factory. Among challenges unique to SOI are novel metrology requirements to account for the buried oxide layer and concerns about differential stress in the topmost silicon layer. The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10–15% increase to total manufacturing costs.

1.2 OBJECTIVE

SOI MOSFETs exhibit interesting properties that make them particularly attractive for applications such as radiation hard circuits, high temperature electronics etc. The aim of this work is to develop a circuit simulation model of SOI MOSFET and study the different characteristics of SOI MOSFET to compare the effects of varying device parameters using the simple models presented in this work. The result and analysis will be implemented by using Silvaco Atlas TCAD simulation software.

1.3 LITERATURE REVIEW

1.3 Literature Review

Silicon-on-insulator (SOI) technology has been of interest since the 1970's due to advantages in device isolation and speed, etc., over regular MOSFET's. In a modern day IC there may be millions of transistors on a small piece of silicon. Naturally the fabrication and design of these IC’s cannot be done without computer aids. Both the fabrication and design of these IC’s require Electronic Design Automation tools (EDA). There is a need for highly precise software tools to analyze and simulate the design and fabrication of integrated circuits. A lot of researches have been done and still going on these issues. As a result we have got highly useful tools for design and fabrication of IC’s.

CMOS technology has been the driving technology for whole microelectronics industry for last many years. In the early 80's many research have been started on various features of SOI MOSFETs. In the beginning of research on SOI devices one of the papers entitled "MOSFETs Fabricated in {100} single crystal silicon-on-oxide obtained by a laser-induced lateral seeding technique" was published analyzing the growth of 1 μm thick layer of SiO2 on selected areas of a {100} silicon wafer such that the resulting oxide surface was level with the original silicon surface and the single crystal growth of the wafer was extended into the oxide region by as much as 80 μm, providing a sufficiently large single crystal SOI region for device fabrication.**[1]** A novel SOI CMOS design has been explored in the paper "Novel SOI CMOS design using ultra thin near intrinsic substrate".**[2]** It utilizes an ultra thin near intrinsic substrate wherein no channel doping is introduced during processing. In another paper among the early research on SOI MOSFETs, the charge coupling between the front and back gates of thin-film silicon-on-insulator MOSFET's is analyzed and expressions for the threshold voltage under all possible steady-state conditions are derived**.[3]** Some research have been done Describing the fabrication process and the electrical characteristics of SOI MOSFET with gate oxide and a gate electrode.**[4]** During the early research works on the development of SOI MOSFETs, major categories of analysis were related to the effect of grain boundaries, propagation delay, kink characteristics using two-carrier modeling, transconductance of SOI MOSFETs, modeling of MOSFET on SOI structure using various techniques like Monte Carlo Simulation Technique, two-step oxidation technique etc. After that, advanced research work was followed based on modeling of subthreshold swing and threshold voltage of ultra-thin-film SOI MOSFETs, SOI gate-all-around MOS device, parasitic BJT design consideration in SOI MOSFETs, analysis of Substrate floating effects of p-channel SOI MOSFETs etc.**[5]** Analysis of p/sup +/ poly Si double-gate thin-film SOI MOSFETs Dynamic effects in SOI MOSFET's involves planar p/sup +/ poly Si double-gate thin-film SOI (silicon-on-insulator) nMOSFETs is fabricated using wafer bonding and the fabricated devices had shown a transconductance exceeding twice that of the single-gate SOI-MOSFET.**[6]** Analysis of the dynamic effects in SOI MOSFETs, analysis of the drain breakdown mechanism in ultra-thin-film SOI

MOSFETs, Suppression of parasitic bipolar effects in thin-film SOI transistors are significant research works done on this issue.**[7][8][9]** Research have been done on the effects of volume inversion in thin-film short-channel SOI MOSFETs and the efficacy of dual-gate operation in enhancing their device performance using two-dimensional device simulations and one-dimensional analytical computations, Self-heating effects in SOI MOSFET's operated at low temperature, TCAD-assisted analysis of back-channel leakage in irradiated mesa SOI nMOSFETs, **[10] [11][12]** etc.

In recent years more advanced development of SOI technology is invented through research and hence new scope of analysis is being opened. The recent and advanced work on SOI MOSFETs includes 3-D TCAD modeling of SOI MOSFET, analysis of short-channel effect in ultrathin SOI MOSFETs etc. **[13]** Recently a paper titled "Detailed characterization of SOI n-FinFETs at very low temperature" was about DC and low frequency noise measurements on strained and unstrained n-channel FinFET transistors processed on silicon on insulator (SOI) substrates were performed at 10 K in order to evaluate the device performances and study the low frequency noise mechanisms.**[14]** The paper Evolution of photodetectors by SOI material was published where new features of photodetectors attained by SOI was introduced.**[15]** Radiation response of state-of-the-art SOI CMOS technologies, low-temperature minority-carrier injection in the n-channel dynamic threshold MOSFET with various silicon-on-insulator (SOI) layer thicknesses etc are among the recent analysis and research on this issues.

1.4 THESIS ORGANIZATION

The Paper is divided into four parts and its outline is given below:

Chapter 1: Introduction and fundamental concept of SOI devices, motivation for present research and literature review.

Chapter 2: Basic theory of semiconductor and MOSFETs, detailed description of SOI MOSFETs, related equations and a brief description of SILVACO TCAD Simulation software.

Chapter 3: The result that is extracted from the analysis and study.

Chapter 4: Scope for future work and conclusion with references.

Chapter 2

Theoretical Overview and Simulation Tools

2.1 MOSFET Fundamentals

2.2 SOI Basics

2.3 Schrödinger and Poisson Equations

2.4 Description of the Simulation Tool

2.5 ATLAS Framework

2.6 ATLAS Coding Process

2.1 MOSFET FUNDAMENTALS

2.1.1 Semiconductor Basics

The materials whose electrical properties lie between those of conductors and Insulators are known as semiconductors.[16] The examples of such materials are germanium (Ge), Silicon (Si), gallium arsenide (Ga As), Cadium Sulfide (Cds), lead telluride etc. At. absolute zero temperature (ie at 0K) there are no electrons in the conduction band of semiconductors and the valence band is completely filled. Thus the semiconductor behave like an insulator at 0K. If the temperature is increased the width of the energy gap reduces, consequently, some of the electrons jump into condition band and semiconductors show some conductivity. It is thus obvious, that the conductivity of semiconductors increases with the increases in temperture.

Commonly used semiconductors

The most frequency used materials are germanium (Ge), and Silicon (Si).[17] It is because then energy required to break their co-valent bonds is every small;being 0.7 eV for Ge and 1.1 eV for Silicon. Germanium is an each element. It is recovered from the ash pd certain coals or from the flue dust of Zinc smelters. The atomic numbers of germanium is 32. It has four valence electrons (ie) it is tetravalent element. Figure shows how the various germanium atoms are held through co-valent bonds. As the atoms are arranged in an orderly pattern, therfore germanium has crystalline structure.

The most common crystal structure among frequently used semiconductors is the diamond lattice. Each atom in the diamond lattice has a covalent bond with four adjacent atoms, which together form a tetrahedron. This lattice can also be formed from two face-centered-cubic lattices, which are displaced along the body diagonal of the larger cube in Figure 2.1 by one quarter of that body diagonal**.[18]** The diamond lattice therefore is a face-centered-cubic lattice with a basis containing two identical atoms.

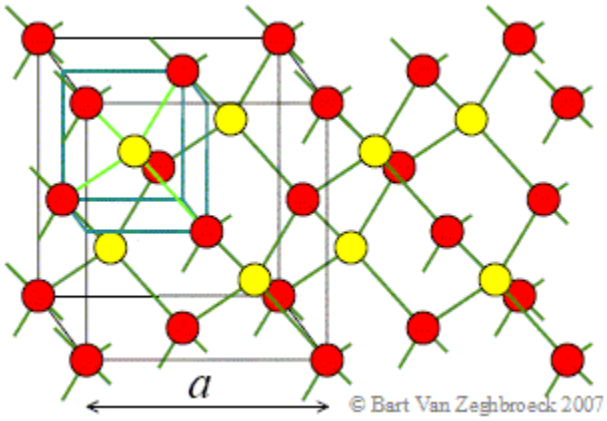


Figure2-1:The zinc-blende crystal structure of GaAs and InP

Materials can be categorized according to their electrical properties as conductors, insulators or semiconductors. The conductivity, σ is a key parameter in identifying the type of material.

In conductor, conduction band is partially filled with electrons and has very high conductivity. In insulator, bandgap between valence band and conduction band is large and conductivity is extremely low. But in semiconductor, valence band is completely filled with electrons at low temperature and conduction band is empty and its conductivity falls between conductor and insulator. In this thesis the main attention is given on the characteristics of semiconductor.

Two general classifications of semiconductors are the elemental semiconductor materials, found in group IV of the periodic table, and the compound semiconductor materials, most of which are formed from special combinations of group III and group V elements and also from the combinations of group II and group VI.

The elemental materials, those that are composed of single species of atoms, are silicon and germanium. Silicon is by far the most common semiconductor used in integrated circuits and will be emphasized to a great extent.

2.1.2 Silicon Structure

Silicon is an element in most of the common rocks. Actually, sand is silicon dioxide. The silicon compounds are chemically reduced to silicon which is 100% pure for use as a semiconductors[19]. Silicon atom has four valence elements (ie) it is a tetravalent element. Silicon is a group IVA element. Silicon is a chemical element with the symbol Si and atomic number 14, atomic mass 28.09 amu, number of protons/electrons 14 and number of neutrons 15. Silicon is a group IVA element. Silicon is a chemical element with the symbol Si and atomic number 14, atomic mass 28.09 amu, number of protons/electrons 14 and number of neutrons 15. Like germanium, Silicon atoms are also arranged in an orderly manner. Therfore , silicon has crystalline structure.

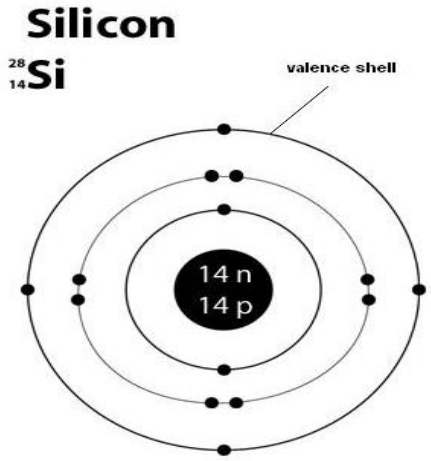


Fig 2-2 : Silicon atom

Consider a pure germanium crystal. Germanium[20] atom has four valency electron. When a small amount of pentavalent impurity is added germanium crystal, the four valence electrons wil form co-valent bonds four valence electrons of germanium atom.

The fifth electron of pentavalent impurity finds no place for co-valent bond and is thus free electron. Thus each arsenic atom introduced on free electron. Thus a samll amount of arsenic provides enough atoms to suply millions of free electrons.Thus many new free electrons are produced by the addition of pentavalent impurity. Because of thermal energy a few hole-electron pairs are created. But the number of free electrons exceeds the number of holes.

The properties of Silicon elements[21] are shown in table 2.1

Table 2.1: Properties of Si at T=300K

Property	**Silicon**
Atoms(/cm3)	5e22
Atomic Weight	28.09
Crystal Structure	Diamond
Density(g/cm3)	2.33
Lattice Constant(cm)	5.43
Melting Point(deg C)	1415
Dielectric Constant	11.7
Bandgap Energy(eV)	1.12
Electron Affinity(volts)	4.01
Nc(/cm3)	2.8e19
Nv(/cm3)	1.04e19
Intrinsic Concentration(/cm3)	1.5e10
Electron Mobility(cm2/V-s)	1350
Hole Mobility(cm2/V-s)	480
Electron Effective Mass	1.08
Hole Effective Mass	0.56

2.1.3 Properties of MOSFET

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a transistor which is mainly used for amplifying or switching electronic signals[22]. The MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals. The body (or substrate) of the MOSFET is connected to the source terminal, which makes it a three-terminal device like other field-effect transistors. There are two types of MOSFET's: enhancement type and depletion type. For each type, there are again two types: N-type and P-type. The structure of each type of mosfet is shown in figure 2.3.

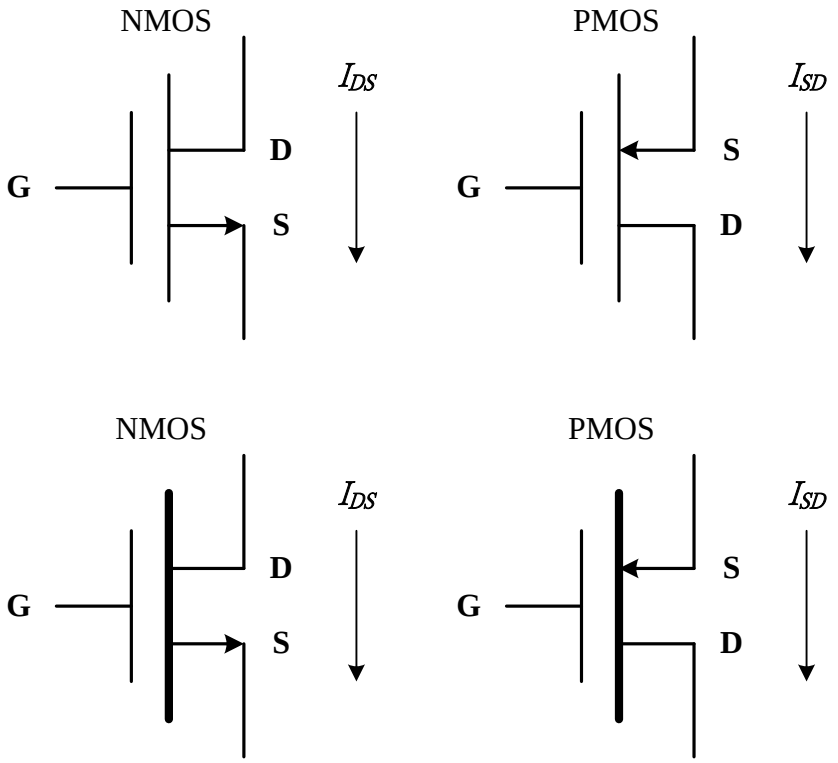


Fig 2-3. Current directions in different type of transistors.

MOSFET Silicon Structure:

MOSFETs are used both as discrete devices and as active elements in digital and analog monolithic integrated circuits (ICs)[23]. In recent years, the device feature size of such circuits has been scaled down into the deep submicrometer range. Presently, the 0.13-μm technology node for complementary MOSFET (CMOS) is used for very large scale ICs (VLSIs) and, within a few years, sub-0.1-μm technology will be available, with a commensurate increase in speed and in integration scale. Hundreds of millions of transistors on a single chip are used in microprocessors and in memory ICs today. CMOS technology combines both n-channel and p-channel MOSFETs to provide very low power consumption along with high speed. New silicon-on-insulator (SOI) technology may help achieve three-dimensional integration, that is, packing of devices into many layers, with a dramatic increase in integration density. New improved device structures and the combination of bipolar and field effect technologies (BiCMOS) may lead to further advances, yet unforeseen. One of the rapidly growing areas of CMOS is in analog circuits, spanning a variety of applications from audio circuits operating at the kilohertz (kHz) range to modern wireless applications operating at gigahertz (GHz) frequencies.

As shown in Fig. there are three important parameters of an NMOS transistor, namely V_{GS}, V_{DS} and I_{DS}. It should be reminded here that in an NMOS transistor, the current flows from drain to source and there is no gate current.

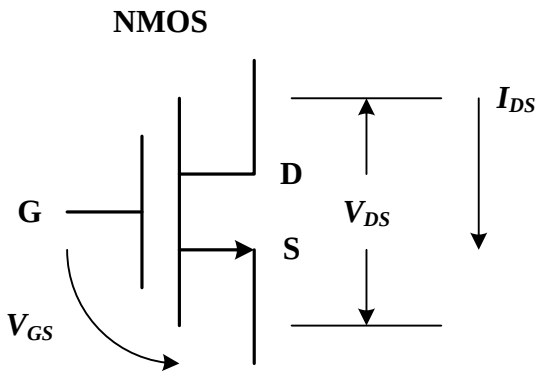


Fig 2-4. Voltage and current in a NMOS transistor.

Suppose we have a fixed V_{GS}, the I_{DS} vs V_{DS} curve is as shown in Fig.2.4.

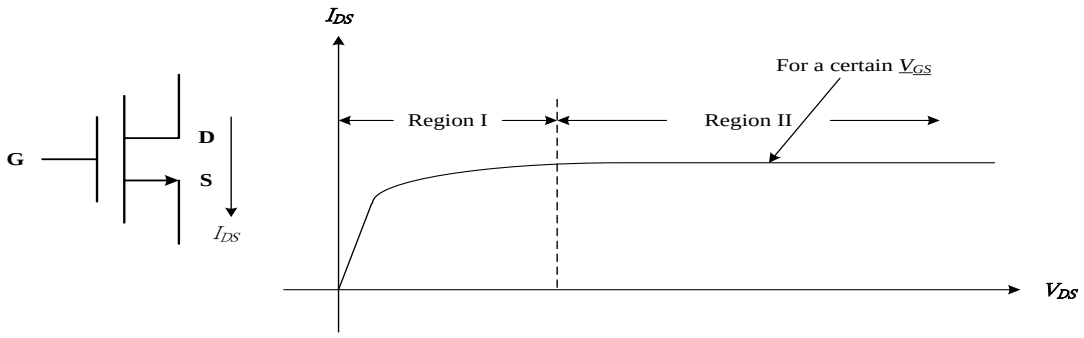


Fig 2-5. I-V curve of an NMOS transistor

At the very beginning, as V_{DS} first increases, I_{DS} increases linearly. After V_{DS} reaches a certain point, I_{DS} stops increasing and almost remains a constant. Therefore, we say that there are two regions as indicated in Fig. 2.4. Region I is called the triode, or ohmic, region and Region II is called the saturation, or constant current, region. For Region I, the transistor almost behaves as a resistor because for a resistor, the current increases linearly with respect to the voltage across it. That is why this region is also called the ohmic region[24].

For different V_{GS}'s, there are different I_{DS} vs V_{DS} curves, as shown in Fig. 2.5. It can be seen that the higher V_{GS} is, the higher I_{DS} is.

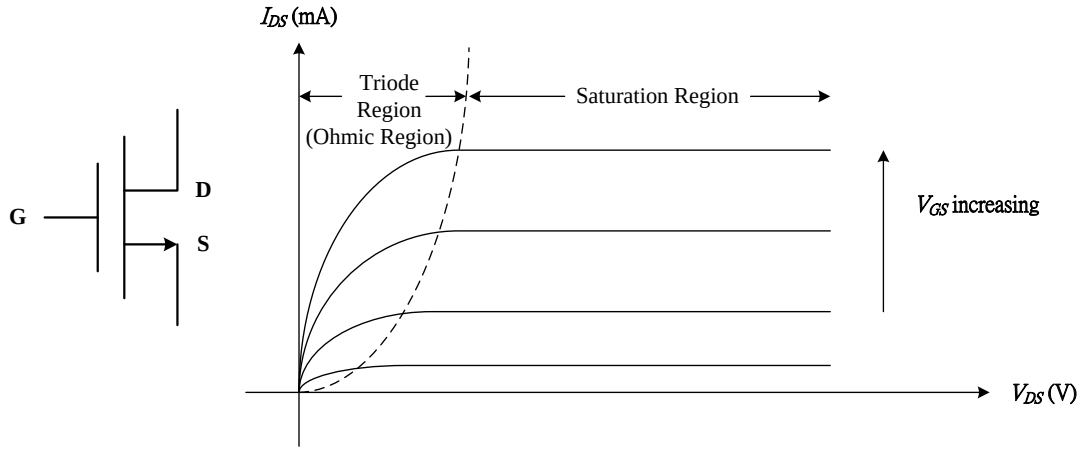


Fig. 2-6 I-V curve of an NMOS transistor for different V_{GS}'s.

The Current in the Saturation Region:

In this section, we present a formula for the current in the saturation region. There exists a certain threshold for V_{GS}. This threshold is called V_t. The transistor is cutoff if $V_{GS} < V_t$. V_t is usually quite small. If $V_{DS} \le V_{GS} - V_t$, the transistor is in the triode region; otherwise, it is in the saturation region, as shown in Fig. 2.7

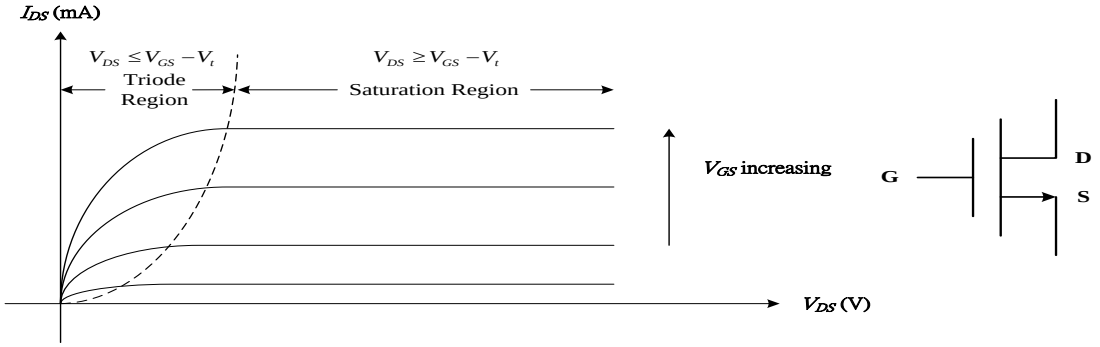


Fig. 2-7 The threshold voltage V_t of an NMOS transistor.

In the triode region, obviously, I_{DS} is a function of both V_{GS} and V_{DS}. The relationship is given by the following formula:

$$I_{DS} = K_L' \left(\frac{W}{L} \right) \left((V_{GS} - V_t) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right) \qquad (2\text{-}1)$$

where K_L' is a constant and W and L are the width and length of the gate respectively. The parameter K_L' is given by the integrated circuit manufacturing process model. At the boundary between the triode and saturation regions, we have

$$V_{DS} = V_{GS} - V_t \qquad (2\text{-}2)$$

and $$I_{DS} = \frac{1}{2} K_L' \left(\frac{W}{L} \right) (V_{GS} - V_t)^2 \qquad (2\text{-}3)$$

Although Equation (2-3) is derived by assuming $V_{DS} = V_{GS} - V_t$, it is valid for $V_{DS} > V_{GS} - V_t$ because once $V_{DS} > V_{GS} - V_t$, the transistor will be in the saturation region and I_{DS} will be constant in this region.

I_{DS} will now be independent of V_{DS} and is only a function of V_{GS}. Thus, we may easily see that Equation (2-3) holds if $V_{DS} \geq V_{GS} - V_t$. Equation (2-3) is illustrated in Fig.2.8. As will be seen later, V_{GS} will not be too large, except in some rare cases. Thus, I_{DS} is usually not very large either. Note that a large I_{DS} will cause a very large power consumption.

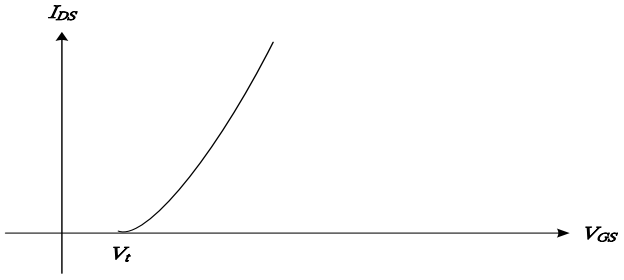


Fig. 2-8. The relationship between I_{DS} and V_{GS}.

Fig. 2-8 can be quite misleading because it somehow gives the reader the impression that I_{DS} grows with respect to V_{GS} without any limit. In practice, this is not the case, as explained in the next section

2.2 SOI BASICS

Silicon on insulator (**SOI**) technology is the use of a layered silicon-insulator-silicon substrate instead of conventional silicon substrates in semiconductor manufacturing to reduce parasitic device capacitance, thereby improving performance.

CMOS integrated circuits are almost exclusively fabricated on bulk silicon substrates for two well known reasons: the availability of electronic grade material and because a good quality oxide can be readily grown on silicon, a process which is not possible on germanium or on compound semiconductors. Yet modern MOSFET's made in silicon are far from the ideal structure. Bulk MOSFET's are made in silicon wafers having a thickness

2.3 SOI MOSFET:

It is of approximately 800 micrometers but only the first micrometer at the top of the wafer are used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects. One of these parasitic is the capacitance between diffused source and drain and substrate. This capacitance increases with substrate doping and becomes larger in modern submicron devices where the doping concentration in the substrate is higher than in previous MOS technologies.

In addition latchup which consist of the unwanted thyristor inherently present in all bulk CMOS structures becomes a serious problem in devices with small dimensions. The solution is SOI MOSFET.[25]

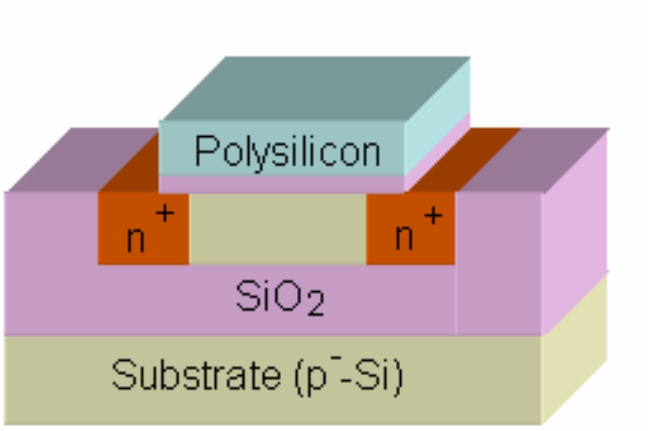


Fig 2-9: SOI Mosfet

In electronics an SOI MOSFET semiconductor device is a silicon on insulator (SOI) MOSFET structure in which a semiconductor layer, e.g. silicon, germanium or the like, is formed above an insulator layer which may be a buried oxide (BOX) layer formed in a semiconductor substrate.[26][27][28].

The MOSFET is the most widely used SOI device. SOI MOSFET's exhibit interesting properties that make them particularly attractive for applications such as radiation hard circuits and high temperature electronics. The physics of the SOI MOSFET is highly depended on the thickness and doping concentration of the silicon film in which they are made

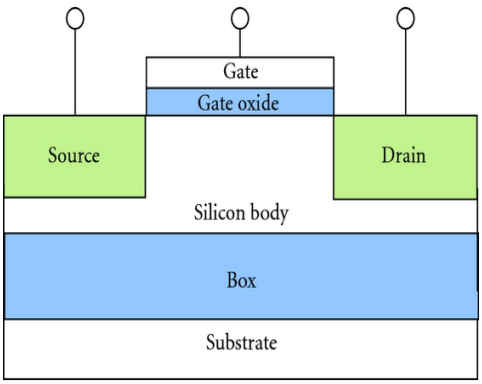


Figure 2-10: Soi mosfet with drain source and gate connection

The SOI MOSFET structure is shown in figure 2.10. It contains the traditional three terminals (source, drain and gate which controls a channel in which current flows from source to drain).The full dielectric isolation of devices prevents the occurrence of most of the parasitic effects experienced in bulk silicon devices. Most parasitic effects in bulk MOS devices find their origin in the interactions between the device and the substrate.

Latch up in bulk devices finds its origin in the PNPN structure of the CMOS inverter. The latchup can be symbolized by two bipolar transistors formed by the substate, the well and the source and drain junctions. For latchup to occur the current gain of the loop formed by the two transistors should be greater than one..

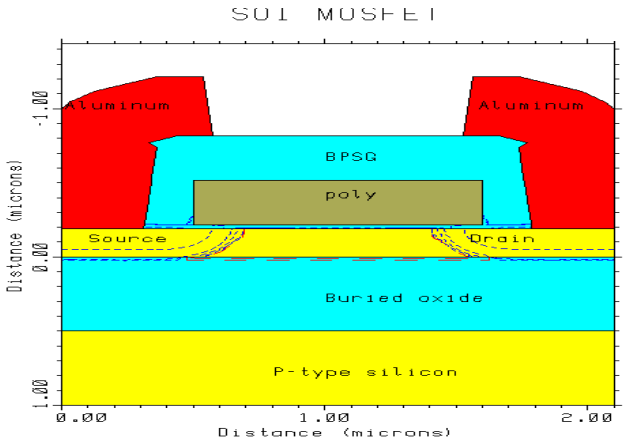


Figure 2-11: regions of SOI mosfet

In an SOI CMOS inverter the silicon film containing the active devices is thin enough for the junction to reach through to the buried insulator.

The cross section of SOI compared to bulk is as shown in fig 2.12 . SOI structures do not vary much from normal bulk CMOS. The major difference is the insertion of the insulation layer beneath the devices. Suppression of bottom junctions lowers parasitic capacitance and makes faster switching and/or lower power dissipation. The full isolation in SOI provide no latch-up, denser layout, lower interferences between the analog and digital parts, lower losses in the passive components at high frequency, lower leakage

current, enabling operation at higher temperature (250°C), thin active area and lower sensitivity to radiations

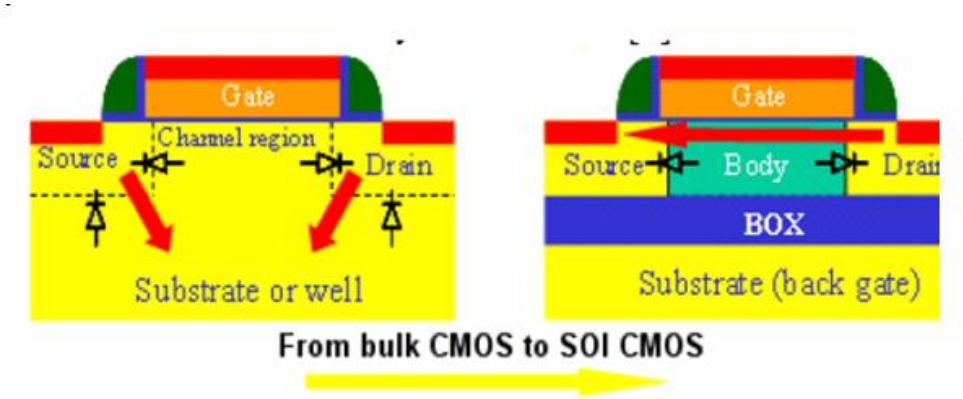


Figure 2-12: migration from bulk to SOI structure

Two types of devices can be distinguished: devices in which the silicon film in the channel region is never completely depleted called partially depleted MOSFET or PD MOSFET. The other type of device where silicon film can be completely depleted is called fully depleted MOSFET or FD MOSFET[29].

PD MOSFET: The silicon film thickness is larger than twice the value of maximum depletion width. In such a case there is no interaction between the depletion zones arising out from the front and back interfaces. A neutral region exists beneath the depletion regions. If this neutral peace of silicon called body is connected to ground by a body contact the characteristic of the device will be exactly those of a bulk device

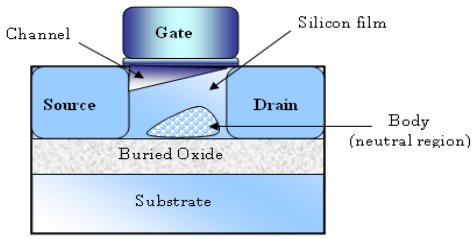


Figure 2-13: PDSOI MOSFET

FD MOSFET: The silicon film thickness is smaller than maximum depletion width. In this case the silicon film is completely depleted at threshold, irrespective of the bias applied at the back gate.

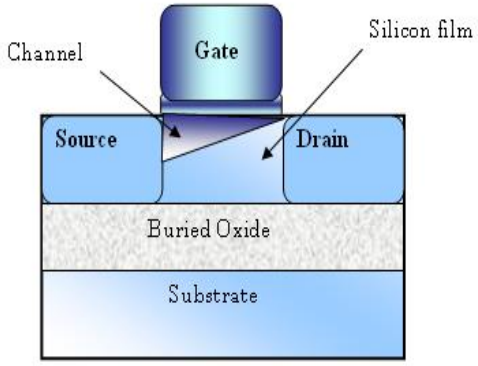


Figure 2-14: FD SOI MOSFET

- Partially Depleted
  - $2X_d < t_{Si}$
- Fully Depleted
  - $2X_d > t_{Si}$

Uses: SOI MOSFET devices are adapted for use by the computer industry. The buried oxide layer can be used in SRAM memory designs.[30]

There are two important characteristics of SOI MOSFETs: the kink effect and lattice heating.

2.3.1 Electrical Properties of SOI MOSFET

A. Threshold Voltage and Leakage Current

Process variability alters the ratio of forward and reverse diode leakages, which will establish new balanced voltages. Shorter channels will also produce more impact ionization, resulting in more history effect. Conducting Hot Electron generation also simultaneously presents as degradation in device current. This degradation's dependence on channel length, and hence the electron-hole pair generation for a typical production CMOS technology. Shorter channels also produce bodies with less total voluless charge, and the decreased volume reduces the time necessary to achieve large excursions in body potential. Voltage of the supply affects junction leakage, and will affect the body potential. Temperature strongly affects junction leakage and device threshold voltage. Lower threshold voltage at higher temperatures increases the portion of the electron energy distribution capable of ionizing silicon lattice points. This again affects the potential where the current into the body is balanced with the current out of the body. Temperature also affects the leakages of the junctions themselves, directly affecting body charge content. The most prominent electrical property of the PD-SOI device is the History Effect. I-V characteristics of the MOSFET built in PD-SOI are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body and the distribution of that charge caused by gate, source, and drain potentials determine the behavior of the device. Charge in the body is directly related to the potential of the body. The dependence of MOSFET threshold voltage on substrate bias is well known. Conceptually, body bias's effect on threshold voltage may be explained by how strongly this

potential reverse-bias the junctions, which must be overcome by gate drive. The magnitude of charge contained in the body is dependent on a number of factors which include: Previous state of transistor, Schematic position of transistor, Slew rate of input, and load capacitance, Channel length and processing corner, Operating supply voltage, Junction temperature, Operating frequency and specific switch factor.

B. Subthreshold Analysis

The Subthreshold behaviour of an SOI MOS[31] device depends on the thickness of the silicon thin-film, the doping density of the silicon thin-film, and the channel length. When the silicon thin-film is thick, partially depleted, the subthreshold slope of the SOI n-MOSFET device is similar to that of the bulk devices. When the silicon thin-film is thin, fully depleted, its subthreshold slope is much better with its value close to the ideal case due to the buried oxide isolation between the channel and the grounded substrate. For a partially depleted device, a higher silicon thin film doping density leads to a worse inverse subthreshold slope silima to the bulk device. A hump in the subthreshold characteristics can be seen in mesa isolated SOI n-MOSFETs. The hump is caused by the 2D effect, which results in a smaller threshold voltage for the sidewall channel as compared to the center channel.

C. Kink Effect

The kink effect is characterized by the appearance kink in the output characteristics of an SOI MOSFET. The kink appears above a certain drain voltage. It is not observed in bulk devices at room temperature when substrate or well connections are provided but it can be observed in bulk MOSFET's operating at low temperatures Kink effect can be explained as follows. Consider a partially depleted SOI n-channel transistor. When the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs, due to impact ionization mechanism. The generated electrons move rapidly into the channel and the drain while the hole migrates towards the place of lowest potential i.e. floating body. The injection of holes into the floating body forward biases the source body diode. The increase of the body potential gives rise to a decrease of threshold voltage. This decrease of threshold voltage induces an increase of the drain current as a function of drain

voltage which can be observed in the output characteristics of device as a kink.

D. Lattice Heating

SOI MOSFET's are thermally insulated from the substrate by the buried insulator. As a result, removal of excess heat generated within the device is less efficient than in bulk, which results in substantial elevation of device temperature. The conduction paths for excess heat are multiple: heat diffuces mostly vertically through the buried oxide but some of it through the siliconisland into the contacts and metallization. Due to self heating , a negative resistance can be seen in the output characteristics of SOI MOSFET. It is due to mobility reduction effect caused by the elevation of temperature. This effect is clearly visible on the output characteristics if sufficient power is dissipated in device. Because of the relatively low conductivity of oxide layer, device can heat up by 50-100 degrees and mobility reduction is observed. This effect has been included in device and circuit simulator.

2.3 SCHRODINGER AND POSSION EQUATIONS:

2.3 Schrodinger and possion equations:

2.3.1 Schrodinger equation:

A general procedure to solve quantum mechanical problems was proposed by Erwin Schrödinger. Starting from a classical description of the total energy, E, which equals the sum of the kinetic energy, K.E., and potential energy, V, or

$$E = K.E + V = \frac{p^2}{2m} + V(x) \qquad (1)$$

he converted this expression into a wave equation by defining a wave function, Y, and multiplied each term in the equation with that wavefunction

$$E\Psi = \frac{p^2}{2m}\Psi + V(x)\Psi \quad (2)$$

To incorporate the de Broglie wavelength of the particle the operator, $-\frac{\hbar^2\partial^2}{\partial x^2}$, can be introduced, which provides the square of the momentum, p, when applied to a plane wave,

$$-\hbar^2\frac{\partial 2\Psi}{\partial x^2} = \hbar^2 k^2\,\Psi = p^2\Psi, \text{ for } \Psi = e^{i(kx-\omega t)} \quad (3)$$

Where k is the wave number, which equals 2p/l. Without claiming that this is an actual proof, we now simply replace the momentum squared, p^2, in equation (2) by this operator yielding the time-independent Schrödinger equation.

$$-\frac{\hbar^2}{2m}\frac{d^2\Psi(x)}{dx^2} + V(x)\Psi(x) = E\Psi(x) \quad (4)$$

To illustrate the use of Schrödinger's equation, two solutions can be presented to Schrödinger's equation, that for an infinite quantum well and that for the hydrogen atom.

2.3.1.1 Physical interpretation of the wavefunction

The use of a wavefunction to describe a particle, as in the Schrödinger equation, is consistent with the particle-wave duality concept. However, the physical meaning of the wavefunction does not naturally follow. Quantum theory postulate states that the wavefunction, $\psi(x)$, multiplied with its complex conjugate, $\psi^*(x)$, is proportional to the probability density function, $P(x)$, associated with that particle.

$$P(x) = \Psi(x)\Psi(x) \quad (5)$$

This probability density function integrated over a specific volume provides the probability that the particle described by the wavefunction is within that volume. The probability function is frequently normalized to indicate that the probability of finding the

particle somewhere equals 100%. This normalization enables to calculate the magnitude of the wavefunction using the following equation:

$$\int_{-\infty}^{\infty} P(x)dx = 1 \qquad (6)$$

This probability density function can be used to find all properties of the particle by using the quantum operators. To find the expected value of a function *f*(*x*,*p*) for the particle described by the wavefunction, the following equation can be used:

$$< f(x,p) >= \int_{-\infty}^{\infty} \Psi(x)F(x)\Psi^*(x)dx \qquad (7)$$

Where *F*(*x*) is the quantum operator associated with the function of interest. A list of quantum operators corresponding to a selection of common classical variables is provided in Table 2.2.

	Classical Variable	Quantum operator
Position	x	x
A function which depends only on position	$f(x)$	$F(x)$
Momentum	p	$\frac{\hbar}{i}\frac{\partial}{\partial x}$
Energy	E	$-\frac{\hbar}{i}\frac{\partial}{\partial t}$

Table 2.2 Selected classical variables and the corresponding quantum operator.

2.3.1.2 The infinite quantum well

The one-dimensional infinite quantum well represents one of the simplest quantum mechanical structures. It is used to illustrate some specific properties of quantum mechanical systems. The potential in an infinite well is zero between $x = 0$ and $x = L_x$ and is infinite on either side of the well. The potential and the first five possible energy levels an electron can occupy are shown in Figure 2.15:

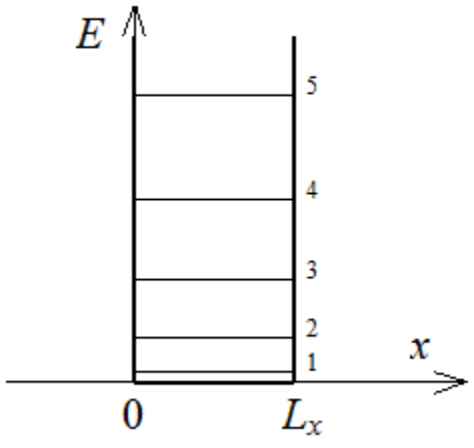


Figure 2-15: Potential energy of an infinite well, with width L_x. Also indicated are the lowest five energy levels in the well.

The energy levels in an infinite quantum well are calculated by solving Schrödinger's equation (4) with the potential, $V(x)$, as shown in Figure 2.15. As a result the following equation can be solved within the well.

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} = E\Psi(x), \text{ for } 0 < x < L_x \qquad (8)$$

The general solution to this differential equation is :

$$\psi(x) = A\sin(\frac{\sqrt{2mE}}{\hbar}x) + B\cos(\frac{\sqrt{2mE}}{\hbar}x), \text{ for } 0 < x < L_x \qquad (9)$$

where the coefficients *A* and *B* must be determined by applying the boundary conditions. Since the potential is infinite on both sides of the well, the probability of finding an electron outside the well and at the well boundary equals zero. Therefore the wave function must be zero on both sides of the infinite quantum well or:

$$\psi(0) = 0 \text{ And } \Psi(L_x) = 0 \tag{10}$$

These boundary conditions imply that the coefficient *B* must be zero and the argument of the sine function must equal a multiple of pi at the edge of the quantum well or:

$$\frac{\sqrt{2mE_n}}{\hbar} L_x = n\pi, \text{ with } n = 1,2, \ldots. \tag{11}$$

Where the subscript *n* was added to the energy, *E*, to indicate the energy corresponding to a specific value of,*n*. The resulting values of the energy, E_n, are then equal to:

$$E_n = \frac{h^2}{2m}\left(\frac{n}{2L_x}\right)^2, \text{ with n=1,2,}\ldots. \tag{12}$$

The corresponding normalized wave functions are given by following equation:

$$\psi_n(x) = \sqrt{\frac{2}{L_x}}\sin\left(\frac{\sqrt{2mE_n}}{\hbar}x\right), \text{ for } 0 < x < L_x \tag{13}$$

where the coefficient *A* was determined by requiring that the probability of finding the electron in the well equals unity or:

$$\int_0^{L_x} \psi_n(x)\psi_n^*(x)dx = 1 \tag{14}$$

The asterisk denotes the complex conjugate.

Here the lowest possible energy, namely E_1, is not zero although the potential is zero within the well. Only discrete energy values are obtained as eigen values of the Schrödinger equation. The energy difference between adjacent energy levels increases as the energy increases. An electron occupying one of the energy levels can have a positive

or negative spin (s = ½ or s = -½). Both quantum numbers, n and s, are the only two quantum numbers needed to describe this system.

The wavefunctions corresponding to each energy level are shown in Figure 2.16 (a). Each wavefunction has been shifted by the corresponding energy and scaled with an arbitrary magnitude. The probability density function, $P(x)= \psi(x)^*\psi(x)$, provides the probability of finding an electron at a certain location in the well. These probability density functions are shown in Figure 2.16 (b) for the first five energy levels. For instance, for n = 2 the electron is least likely to be in the middle of the well and at the edges of the well. The electron is most likely to be one quarter of the well width away from either edge.

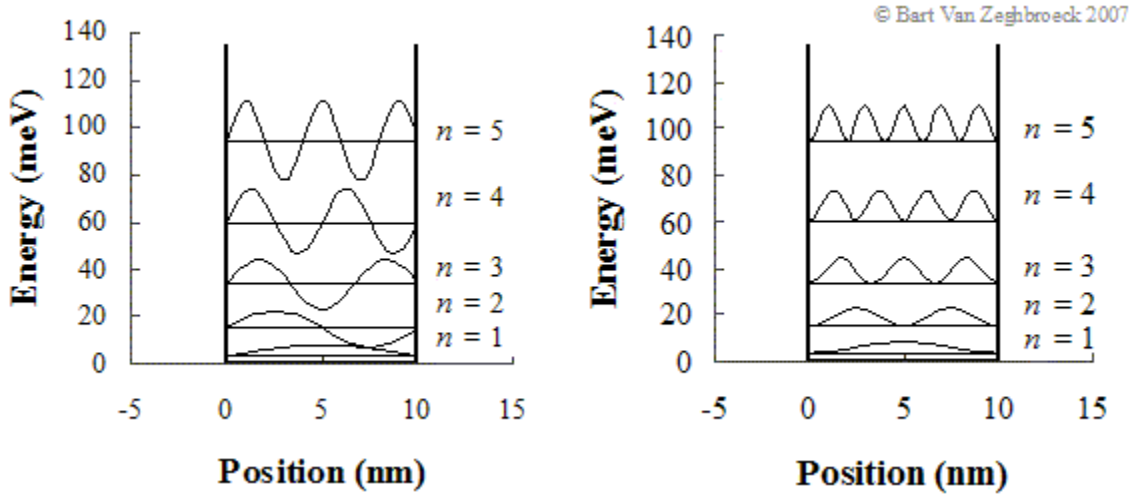


Figure 2.16: (a) Energy levels, wavefunctions and (b) probability density functions in an infinite quantum well. The figure is calculated for a 10 nm wide well containing an electron with mass m_0. The wavefunctions and the probability density functions have an arbitrary magnitude (i.e. they are not normalized) and are shifted by the corresponding electron energy.

2.3.2 Poisson's equation

The electric field is defined as minus the gradient of the electrostatic potential, $\boldsymbol{\varepsilon}$, or, in one dimension, as minus the derivative of the electrostatic potential. It can be specified by the following equation:

$$\frac{d\phi(x)}{dx} = -\varepsilon(x) \tag{15}$$

The electric field vector therefore originates at a point of higher potential and points towards a point of lower potential.

The potential can be obtained by integrating the electric field. It can be described by the following equation:

$$\phi(x_2) - \phi(x_1) = -\int_{x_1}^{x_2} \varepsilon \, dx \tag{16}$$

At times, it is convenient to link the charge density to the potential by combining equation (15) with Gauss's law, the following equation is obtained:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon} \tag{17}$$

which is referred to as Poisson's equation

For a three-dimensional field distribution, the gradient of the potential is described by:

$$\vec{\nabla}\phi(x,y,z) = -\vec{\varepsilon}(x,y,z) \tag{18}$$

2.4 DESCRIPTION OF THE SIMULATION TOOL

Technology–Computer Aided Design (TCAD) is one of the most commonly used simulation tools. It helps the engineers to save time, cost and also reduce the complexity of the original design during the designing process using the available detail of the semiconductor properties. This is a very powerful tool as it could show the result as close as the actual process. This simulation tool does not require any applied of complicated formula and the command were more easy to understand. This simulation software is able to model the two dimensional on the electrical characteristics when bias condition is applied. Two types of simulation tools

1. Athena: It is the process simulator, which is used to predict the physical structures of the processing steps..

2. Atlas: also has the same feature as athena to construct the structure of the device but only in a simple form.

2.5 ATLAS FRAMEWORK

Atlas is a modular and extensible framework for one, two and three dimensional semiconductor device simulation. It is implemented using modern software engineering practices that promote reliability, maintainability, and extensibility. Products that use the atlas Framework meet the device simulation needs of all semiconductor application areas.

Atlas is a physical-based device simulator used for device simulation, which have 3 major advantages. They are predictive, provide insight and captures theoretical knowledge that will benefit the non-experts.

Atlas is a good combination of sophisticated in–depth device analysis in 2D or 3D. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

2.6 ATLAS CODING PROCESS

Most atlas simulations use two input files. The first input file is a text file that contains commands for atlas to execute. The second input file is a structure file that defines the structure that will be simulated.

Atlas produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point.

2.6.1 Input File Structure

Silvaco Atlas receives input files through DeckBuild. Each Atlas run inside DeckBuild should start with the following command:

go atlas

A single input file may contain several Atlas runs each separated with a go atlas line.
Atlas follows the following format for statements and parameters:

<STATEMENT><PARAMETER>=<VALUE>

For any <STATEMENT>, may have four different types for the <VALUE> parameter. These are: Real, Integer, Character, and Logical.

2.6.2 Stucture Specification

The structure specification is done by defining the mesh, the region, the electrodes and the doping levels.

To define a device through the atlas command language, a mesh must be defined first. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to construct the device. After the regions are defined, the location of electrodes is specified. The final step is to specify the doping in each region.

When using the command language to define a structure, the information described in the following four sub-sections must be specified in the order listed

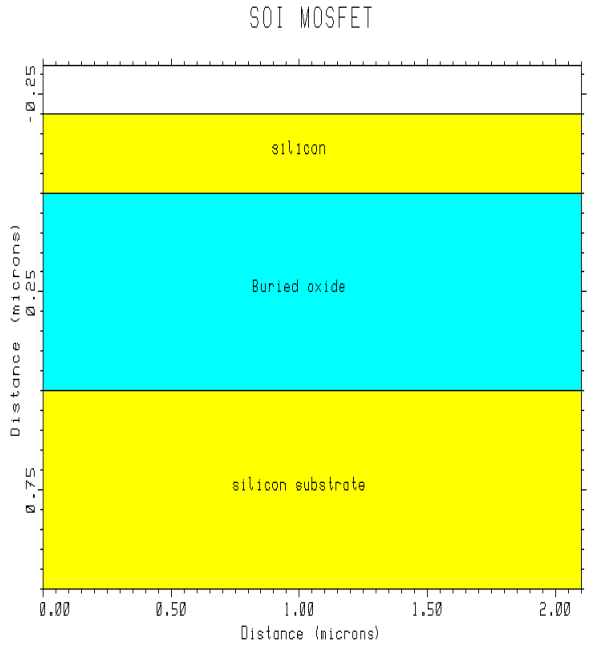


Figure 2-17: SOI structure

2.6.2.1 Mesh

The mesh used for this thesis is two-dimensional. Therefore, only *x* and *y* parameters are defined. The mesh is a series of horizontal and vertical lines and spacing between them.

The general format to define the mesh is:

X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>

The X.MESH and Y.MESH statements are used to specify the locations in microns of vertical and horizontal lines, respectively, together with the vertical or horizontal spacing associated with that line. At least two mesh lines must be specified for each direction.

2.6.2.2 Region

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements. The format to define the regions is as follows:

REGION number=<integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased. If a composition-dependent material type is defined, the x and y composition fractions are specified in the REGION statement.The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

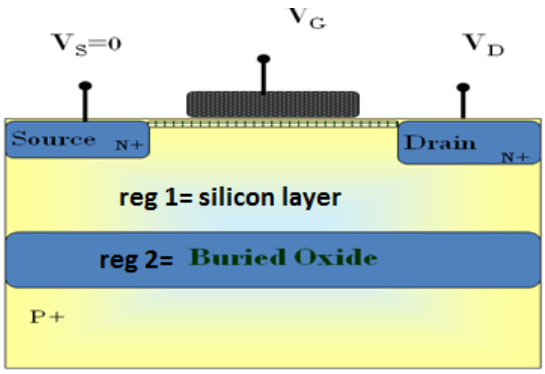


Figure 2-18: regions are defined

2.6.2.3 Electrodes

The next structure specification corresponds to electrodes. Typically, in this simulation the only electrodes defined are the anode and the cathode. However, Silvaco Atlas has a limit of 50 electrodes that can be defined. The format to define electrodes is as follows:

ELECTRODE NAME=<electrode name> <position_parameters>

Multiple electrode statements may have the same electrode name. Nodes that are associated with the same electrode name are treated as being electrically connected.

2.6.2.4 Doping

The last aspect of structure specification that needs to be defined is doping. The format of the Atlas statement is as follows:

DOPING <distribution type><dopant_type><position parameters>

2.6.3 Materials Model Specification

After the structure specification, the materials model specification is next. The materials model specification can be classified into material, models, contact, and interface.

2.6.3.1 Materials

The format for the material statement is as follows:

MATERIAL <localization><material_definition>

2.6.3.2 Models

The physical models fall into five categories:mobility, recombination, carrier statistics, impactionization, and tunneling. The syntax of the model statement is as follows:

MODELS <model flag><general parameter><model dependent parameters>

2.6.3.3 Contact

Contact determines the attributes of the electrode. The syntax for contact is as follows:

CONTACT NUMBER=<n> |NAME=<ename>|ALL

The following is an example of the contact statement.

CONTACT NAME=anode current

2.6.3.4 Interface

The semiconductor or insulator boundaries are determined with the interface statement. The syntax is as follows:

INTERFACE [<parameters>]

2.6.4 Numerical Method Calculation

After the materials model specification, the numerical method selection must be specified.

There are three types of solution techniques used in Silvaco Atlas:

1. Decoupled (GUMMEL) : The GUMMEL method solves for each unknowns by keeping all other unknowns constant. The process is repeated until there is a stable solution. It is used for a system of equations that are weakly coupled and there is linear convergence.

2. Fully coupled (NEWTON): The NEWTON method solves all unknowns simultaneously. used when equations are strongly coupled and there is quadratic convergence.

3. BLOCK: The BLOCK method solves some equations with the GUMMEL method and some with the NEWTON method.

2.6.5 Solution specification

After completing the numerical method selection, the solution specification is next.

2.6.5.1 LOG

LOG saves all terminal characteristics to a file. DC, transient, or AC data generated by a SOLVE statement after a LOG statement is saved.

The following shows an example of the LOG statement.

LOG OUTFILE=myoutputfile.log

The example saves the current-voltage information into myoutputfile.log.

2.6.5.2 Solve

The SOLVE statement follows the LOG statement. SOLVE performs a solution for one or more bias points. The following is an example of the SOLVE statement.

**SOLVE B1=10 B3=5 BEAM=1 SS.PHOT SS.LIGHT=0.01 **

MULT.F FREQUENCY=1e3 FSTEP=10 NFSTEP=6

B1 and B3 specify the optical spot power associated with the optical beam numbers 1 and 3, respectively. The beam number is an integer between 1 and 10. BEAM is the beam number of the optical beam during AC photogeneration analysis. SS.PHOT is the small signal AC analysis. SS.LIGHT is the intensity of the small signal part of the optical beam during signal AC photogeneration analysis. MULT.F is the frequency to be multiplied by FSTEP. NFSTEPS is the number of times that the frequency is incremented by FSTEP.

2.6.5.3 Load And Save

The LOAD statement enters previous solutions from files as initial guess to other bias points. The SAVE statement enters all node point information into an output file. The following are examples of LOAD and SAVE statements.

SAVE OUTF=SOL.STR

In this case, SOL.STR has information saved after a SOLVE statement. Then, in a different simulation, SOL.STR can be loaded as follows:

LOAD INFILE=SOL.STR 67

2.6.5 Result Analysis

Once a solution has been found for a semiconductor device problem, the information can be displayed graphically with TonyPlot.

Chapter 3

Result and Discussion

3.1 Basic Structure

3.2 Threshold, Subthreshold and Output Curve

3.3 Band Diagram

3.4 Changing characteristics Curve with different parameters

Numerical simulation is an extremely helpful tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices.

Simulation results we present in this study had been obtained using Atlas SILVACO Software .

3.1 BASIC STRUCTURE

The below structure is obtained using ATLAS device simulation using

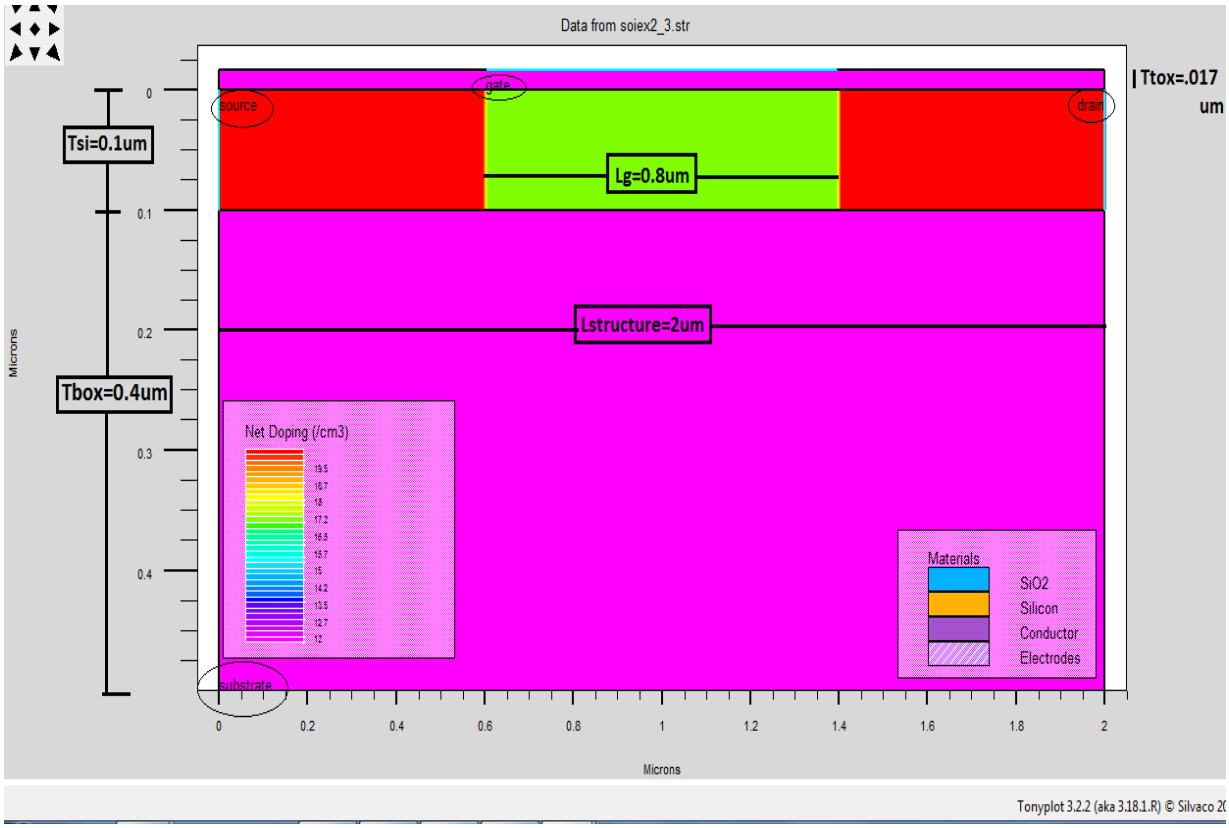


Figure 3-1: Basic structure of SOI MOSFET

Drain and source length are placed vertically

Gate length =0.8 um

Channel length =0.8um

Gate oxide thickness TOX=0.017um

Silicon film thickness tsi= 0.1µm

Buried oxide thickness TBOX=0.4um

Length of the structure=2um

Channel doping= 1e17 cm-3 p. type

Drain and Source doping=1e20 cm-3 n .type

3.2 THRESHOLD, SUB THRESHOLD AND OUTPUT CURVE:

3.2.1Threshold curve:

In our simulation we compare threshold curve at silicon thickness between 0.2um and 0.1um.

At Tsi=0.1um threshold voltage=0.5V

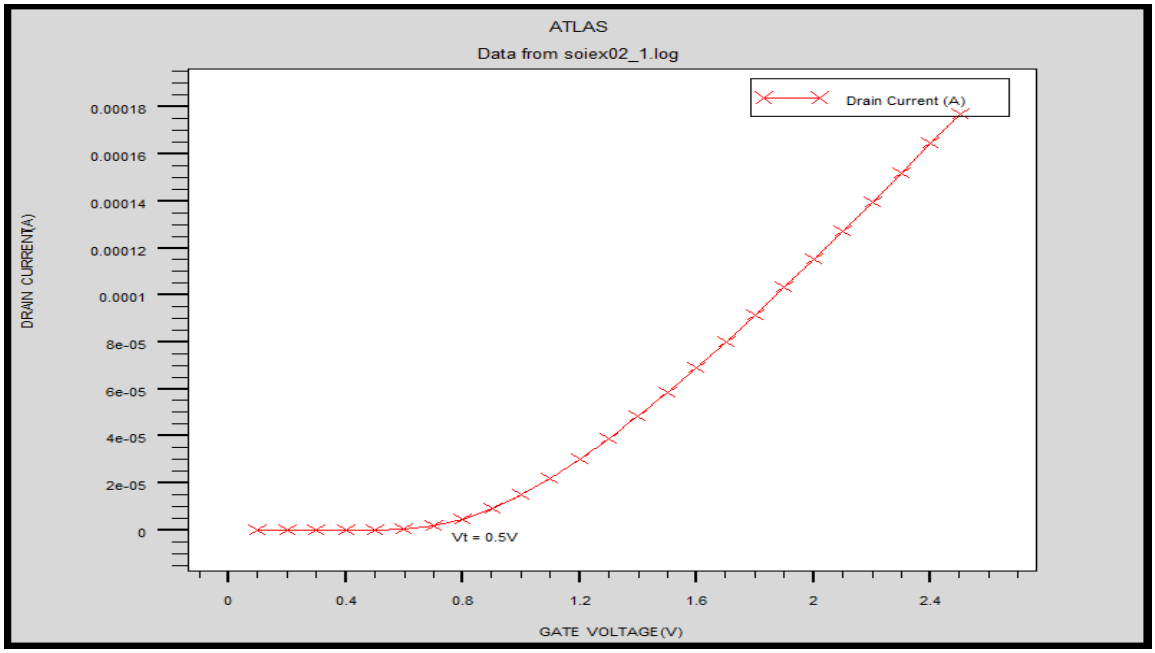


Figure 3-2: Threshold curve at Tsi=0.1um, Ttox=.017um,Tbox=0.4um

At Tsi=0.2um, threshold voltage=1v

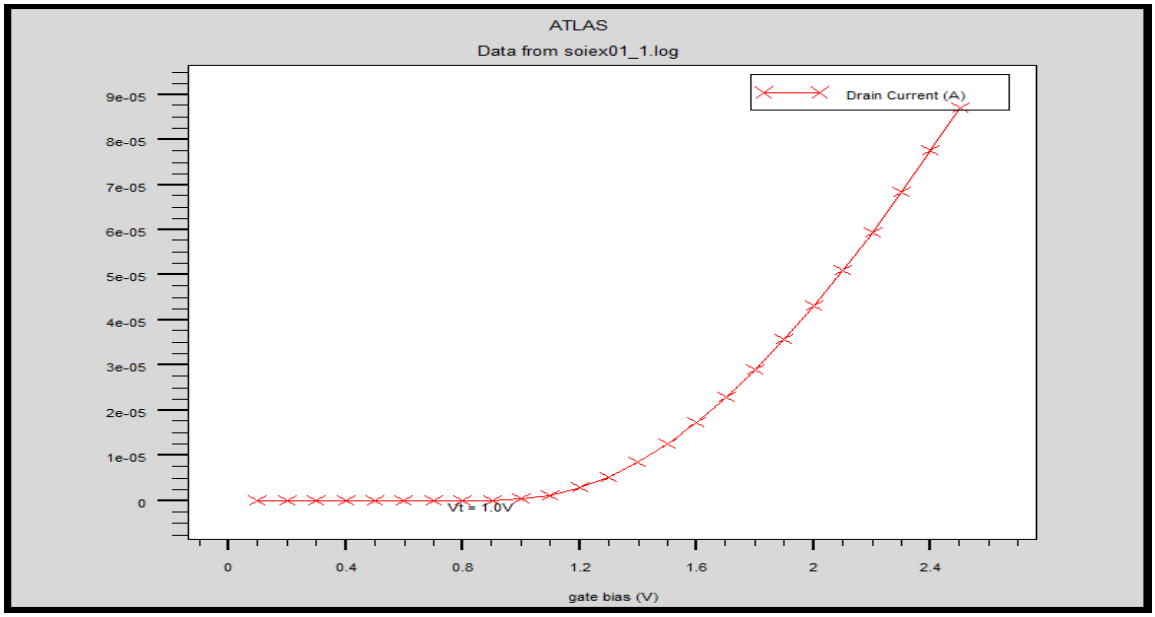


Figure 3-3: threshold curve at Tsi=0.2um, Tbox=0.4um,Ttox=0.017um

3.2.2. Sub threshold curve:

In our simulations, at Tsi=0.1um the sub threshold voltage=72 mv/decade

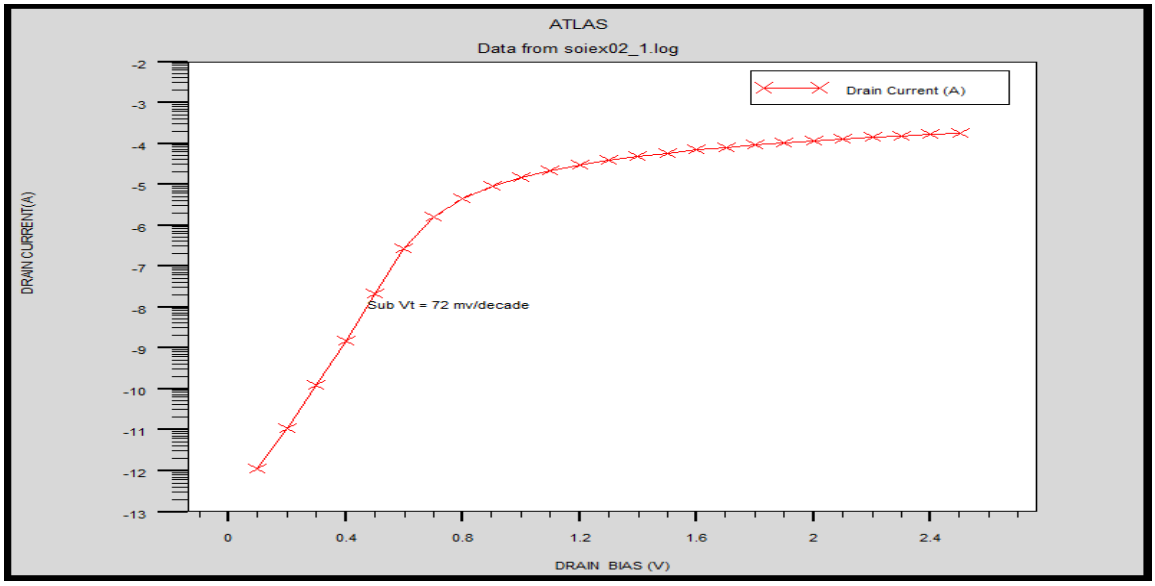


Figure 3-4: Sub threshold voltage curve at Tsi=0.1um, Ttox=.017um,Tbox=0.4um

At Tsi=0.2um sub threshold voltage=107 mv/decade

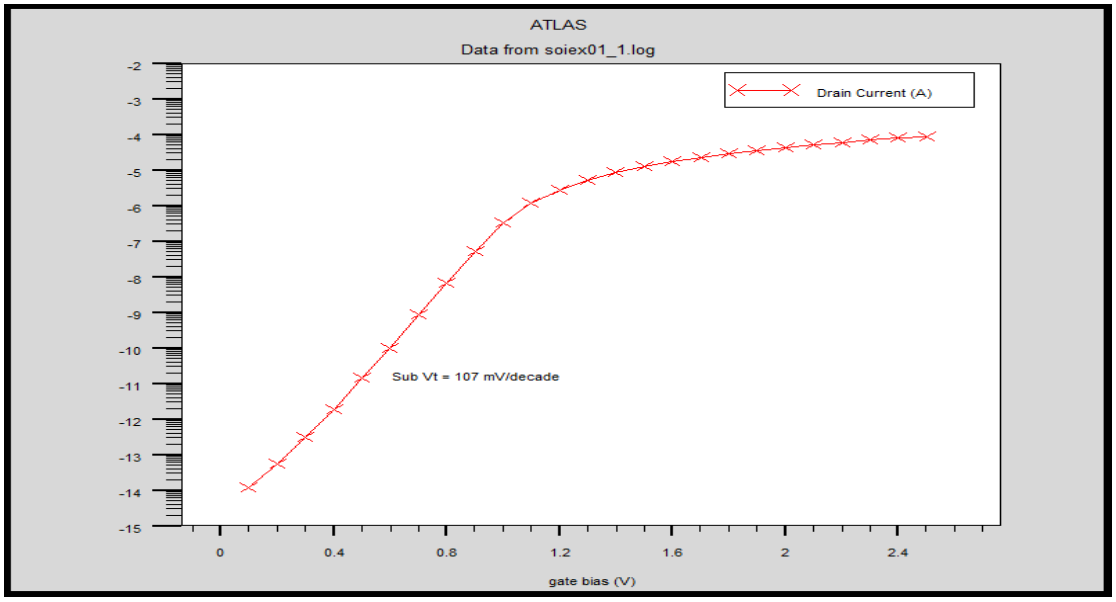


Figure 3-5: Sub threshold curve at Tsi=0.2um,Ttox=.017um,Tbox=0.4um

3.2.3 Output characteristics curve:

In our simulations we can see changes of drain current by applying different gate voltage

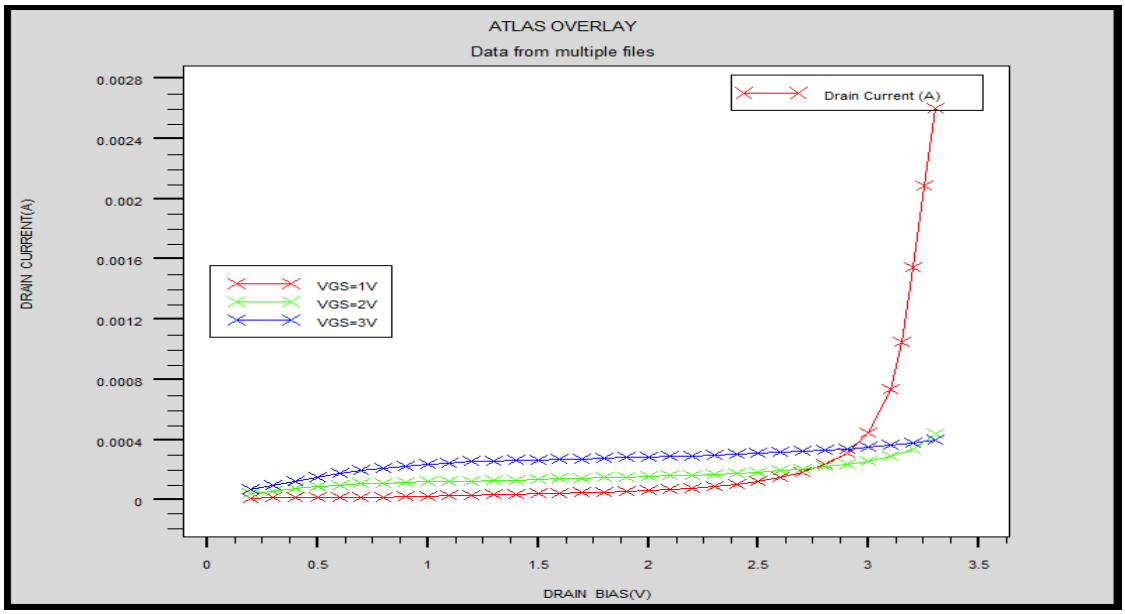


Figure 3-6: Simulated output characteristics curve at different gate voltage

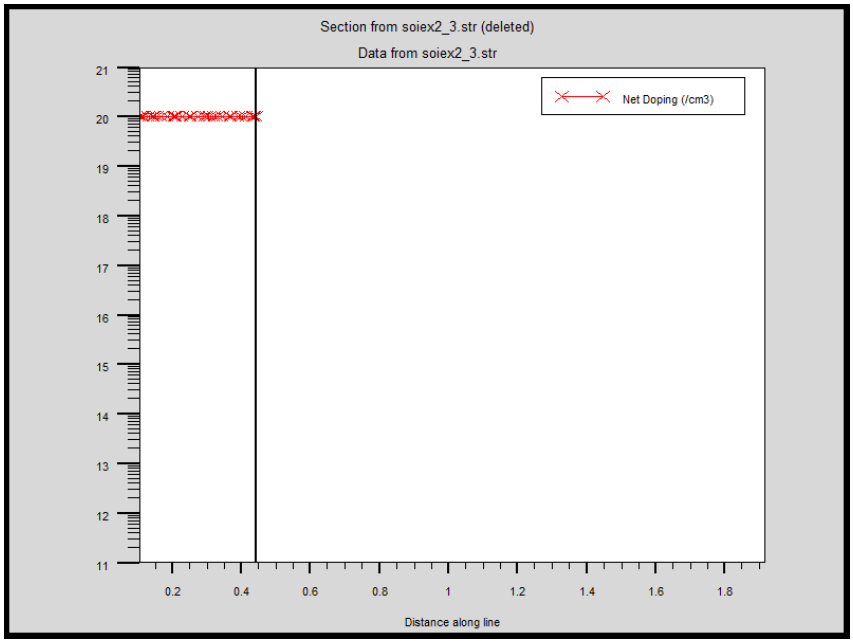
3.3 BAND DIAGRAM:

In our simulation we observed 3 types of band diagram

1. Net doping
2. Conduction band
3. Valence band

In our simulation, we work on two types of mosfets. The silicon thickness and doping concentration parameter differs those two mosfets. We do simulation there are some differences in the band diagram because of the variation of silicon thickness and doping concentration. The comparison of the diagram are given on the next page:

3.3.1.Net doping:



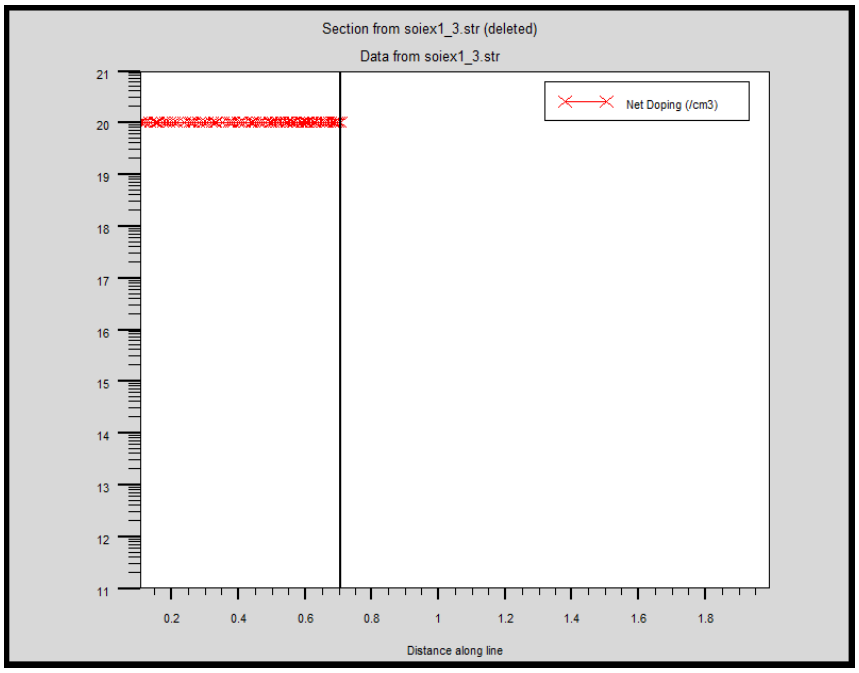
Tsi=0.1um

Tbox=.4um

Substrate doping=1e17cm-3 p type

Drain and source doping=1e20cm-3 ntype

Figure 3-7: Band diagram of net doping at Tsi=0.1um



Tsi=0.2um

Tbox=.4um

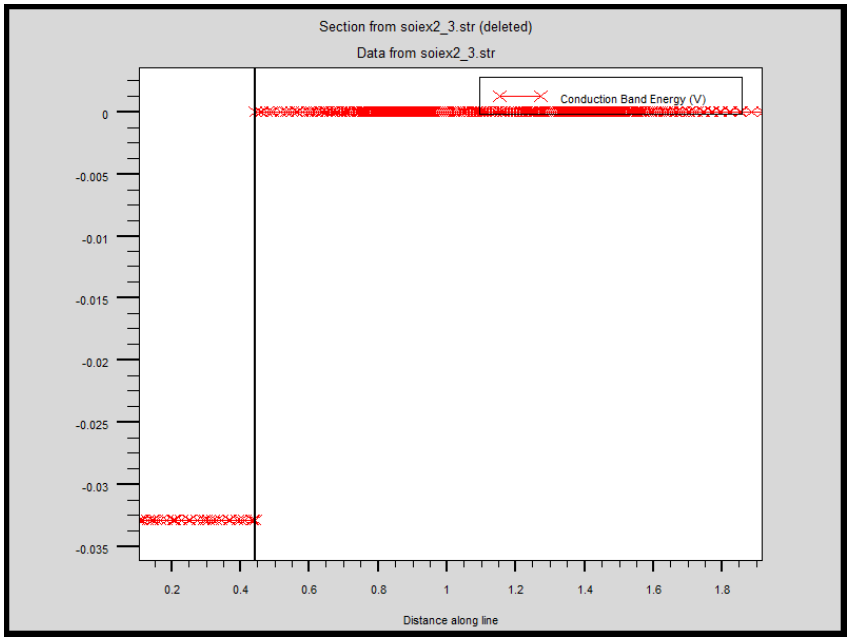
Substrate doping=2e17cm-3 p type

Drain and source doping=1e20cm-3 n type

Figure 3-8: band diagram of net doping at Tsi=0.2um

3.3.2.Conduction band energy:

The changes of the parameter are given on the right box



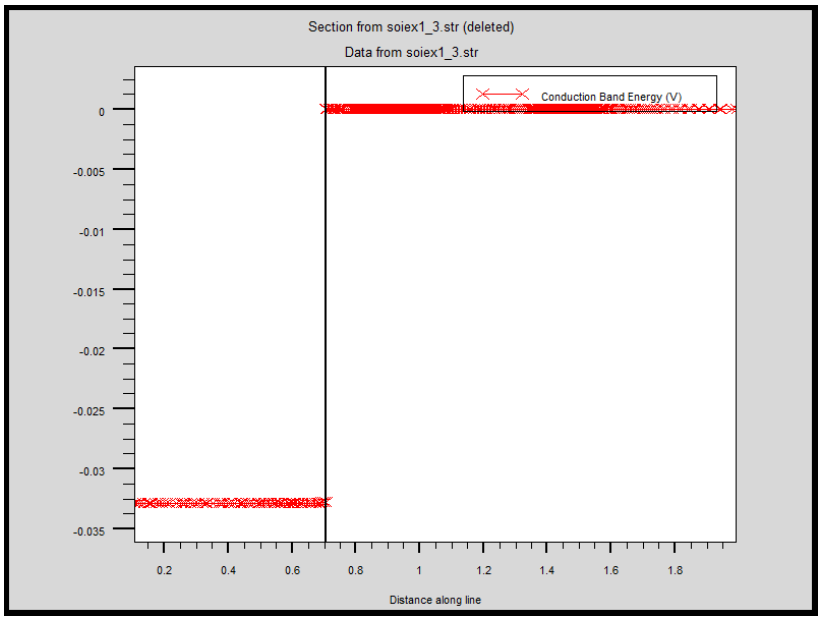
Tsi=0.1um

Tbox=.4um

Substrate doping=1e17cm-3 p type

Drain and source doping=1e20cm-3 n type

Figure 3-9:Band diagram of conduction band energy at Tsi=0.1um



Tsi=0.2um

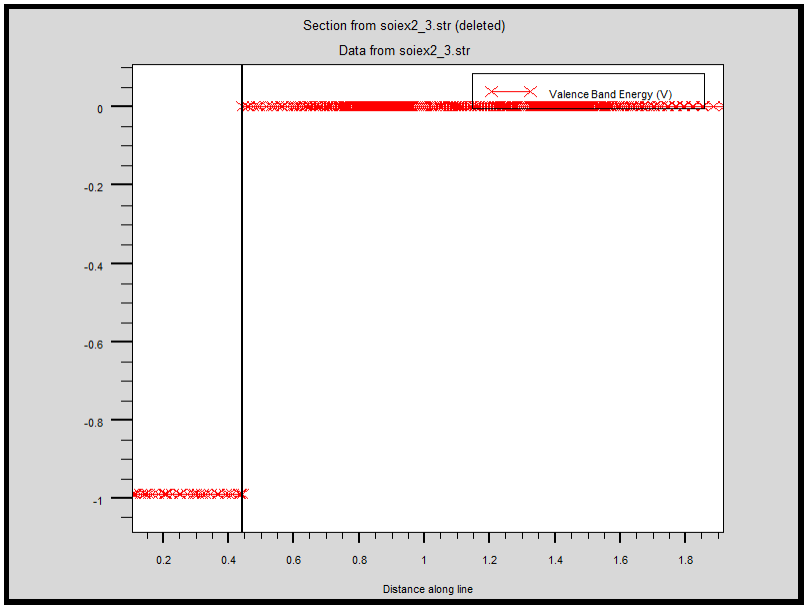
Tbox=.4um

Substrate doping=2e17cm-3 p type

Drain and source doping=1e20cm-3 ntype

Figure 3-10:Band diagram of conduction band energy at Tsi=0.2um

3.3.3.Valence band energy:



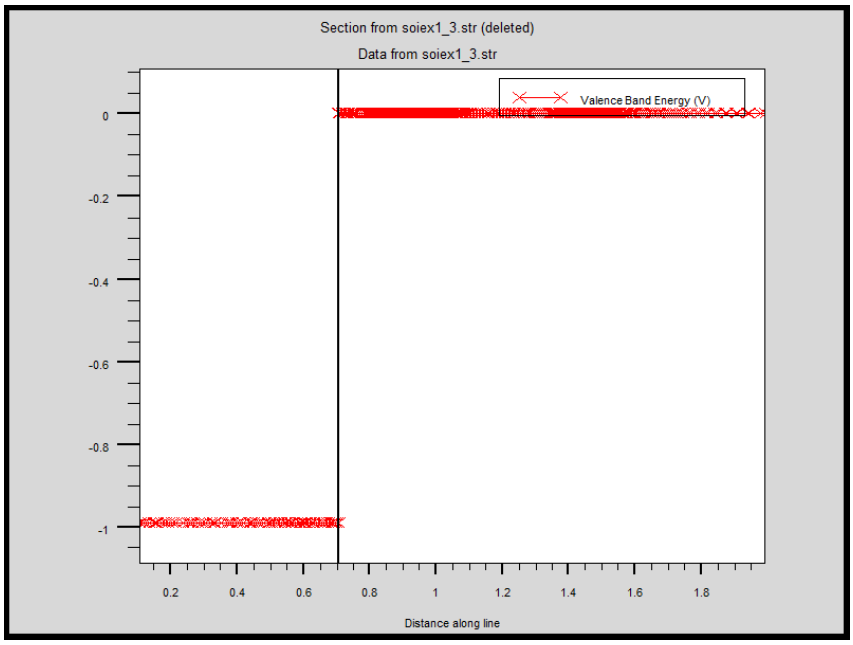
Tsi=0.1um

Tbox=.4um

Substrate doping=1e17cm-3 p type

Drain and source doping=1e20cm-3 ntype

Figure 3-11:Band diagram of valence band energy at Tsi=0.1um



Tsi=0.2um

Tbox=.4um

Substrate doping=2e17cm-3 p type

Drain and source doping=1e20cm-3 ntype

Figure 3-12:Band diagram of valence band energy at Tsi=0.2um

3.4 CHARACTERISTICS CURVE WITH DIFFERENT PARAMETER:

We can make variation of the characteristics curves like transfer characteristics curve and output characteristics curves by changing

1. Silicon body thickness
2. Gate oxide thickness
3. Channel length
4. Doping concentration

3.4.1: Influence of silicon body thickness on ID current:

Scaling silicon film thickness is desirable for better short channel behavior and reduced floating body effect. In practical it is consider the impact of silicon body thickness on the device performance.

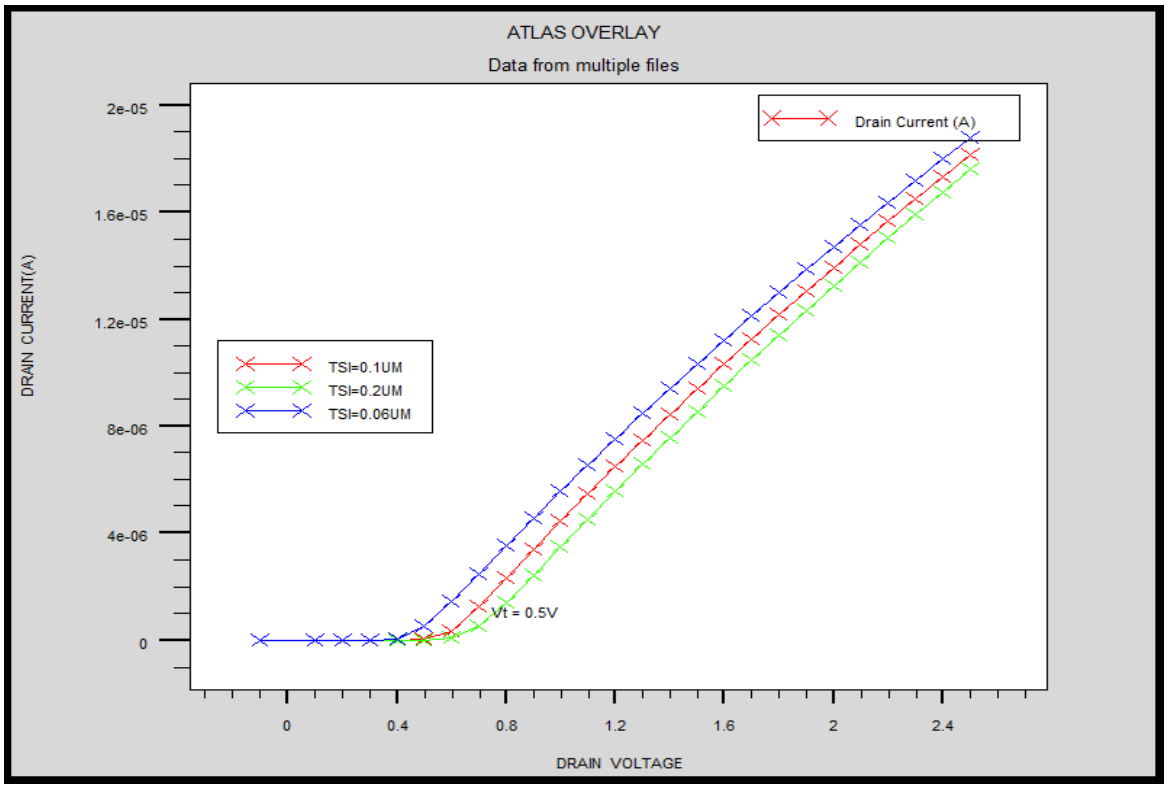


Figure 3-13: Transfer characteristics at different silicon film thickness at Tsi,Ttox=0.017um, Tbox=0.4um

Figure 3-13 illustrates that drain current increases with the increase in the thickness of the silicon film, but after a certain limit of Tsi, when its thickness is greater than 0.2 μm, where threshold voltage remains the same and is insensitive to the thin-film thickness since the depletion region is independent of this film thickness.

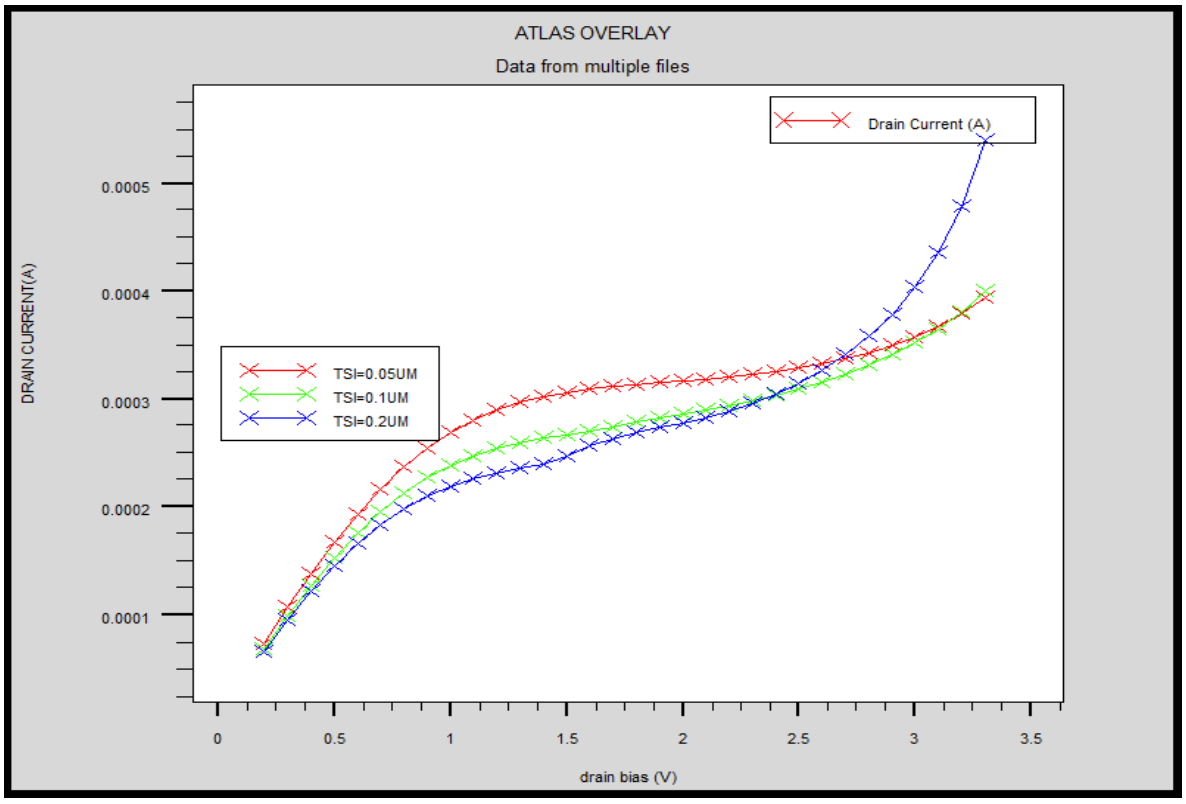


Figure 3-14: Output characteristics at different silicon film thickness at Tsi, Ttox=0.017um, Tbox=0.4um

If we illustrates figure 3-14, we can observe that for a significant Tsi, (Tsi>0.2µm), the depletion zone under the conducting channel does not extend sufficiently in-depth to reach buried oxide. It can be said as PDSOI MOSFET(partially depleted mosfet) .This effect appears in IDS-VDS characteristics by the emergence of a**" kink**. "

For n channel and Tsi>0.2um above a certain value of VDS voltage the kink appears essentially at room temperature."Kink effect" is not observed in bulk devices when substrate or well connections are provided, however kink effect can be observed in bulk MOSFET's operating at low temperatures.

Kink effect is one of the principal effects of the floating substrate, started by the accumulation of carriers produced by impact ionization in the silicon film. This effect is translated in transistors where Tsi>0.2um and by the increase of drain current and an electric noise in its saturation region. When we reduce silicon film thickness, this

depletion layer reach the BOX, It can be said as Fully Depleted SOI MOSFET “FDSOI”. It is observe that the kink effect does not appear for

Tsi<0.2um on IDS-VDS characteristics. It is also important to notice that a thin silicon film allows a better electrostatic control of the gate on the channel leading to threshold voltage reduction.

3.4.2: Influence of Tox variation on ID current:

Scaling oxide thickness is desirable for better drain current. In practical it is consider to the impact of Tox thickness on the device performance.

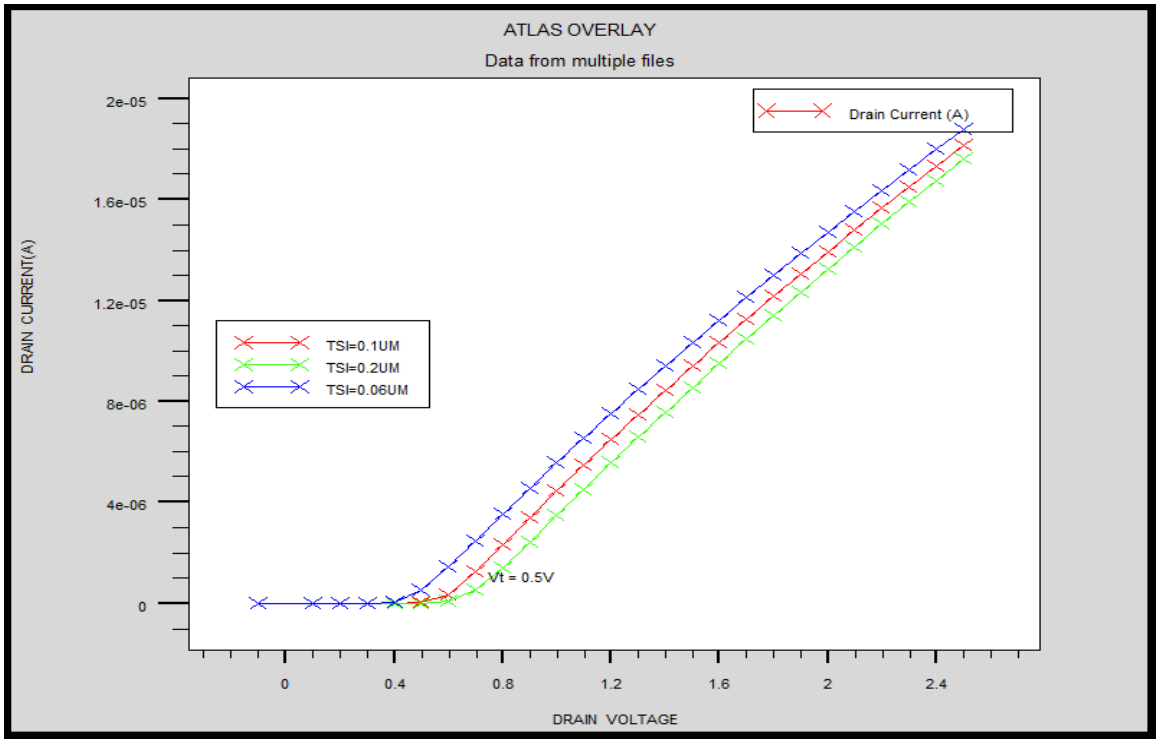


Figure 3-15: Transfer characteristics curve at various Tox,Tbox=0.4um,Tsi=0.1um,vds=0.5v

Figure 3-15 illustrates transfer characteristics for a (Tsi=0.1µm) at different oxide thickness. We can observe that drain current decrease for lower oxide thickness. Indeed, oxide thickness decreasing leads to Cox increasing and consequently to drain current

decreasing, We can then conclude that gate oxide thickness has a very big effect on the drain current

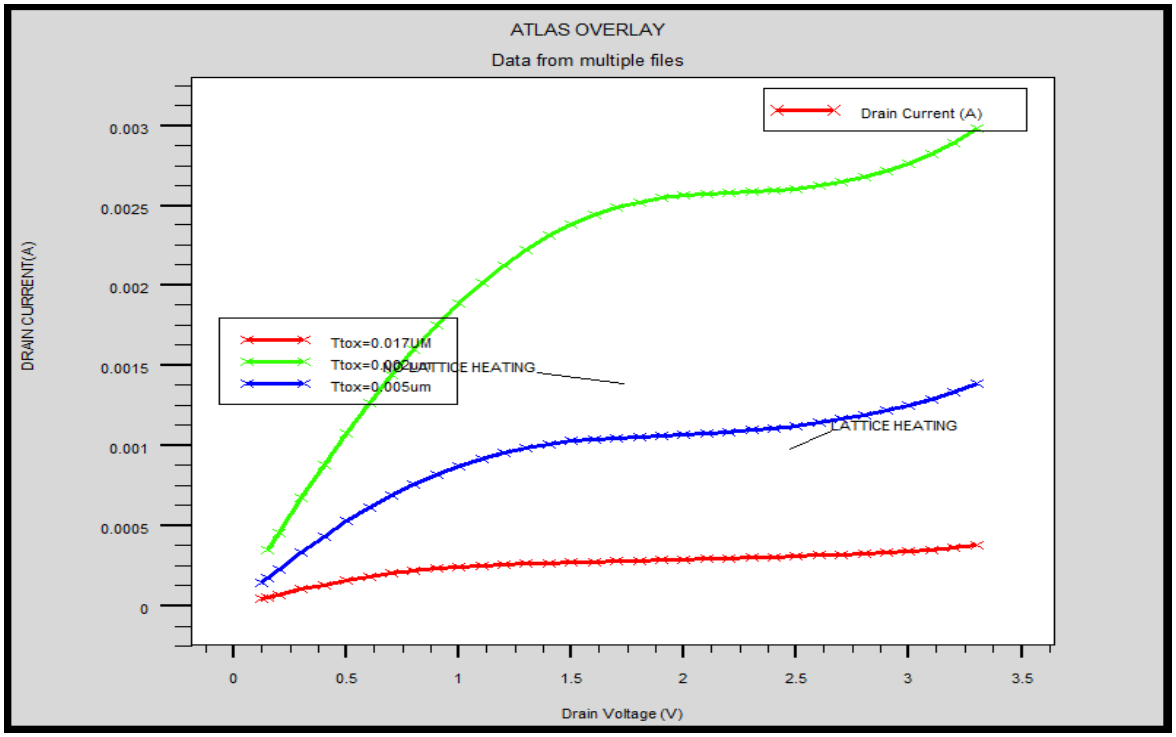


Figure 3-16: Output characteristics curve at various Tox, Tbox=0.4um,Tsi=0.1um,Vds=0.5v

At shorter oxide thickness, the drain saturation current increases strongly. We can conclude for this variation that thinner gate oxides lead to product higher drain currents and transconductances, and a better pinch-off behavior. Consequently it is recommended to choose the lowest possible oxide thickness.

Again we notice that lattice heating occurs as the oxide thickness increases. The range between .005um to .017um lattice heating occurs. Again, it is recommended that the lower the oxide thickness the better the transfer characteristics curve.

3.4.3: Influence of channel length on ID current:

This section deals with the study of gate length variation effect on the electrical device characteristics.

In order to achieve this task, the channel length transistor was held constant. however the gate length covers part or the entire channel.

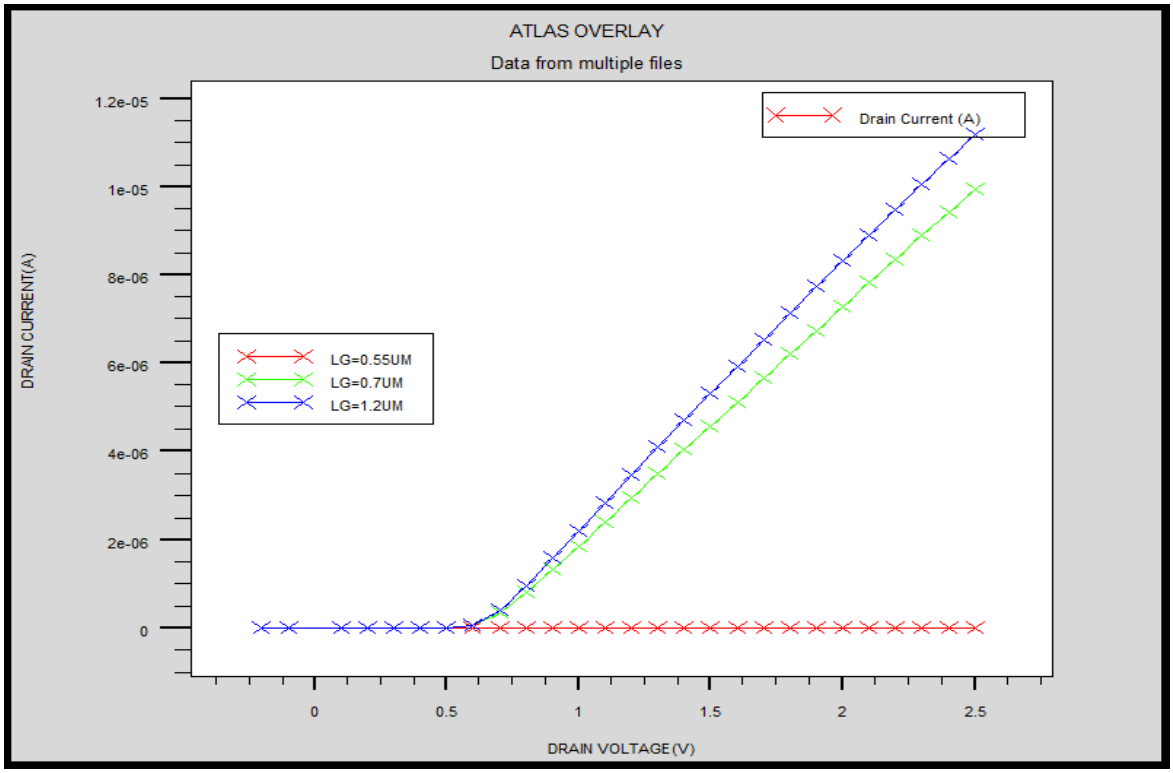


Figure 3-17:Transfer characteristics curve on different gate length

Figure 3-17 illustrates that when the gate length,Lg=0.55um no drain current occurs. So it can be said that at Lg=0.55um there is no drain current..

When the gate length increases, at Lg=0.7um and Lg=1.2um the drain current characteristics slope increase. Therefore the transistor transconductance increases .At shorter gate lengths a threshold voltage roll off can be observed. In fact we can conclude that gate length must be chosen wisely because the gate loss its control on the channel when Lgate is less significant than Lchannel.

3.4.4 Influence of doping on ID current:

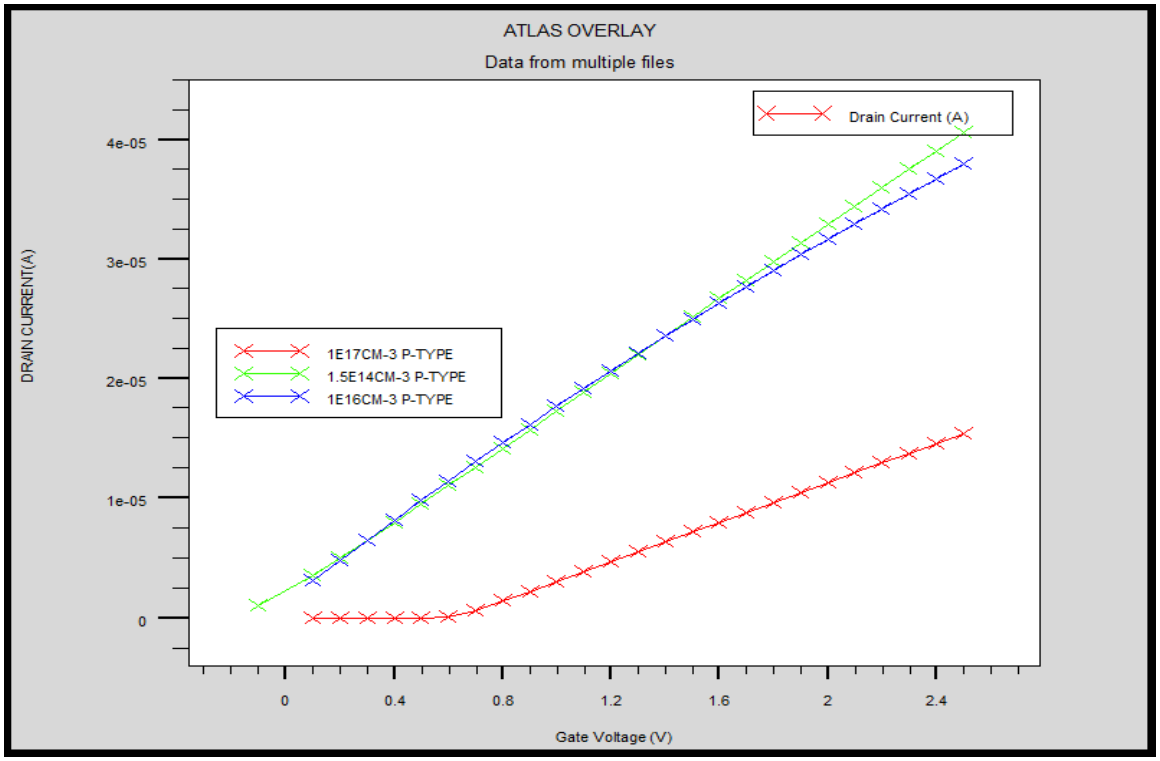


Figure 3-18: Transfer characteristics curve on different doping

Figure 3-18 illustrates that with the decrease of the doping of p-type drain current increases. When the doping is 1e17 p type at first the drain current is zero. When the gate voltage is 0.6v the drain current increases slowly.

But when the doping is 1.5e14 to 1e16 ptype the drain currents have a sharp rise. lowering the subtrate doping concentration resulted in a better saturation region and higher current drive. Lower subtrate doping concentration provides better mobility and hence, less velocity saturation.

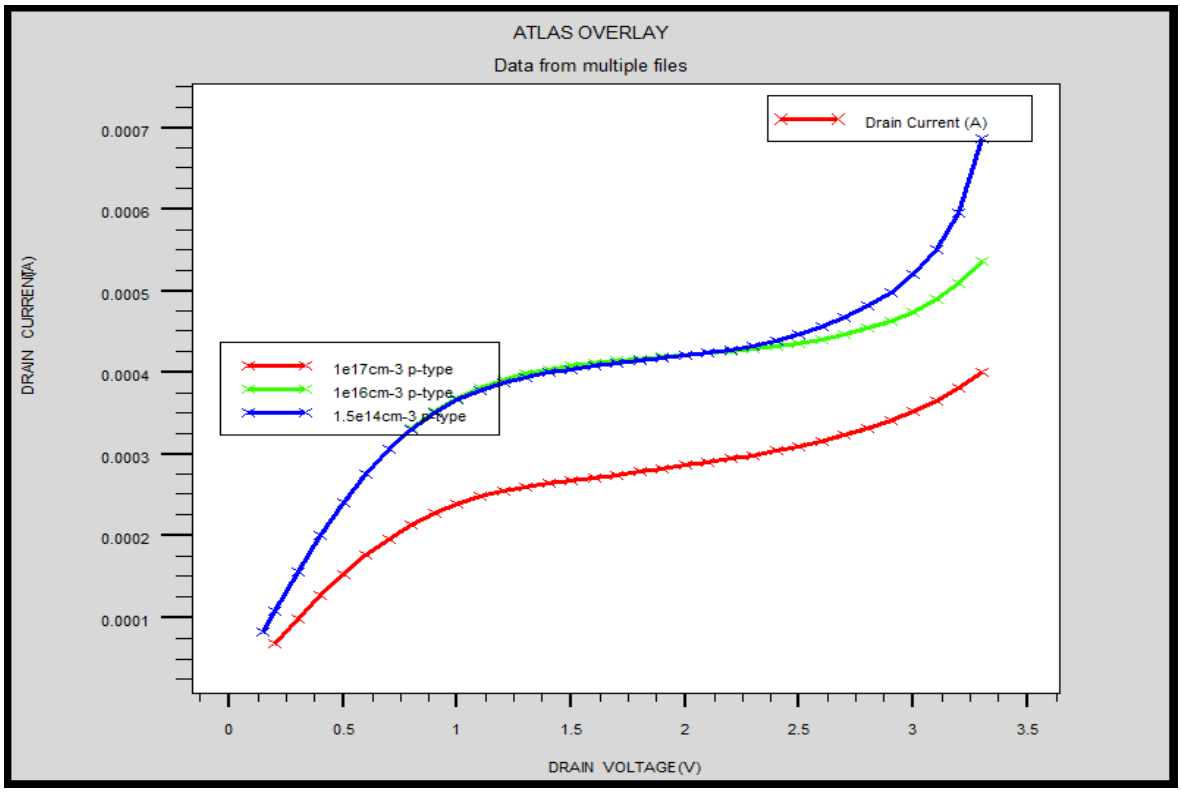


Figure 3-19: output characteristics curve at different doping

Reduction of the channel doping concentration Which improve the saturation region of the IDVD curves and reduces threshold voltage.

Chapter 4

Conclusion and Future scope

4.1 Conclusion

4.2 Recommendation for future work

4.1.Conclusion:

The scaling down of planar bulk MOSFETs according to the International Technology Roadmap for Semiconductors ITRS requires new structures such as SOI MOSFETs. These structures allow reducing short channel effects that appears under 50nm node. In order to conceive these new structures numerical devices simulations are required. We do simulation with SILVACO using ATLAS by changing the various parameter.

Effective ways to improve the degraded electrical characteristic.

1. Thinning the silicon film allows a better electrostatic control of the gate on the channel leading to threshold voltage reduction. This will reduce the kink

2. Thinner gate oxides lead to product higher drain currents and transconductances, and a better pinch-off behavior.

3. Increasing the gate length , the drain current characteristics slope increase to, and therefore the transistor transconductance increased.

4. Lower subtrate doping concentration provides better mobility and hence, less velocity saturation

4.2. Recommendation for Future scope:

Partially Depleted SOI technologies are increasingly being implemented for use in high-performance CMOS applications. High-performance applications (e.g., Microprocessors) need ever-improving MOSFET performance. However, as MOSFETs are scaled down into the sub-50nm regime, it is becoming increasingly difficult to meet the twin challenges of (a) improving performance, while (b) containing power dissipation.

PD/SOI MOSFETs are good candidates for offering a better trade-off between power and performance. This is due to their low junction capacitance as well as potentially beneficial floating-body effects that can be exploited in circuit design. They are also relatively friendly to implement in a high-performance CMOS manufacturing environment. There are, however, key areas where special attention is needed.