PERFORMANCE ANALYSIS OF THIN FILM TANDEM SOLAR CELL USING DIFFERENT MATERIALS AND MAXIMIZING EFFICIENCY OF SOLAR PANEL BY SOLAR TRACKING USING FPGA

The thesis submitted in partial fulfillment of the requirements for the degree of

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APPROVAL

The undersigned certify that he has read and recommended for acceptance, a thesis entitled **"PERFORMANCE ANALYSIS OF THIN FILM TANDEM SOLAR CELL USING DIFFERENT MATERIALS AND MAXIMIZING EFFICIENCY OF SOLAR PANEL BY SOLAR TRACKING USING FPGA "** in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical, Electronic and Communication Engineering.

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DECLARATION

It is hereby declared that this thesis titled **"PERFORMANCE ANALYSIS OF THIN FILM TANDEM SOLAR CELL USING DIFFERENT MATERIALS AND MAXIMIZING EFFICIENCY OF SOLAR PANEL BY SOLAR TRACKING USING FPGA"** or any part of it has not been submitted elsewhere for the award of any degree or diploma.

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DEDICATED

TO

OUR BELOVED PARENTS

AND

MIST

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ABSTRACT

This treatise has focused on the resolution of thin film photovoltaic cells and solar power efficiency. During schooling, elementary knowledge about various types of thin film terminology and their device structure and working principle have been attained. Despite remarkable progress in all perspectives of production of crystalline silicon based PV cells, the cost of production and installment is still much higher. This can be attenuated by the use of microstructure and tandem thin film PV cells and proper installation methods and initiatives.

In fine, simulations of thin film tandem solar cell, tandem CIGS solar cell and proposed tandem silicon solar cell with pyramids design have been done along with a comparison of various output parameters; fill factor and energy conversion efficiency.

Ultimately, the dual-axis solar tracker has been made to meet the ever increasing demand of high solar power efficiency by using FPGA and Verilog. This project will unveil a whole new horizon due to use of FPGA.

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LIST OF ABBREVIATION

AM	-	Air Mass
ASIC	-	Application Specific Integrated Circuit
AADAT	-	Azimuth Altitude Dual Axis Tracker
CIGS	-	Copper Indium Gallium Selenide
CAD	-	Computer Aided Design
DSP	-	Digital Signal Processing
DCM	-	Digital Clock Manager
DSSC	-	Dye-Sensitized Solar Cell
EHP	-	Electron Hole Pair
FF	-	Fill Factor
FDTD	-	Finite Difference Time Domain
FPGA	-	Field Programmable Gate Array
HDL	-	Hardware Description Language
HSAT	-	Horizontal Single Axis Tracker
IC	-	Integrated Circuit
MMI	-	Monolithic Memories Incorporated
MAC	-	Multiply and Accumulate
PV	-	Photo Voltaic
PCB	-	Printed Circuit Board
PLA	-	Programmable Logic Array

PROM	-	Programmable Read Only Memory
PWM	-	Pulse Width Modulation
PASAT	-	Polar Aligned Single Axis Tracker
ROM	-	Read Only Memory
TF	-	Thin Film
TFPV	-	Thin Film Photo Voltaic
TCO	-	Transparent Conducting Oxide
TSAT	-	Tilted Single Axis Tracker
TTDAT	-	Tip-Tilt Dual Axis Tracker
VSAT	-	Vertical Single Axis Tracker

CHAPTER 1

INTRODUCTION

1.1. Introduction

Renewable energy solutions are becoming increasingly popular. Photovoltaic (solar) systems are but one example. Maximizing power output from a solar system is desirable to increase efficiency. In the world of photovoltaics, dozens, if not hundreds, of different materials and architectures have been investigated which range from inorganic single-crystal single junctions to solution-processed organic tandem cells to hybrid organic/inorganic devices. More than fifty years after the first report of cells based on crystalline silicon p-n junction, this structure still represents more than 90% of the market. It is indeed a mature technology, which developed in parallel to the microelectronics industry. It has reasonable power conversion efficiencies, its stability is good ,most importantly, its energy payback time, i.e., the required operation time for an installation to produce the amount of energy used during its production, is small (about two years) as compared to its lifetime. But in short, crystalline silicon is too expensive. That is why, in spite of unique growth rates (between 30% and 40% per year for years), the contribution by photo voltaics to the global energy mix is still negligible. Thin film PV cells are promising approach and it has tremendous potential. The thinness of the cell is the defining characteristic of the technology. Unlike silicon-wafer cells, which have light-absorbing layers that are traditionally 350 microns thick, thin-film solar cells have light-absorbing layers that are just one micron thick. There are three main types of inorganic thin-film solar cells, depending on the type of semiconductor used:

Amorphous Silicon (a-Si), Cadmium Telluride (CdTe) and Copper Indium Gallium Selenide (CIGS).Amorphous silicon is the most developed of the complex thin film technologies. In its simplest form, the cell structure has a single sequence of p-i-n layers. Such cells suffer from significant degradation in their power output when exposed to the sun. Thinner layers can be used to increase the electric field strength across the material and to provide better stability. However, the use of thinner layers

reduces light absorption, and hence cell efficiency. But this can be significantly improved by using multi-layer absorber i.e. multi-junction thin film solar cells. In fact, until now, highest recorded efficiency has been achieved using this technology with concentrators.

Field programmable Gate Arrays (FPGAs) are prefabricated silicon devices that can be electrically programmed in the field to become almost any kind of digital circuit or system. For low to medium volume productions, FPGAs provide cheaper solution and faster time to market as compared to Application Specific Integrated Circuits (ASIC) which normally require a lot of resources in terms of time and money to obtain first device. FPGAs on the other hand take less than a minute to configure and they cost anywhere around a few hundred dollars to a few thousand dollars. Also for varying requirements, a portion of FPGA can be partially reconfigured while the rest of an FPGA is still running. Any future updates in the final product can be easily upgraded by simply downloading a new application bit stream. However, the main advantage of FPGAs i.e. flexibility is also the major cause of its draw back. Flexible nature of FPGAs makes them significantly larger, slower, and more power consuming than their ASIC counterparts. These disadvantages arise largely because of the programmable routing interconnect of FPGAs which comprises of almost 90% of total area of FPGAs. But despite these disadvantages, FPGAs present a compelling alternative for digital system implementation due to their less time to market and low volume cost.

A single FPGA can replace thousands of discrete components by incorporating millions of logic gates in a single integrated circuit (IC) chip. The software flow (CAD flow) takes an application design description in a Hardware Description Language (HDL) and converts it to a stream of bits that is eventually programmed on the FPGA. Unlike processors, FPGAs use dedicated hardware for processing logic and do not have an operating system. FPGAs are truly parallel in nature so different processing operations do not have to compete for the same resources. As a result, the performance of one part of the application is not affected when additional processing is added. Also, multiple control loops can run on a single FPGA device at different rates. FPGA-based control systems can enforce critical interlock logic and can be designed

to prevent I/O forcing by an operator. However, unlike hard-wired printed circuit board (PCB) designs which have fixed hardware resources, FPGA-based systems can literally rewire their internal circuitry to allow reconfiguration after the control system is deployed to the field. FPGA devices deliver the performance and reliability of dedicated hardware circuitry.

1.2. Background

1.2.1. Early History of PV Cell

Forty years after Edmund Bequerel discovered the photovoltaic effect from the immersed platinum in electrolytes, William Adams and Richard Day observed the photovoltaic effect in a sample of selenium placed between two metal electrodes. This was the first solid photovoltaic device. The photovoltaic effect in this device originates from the association of selenium and metal. Twenty years later, Charles Fritts developed the first large-area photovoltaic device. Each of these early cells was comprised of a metal electrode/ semi-conductor/ semitransparent thin metal electrode with a bottle neck to transmit incident light. Due to this limitation, the resulting power conversion efficiency was limited to less than 1%.

In 1954, Bell Labs revealed the first high-power silicon PV cell, which used a p-n junction and reported a efficiency of 6%.In the 1970s, research into tandem cell structures and bandgap tuning of semiconducting materials was conducted to improve power conversion efficiency.

Carlson and Wronski announced the first experimental a-Si:H solar cell made at RCA. Laboratory in 1976 which had an energy conversion efficiency of 2.4%. Since then , this technology has improved tremendously and today, it is considered as a matured thin film solar cell technology.

1.2.2. Early History of FPGA

The origins of the contemporary Field-Programmable Gate Array are tied to the development of the integrated circuit in the early 1960s. Early programmable devices employed architectural regularity and functional flexibility. Cellular arrays typically consisted of a two-dimensional array of simple logic cells with fixed, point-to-point communication. These first arrays contained logic cells which could be programmed via metalization during manufacturing to implement a range of two-input logic functions. By the mid-1960s, field-programmability, the ability to change the logic function of a chip after the fabrication process, was achieved via the introduction of "cutpoint" cellular arrays. Although the connections between the elements of the array were fixed, the functionality of each logic cell in the array could be determined by setting programmable fuses. These fuses could be programmed in the field through the use of programming currents or photo-conductive exposure. [1] As a result, field-customization allowed for simplified array manufacturing and wider applicability.

In the 1970s, a series of read-only memory (ROM)-based programmable devices were introduced and provided a new way to implement logic functions. Although mask-programmable ROMs and fuse-programmable ROMs (PROMs) with N address inputs can implement any N-input logic function, area efficiency quickly becomes an issue for all but small values of N due to the exponential dependence of area on N. The first programmable logic arrays (PLAs) improved on this with two-level AND–OR logic planes (each plane in a wired-AND or wired-OR structure along with inverters can build any 'AND' or 'OR' logic term) that closely match the structure of common logic functions and are significantly more area-efficient. An example PLA is shown in Figure 1.1 (a).

These architectures evolved further with the realization that sufficient flexibility was provided by a programmable AND plane followed by a fixed OR plane, in the programmable array logic (PAL) devices that were introduced in 1977 by Monolithic Memories Incorporated (MMI) As shown in Figure 1.1(b), it is notable that these devices contained programmable combinational logic which fed fixed sequential logic in the form of D-type flip–flop macro cells. With these devices, logic functions must be implemented using one or more levels of two-level logic structures.

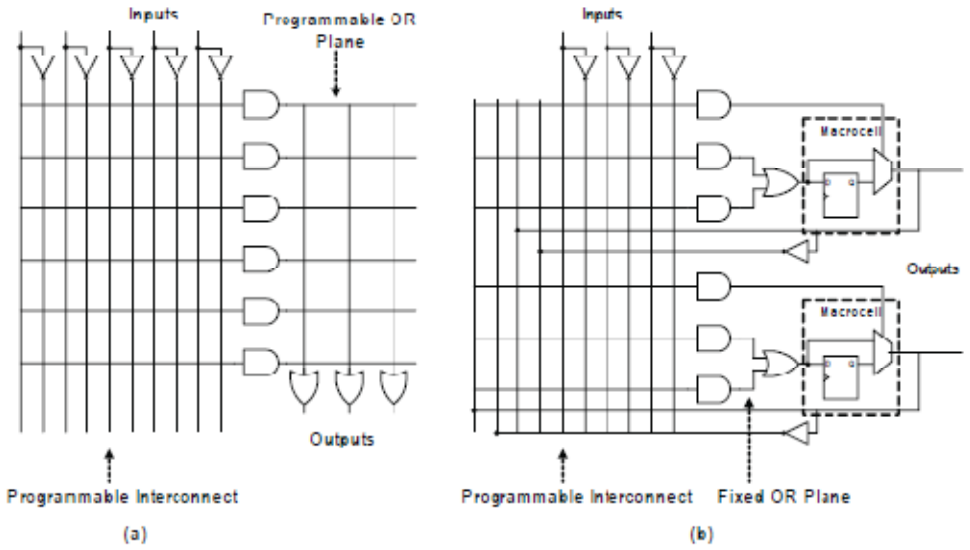


Figure1.1: PLA and PAL architectures.[1]

Device inputs and intermediate combinational sums are fed into the array via a programmable interconnect that is typically a full cross-bar, leading to significant interconnect costs for this programmable architecture. For data path and multi-level circuits, the area costs of two-level implementation quickly become prohibitive.

The first static memory-based FPGA (commonly called an SRAM based FPGA) was proposed by Wahlstrom in 1967. This architecture allowed for both logic and interconnection configuration using a stream of configuration bits. Unlike its contemporary cellular array counterparts, both wide-input logic functions and storage elements could be implemented in each logic cell. Additionally, the programmable inter-cell connections could be easily changed (through memory-configurability) to enable the implementation of a variety of circuit topologies. Although static memory offers the most flexible approach to device programmability, it requires a significant increase in area per programmable switch compared to ROM implementations. It is likely this issue delayed the introduction of commercial static memory-based programmable devices until the mid 1980's, when the cost per transistor was sufficiently lowered.

The first modern-era FPGA was introduced by Xilinx in 1984.It contained the now classic array of Configurable Logic Blocks. From that first FPGA which contained 64

logic blocks and 58 inputs and outputs, FPGAs have grown enormously in complexity. Modern FPGAs now can contain approximately 330,000 equivalent logic blocks and around 1100 inputs and outputs in addition to a large number of more specialized blocks that have greatly expanded the capabilities of FPGAs. These massive increases in capabilities have been accompanied by significant architectural changes that will be described in the remainder of this survey.

1.3. Objective of the Thesis

The objective of this thesis is to study and analyze the performance of multi-junction thin film solar cell using different materials. For handling these, fundamental semiconductor equations like Poisson's equation, Schrodinger's equation, Carrier continuity equation, Drift-Diffusion Transport Model, Fermi-Dirac Statistics and Boltzmann statistics, etc have been studied along with physical models for light propagation, optical intensity profiles etc. ATLAS simulation software provided by SILVACO has been used for modeling the PV Cell devices.

A detailed analysis of material properties of different materials and their optoelectronic properties has been performed and from the above analysis, an optimized tandem Silicon solar cell with pyramids structure has been proposed. After that simulation has been performed by ATLAS, outputs like short-circuit current density (Jsc), open circuit voltage (Voc), maximum power (Pm), maximum output voltage (Vm), maximum output current (Im), fill factor(FF) and efficiency for multi-junction thin film photo voltaic cells of different Materials have been extracted and compared for observation and analysis.

The main object of this dual-axis solar tracker project is to increase the efficiency of the solar power that we receive from the sunlight. Solar tracker is not a very new topic of course, but it has been tried to take the system to a whole new level by implementing the system using Field Programmable Gate Arrays (FPGA). The system has been implemented by using Verilog hardware description language. Previously

this kind of tracker had been made by using microcontroller. Though using FPGA will add some more complexity to the system but it will be also become capable of taking out the advantages of the FPGA. One of the major advantages of FPGA is parallel processing. FPGAs could contain a multitude of things at the same time. The bigger ones can even have two Power PC microprocessors running at the same time in the same FPGA.

1.4. Layout of the thesis

This thesis includes eight chapters.

Chapter one is the introduction which includes a brief idea, short history and a brief objective of the thesis.

Chapter two describes basic theory of light and semiconductor Physics with necessary definitions, equations and figures.

In chapter three, in brief fundamental working principle and characteristics of photovoltaic devices have been discussed.

Chapter four describes material properties and structure of thin film solar cell, tandem solar cell, its working principle, material properties and advantages over other technologies.

Chapter five is all about simulation and analysis . It also includes the proposed tandem Silicon solar cell with pyramids structure.

In chapter six, Solar Tracker has been discussed.

In chapter seven, FPGA has been discussed.

Conclusions are in chapter eight. Suggestions for future works are also provided here.

CHAPTER 2

BASIC THEORY OF LIGHT AND SEMICONDUCTOR PHYSICS

2.1. Basic of Light's Wave Nature

2.1.1. Schrodinger Equation

When the quantum confinement is in one dimension(along Y-axis),the calculation of quantum electron density relies upon a solution of a one dimensional schrodinger equation solved for Eigen state energies $E_{iv}(x)$ and wave function Ψ_{iv} (x,y) at each slice perpendicular to the X -axis and each electron valley (or hole band)v.[2]

$$-\frac{\pi^2}{2}\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(\mathrm{x,y})}\quad\frac{\partial\Psi_{iv}}{\partial y}\quad\right)+E_C(\mathrm{x,y})\Psi_{iv}=E_{iv}\Psi_{iv}$$

Here, Here, m_y^v(x,y)is a spatially dependent effective mass in Y direction for the v-th valley and E_c(x,y) is conduction band edge. The equation for holes is obtained by substituting hole effective masses instead of electron ones and valance band edge - E_v(x,y) instead of E_c(x,y).

Two dimensional Schrodinger Equation reads:

$$-\frac{\pi^2}{2}\left[\frac{\partial}{\partial x}\left(\frac{1}{m_x^v(\mathrm{x,y})}\quad\frac{\partial\Psi_{iv}}{\partial x}\quad\right)+\frac{\partial}{\partial y}\left(\frac{1}{m_y^v(\mathrm{x,y})}\quad\frac{\partial\Psi_{iv}}{\partial y}\quad\right)\right]+E_C(\mathrm{x,y})\Psi_{iv}=E_{iv}\Psi_{iv}$$

2.1.2. Reflection and Transmission

Figure 2.1 shows the relationship between the angles of incidence(θ_i), reflection(θ_r) and transmission (θ_t)at the interface between two media . [3]

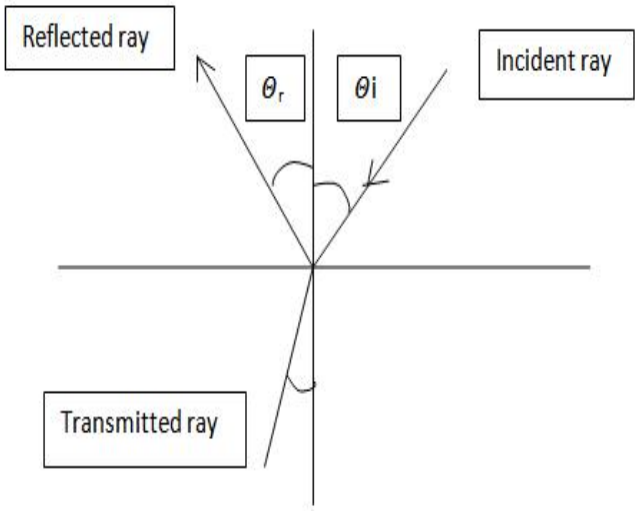


Figure 2.1: Angles of Incidence, Reflection and Transmission.

2.1.3. Light Absorption and Photo Generation

The cumulative effects of the reflection coefficient, transmission coefficient and the integrated loss due to adsorption over the ray path are saved for each ray. The generation associated with each grid point can be calculated by integration of the Generation Rate Formula over the area of intersection between the ray and the polygon associated with the grid point.[3]

$$G = \eta_0 \frac{P\lambda}{hc} \alpha e^{-\alpha y}$$

Here,

a) P is the ray intensity factor which contains the cumulative effects of reflections, transmissions and loss due to absorption over the ray path.

b)η_0 is the thermal quantum efficiency which represents the number of carrier pairs generated per photon observed.

c) y is the relative distance for ray.

d) h is the plank's constant.

e) c is the speed of light

f) α is the absorption coefficient given by the following equation:

$$\alpha = \frac{4\pi}{\lambda} \mathrm{k}$$

Where k is imaginary part of the optical index of refraction.

2.1.4. Physical Models for Light Propagation

The propagation of light can be described by any one of three physical models. The physical models for light propagation include the followings:

a) Characteristic Matrix (Transfer Matrix) Method:

First, the characteristics matrix of a single layer is described.[4] The matrix relates tangential components of the electric E(z)and magnetic H(z) fields at the layer boundaries z=0 and z=d.

$$\begin{pmatrix} E(0) \\ H(0) \end{pmatrix} = M \begin{pmatrix} E(d) \\ H(d) \end{pmatrix}$$

The Matrix itself is

$$\mathrm{M} = \begin{bmatrix} \cos\phi & j\sin\phi/Y \\ jY\sin\phi & \cos\phi \end{bmatrix}$$

$$\phi = \frac{2\pi}{\lambda} \mathrm{nd}\cos\theta$$

Where ϕ is the phase shift for the wave propagating through the layer, n is the complex refractive index , θ is the angle of propagation in the layer, Y is the optical admittance of the layer which is parallel and perpendicular polarizations is given by

$$Y^{(s)} = \sqrt{\frac{\epsilon_0}{\mu_0}} \mathrm{n}\cos\theta$$

$$Y^{(p)} = \sqrt{\frac{\epsilon_0}{\mu_0}} \frac{n}{\cos\theta}$$

Where ϵ_0 and μ_0 are permittivity and permeability of free space.

b) Finite Difference Time Domain Analysis:

The Finite Difference Time Domain (FDTD) Method can be used to model optical inter-actions between a directed optical source and a semiconductor device in much the same way as in geometric ray tracing. The difference is that the FDTD solves for the electric and magnetic field propagation directly from the fundamental wave equations. The FDTD approach correctly models the wave propagation with reflection, diffraction and interference effects at relatively high computational expense.[5]

c) Beam Propagation Method in Time Dimension:

Most optoelectronic devices can be simulated using ray tracing based on geometrical op-tic principles. But when diffraction or coherent effects are important, ray tracing methods are no longer sufficient. In this case, a method is needed that takes into account the wave nature of light.[6]

A method that does this called the Beam Propagation Method (BPM). BPM has been extended to solve a more general Helmholtz Wave Equation. The Helmholtz Wave Equation is consistent with the Rayleigh-Sommerfeld Formulation of scalar diffraction and isotropic media and neglecting non- linear effects.

These assumption put certain restrictions on the applicability of BPM. For example, material regions with gradual change in refractive index or photo detector saturation modeling are not supported.

2.2. Basic Semiconductor Physics

2.2.1. Poisson's Equation

Poison's Equation related electrostatic potential to space charge density :

$$\Delta^2 \phi = \frac{\rho f}{\epsilon}$$

Where, ϕ is the electrostatic potential, ϵ is the permittivity, ρ_{f} is the local space charge density. the local space charge density is the sum of contributions from all mobile and fixed

charges, including electrons, holes, and ionized impurities.[7]

The electric field is obtained from the gradient of the potential :

$$E = -\nabla\phi$$

2.2.2. Fermi-Dirac and Boltzmann Statistics

Electron in thermal equilibrium at temperature T_L with a semiconductor lattice obey Fermi-Dirac statistics. That is the probability f(ϵ) that an available electron state with energy is occupied by an electron is :

$$f(\epsilon) = \frac{1}{1+exp(\frac{\epsilon - E_F}{kT})}$$

Where E_F is a spatially independent reference energy known as the Fermi level and k is Boltzmann's constant.[8]

In the limit , $\epsilon - E_F >> k\,T_L$ above equation can be approximated as :

$$f(\epsilon) = exp(\frac{E_F - \epsilon}{kT})$$

2.2.3. Effective Density of States

Integrating the Fermi-Dirac statistics over a parabolic density of states in the conduction and valence bands, whose energy minimum is located at energies E_C and E_V respectively yields the following expressions for the electron and hole concentration:

$$n = N_C \exp(\frac{E_F - E_C}{kT}) \quad (2.1)$$

$$p = N_V exp(\frac{E_V - E_F}{kT}) \quad (2.2)$$

Which are referred as the Boltzmann approximations.[9]

2.2.4. Intrinsic Carrier Concentration

Multiplying equation 2.1 with equation 2.2

$$np = n_{ie}^2$$

Where , n_{ie} is the intrinsic carrier concentration and is given for Boltzmann statistics by

$$n_{ie}=\sqrt{N_C N_V}\exp(-\frac{E_g}{2kT})$$

$E_g = E_C - E_V$=Bandgap Energy

For intrinsic (undoped) materials, p=n. By equating equations 2.1 and 2.2 and solving for yields:

$$E_F=E_i=-q\Psi_i=\frac{E_C-E_V}{2}+(\frac{kT}{2})\ln(\frac{N_V}{N_C})$$

Where, E_i is the Fermi level for intrinsic silicon and Ψ_i is the intrinsic potentials. Above equation also defines the intrinsic potential under non-equilibrium conditions[9] The electron and hole concentrations can be expressed in terms of the intrinsic carrier concentration as:

$$n = n_{ie}\, exp(\frac{q(\Psi-\phi_n)}{kT})$$

$$p = n_{ie}\, exp(\frac{q(\Psi-\phi_p)}{kT})$$

Where, Ψ is the intrinsic potential and ϕ is the potential corresponding to the Ferm level.

2.2.5. Criterion of EHP Generation

When a light of photon energy hν impact on the film at which hν > E_g , the energy of this photon will be absorbed by the valance band electron of the intrinsic silicon and a sufficient energy creates an electron in the conduction band and a hole in the valance band. That means EHP is created.[10]When this EHP is created there is a criterion of Quasi Fermi level on the n^+ and p^+ region. Because the Fermi level is no longer

constant in every region after illumination, due to excess minority carrier.

Excess carriers generated in the intrinsic region are separated by electric field and this electric field will create drift current. There is also a diffusion current component.

For intrinsic region:

Case 1:

Before illumination or at thermal equilibrium

$$n_0 = p_0 = n_i$$

Where, n_i is the intrinsic carrier concentration.

$$n_i = \sqrt{N_C N_V exp(-\frac{E_g}{2kT})}$$

After illumination

$$n = n_0 + \delta_n$$

$$p = p_0 + \delta_p$$

$\delta_n \; and \; \delta_p$ are created for EHP Where, $\delta_n = \delta_p$

2.2.6. Consideration of Excess Carrier Recombination

An external excitation, such as light or flux of photon can generate EHP there have regeneration impact on the p-i-n semiconductor. In thermal equilibrium the generation rate = recombination rate.

$$g' = R'$$

Where, R' is the recombination rate.[11]

But when a ray of light incidents upon thin film, it is no longer in thermal equilibrium.

$$g' \neq R'$$

But when the light incident generates EHP, then electron and hole recombination occur in pair.

So, the recombination rate must be equal. Where, $R_n = R_p$

R_n= Recombination rate for excess electron.

R_p= Recombination rate for excess holes.

The rate at which electron recombine must be proportional to the electron concentration and must also be proportional to the hole concentration.

Low Level Injection:

Low level injection means that the excess carrier concentration is much less than the thermal equilibrium majority carrier concentration.[12]

High Level Injection:

High level injection means the excess carrier concentration is much greater than the thermal equilibrium carrier concentration.[12]

2.2.7. Band Gaps of Some Common Semiconductors Relative to the Optical Spectrum

We can observe that GaAs, Si, Ge and InSb lie outside the visible region and lie in the infrared region. Other semiconductors such as GaP and CdS are in the visible range.[13]

As discussed before, semiconductor absorbs photon when h is much higher than the band gap energy E_g. So, in infrared region material can absorb more variation of light.For example silicon absorbs light which has wavelength less than 1 m.

2.2.8. Consideration of Basic Parameters in Thin Film Analysis

The wave particle duality principle states that light wave cab be treated as particles which are referred as photon.[14]

The energy of a photon E = h ν. Where h= Plank's constant and ν = frequency of the wave.

$$E = \frac{hc}{\lambda} = \frac{1.24}{\lambda}$$

$$=> \lambda = \frac{1.24}{E(\mu m)}$$

Where, λ is the wave length.

This photon can interact with film impurity atom. Either donor or acceptor or both

interact with the defects of the semiconductor. The basic photon interaction process is of great interest in interaction with valance electron. When a photon collides with a valance electron enough energy may be imparted to elevate the electron in the conduction band. Such a process generates electron hole pair and creates excess carrier concentration.

2.2.9. Photon Absorption Coefficient

If the intensity of the photon flux is denoted by I(x) and its unit is energy/ cm^2 ,the following figure 2.2 shows an incident photon density at a position. The energy absorbed per unit time in distance dx is given by E = I(x)dx . Where is absorption coefficient and its unit is cm^{-1}.[14]

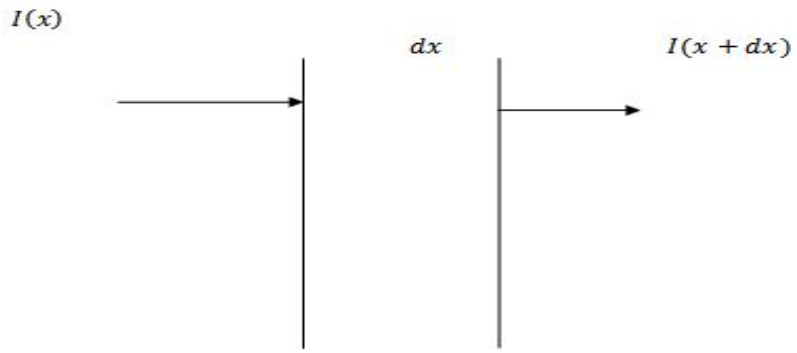


Figure 2.2: Optical Absorption in a Differential Length

So,

$$I(x + dx) - I(x) = \alpha I(x)dx$$

Here,

$$I(x + dx) < I(x)$$

So, $\frac{dI(x)}{dx} = -\alpha I(x)$

The solution of this equation is

$$I = I_0 \exp(-\alpha x)$$

I_0 is the intensity at distance at x =0

So, the distance of photon flux decreases exponentially with distance through the film. The absorption coefficient in semiconductor thin film is very strong function of photon energy and band gap energy.

Now, finding the effect of thickness of thin film and relation between absorption coefficient and thickness of the thin film.

As mentioned earlier $I = I_0 \exp(-\alpha x)$

If the thickness of the film is d, at distance d the intensity of the photon flux is

$$I = I_0 \exp(-\alpha d)$$

Or, $\frac{I}{I_0} = \exp(-\alpha d)$

Or, $\ln(\frac{I}{I_0}) = -\alpha d$

So, d is inversely proportional to the absorption coefficient.

For more sophisticated relationship between d and α :

$$d = \frac{1}{\alpha \ln(I/I_0)}$$

As the incident photon energy increases the absorption coefficient increases rapidly. So, photon energy can be totally absorbed in a very narrow region.

So, for higher of frequency of light the narrow thickness of thin film is capable absorbing all the energy. But it is not possible for low frequency.

2.2.10. Optical Generation Conditions for Electron Hole Pair Formation

When thin film is illuminated with light the photon may absorb or they propagate through film depending on photon energy and the band gap energy E_g.[15]

Conditions:

Case 1:

When $E = h\nu < E_g$

The photon energy is less than E_g, photon energy are not readily absorbed. In this case the light is transmitted through the material and film appears to be transparent.

Case 2:

When $E = h\nu > E_g$, the photon can interact with valance electron into conduction band. This interaction causes electron hole pair (EHP).

Figure 2.3 shows the optically generated electron hole pair formation in a Pseudo semiconductor.

When $h\nu > E_g$ an electron hole pair is created and the excess energy may give the electron or hole additional kinetic energy, which will be dissipated as heat in thin film.

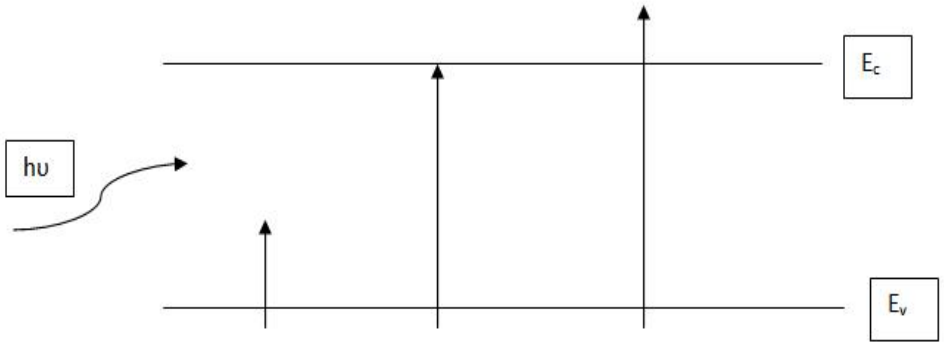


Figure 2.3: Optically Generated Electron Hole Pair Formation in a Pseudo Semiconductor. (Left to Right: $h\nu < E_g$, $h\nu = E_g$ and $h\nu > E_g$).

Consideration of Absorption Coefficient α in Two Situation:

If the absorption coefficient considered, two situations can come up. They are :

Case 1: α increases very rapidly for $h\nu > E_g$ or $\lambda < 1.24/E_g$.

Case 2: the absorption coefficient are very small for $h\nu < E_g$ or $\lambda > 1.24/E_g$.

In this situation film appears transparent to photon.

From these consideration it is concluded that high frequency light has high absorption coefficient for thin film and vice versa.

CHAPTER 3

PHOTO VOLTAIC DEVICES

3.1. Solar Energy Spectrum

Photo voltaic devices or solar cell converts incident solar energy into electrical energy. Incident photons are absorbed by the photo voltaic device material and charge carriers are generated. By passing these carriers through external circuit we get electricity. The intensity of radiation emitted from sun has a spectrum that resembles a black body radiation at temperature of about 6000K. Figure 3.1 shows the intensity spectrum of the sun under two different conditions above the earth's atmosphere and at the earth's surface.

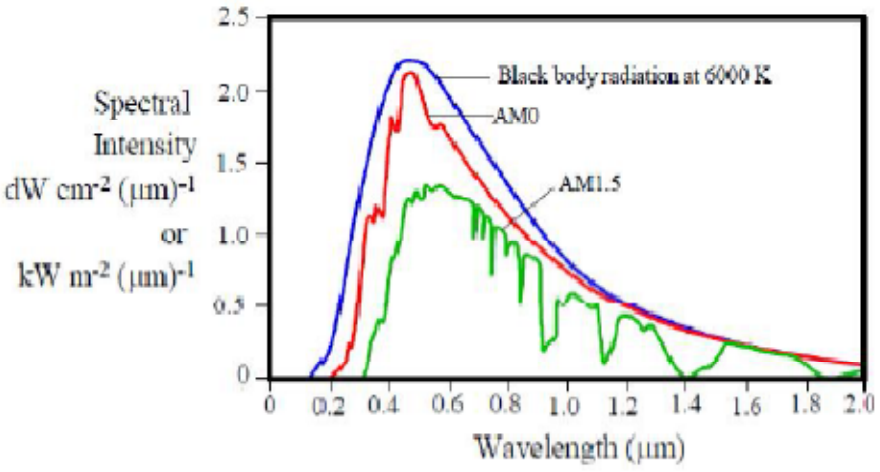


Figure 3.1: The Spectrum of Solar Energy Represented as Spectral Intensity Vs Wavelength Above Earth's Atmosphere (AM0) and at the Earth's Surface.[16]

Black body radiation at 6000K.

Fraunhofer absorption and temperature variation is typically representd by intensity per unit wavelength called spectral intensity I_λ so that $I_\lambda \delta\lambda$ is the intensity in a small interval $\delta\lambda$. Integration of I_λ over the whole spectrum gives rise the integrated or the total intensity, I.

3.2. Air Mass

The integrated intensity above Earth's atmosphere gives the total power flow through a unit area to the direction of the sun. This quantity is called the solar constant or air mass zero (AM0). The actual intensity spectrum on Earth's surface depends on the absorption and the scattering effects of the atmosphere and hence on atmospheric composition and the radiation path length through the atmosphere. Cloud increases the absorption and scattering of sun light and hence substantially reduce the incident intensity. On a clear sunny day the light intensity arriving on Earth's surface is roughly 70% of the intensity above the atmosphere. Absorption and scattering increase with the sun beam's path through the atmosphere. The shortest path through the atmosphere is when the sun directly above that location and received spectrum is called air mass one (AM1). All other angle incidence($\theta \neq 90$) increase the optical path through the atmosphere losses. Air mass m(AM m) is defined as the ratio of the actual radiation path h to the shortest path h_0.[17]

When h > h_0

$$\text{Air mass m (AM m)} = \frac{Actual\ Radiation\ Path, h}{Shortest\ Radiation\ Path\ , h_0}$$

Figure 3.2 shows the effect of the angle of incidence θ on the ray path length and the definition of AM0,AM1 and AM($\sec\theta$).

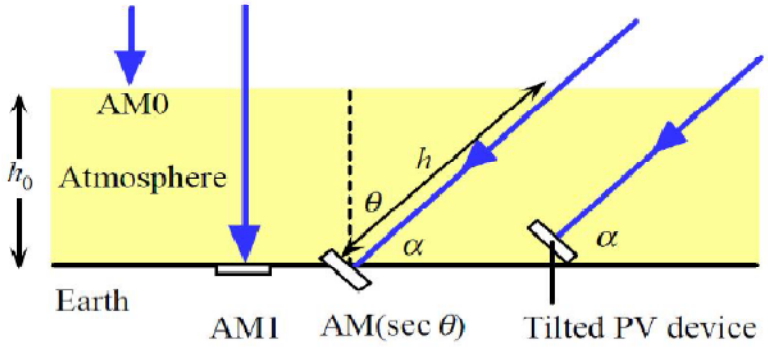


Figure 3.2: the effect of the angle of incidence θ on the ray path length and the definition of AM0, AM1 and AM(sec θ).

3.3. Photo Voltaic Device Principles

A simplified diagram of a typical solar cell is shown in Figure 3.3.

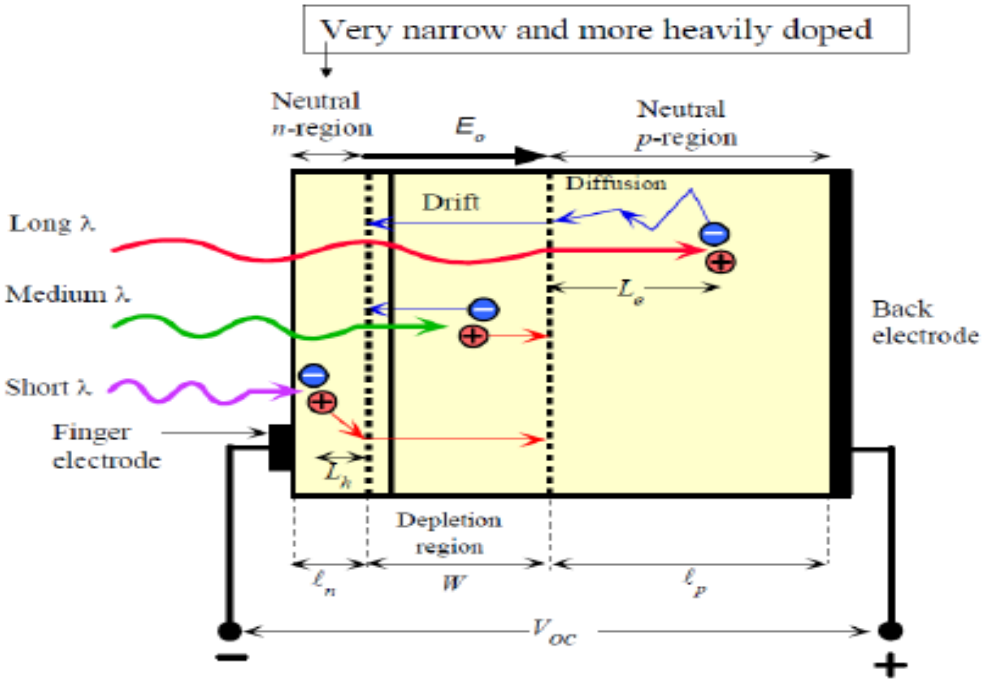


Figure 3.3: Principle of Operation of PV Cell

Consider a p-n junction with a very narrow and more heavily doped n-region. The illumination is through the thin n-side. The depletion region (W) or the space charge layer extends primarily into p-side. There is a build-in field E_0 in this depletion layer. The electrodes attached to the n-side must allow illustration to enter the device and at the same time result in a small series resistance. They are deposited on to n-side to form an array of finger electrodes on the surface. A thin antireflection coating on the surface reduces reflections and allows more light to enter the device.[18]

As the n-side is very narrow most of the photons are absorbed within the depletion region and within the neutral p-side (I_p) and photo generate electron–hole pair (EHPs) in these regions. The EHPs are immediately separated by the built-in field (E_0) which drifts them apart. The EHPs photo generated by long wavelength photons that are absorbed in the neutral p-side can only diffuse in this region as there is no electric field. If recombination life time of the electron is τ_e , it diffuses a mean distance L_e given by $\sqrt{(2D_e t\alpha\mu_e)}$ where D_e is its diffusion coefficient in the p-side. Consequently only those EHPs photo generated within the minority carrier diffusion length L_e to the depletion layer can contribute to the photovoltaic effect.

3.4. I-V Characteristics of Solar Cell

3.4.1. I-V Characteristics

If a solar cell is short circuited with illuminating by sunlight, there will have a short circuit current. This current is known as photo current I_{ph} which depends on the number of EHPs photo generated within the volume enclosing the depletion region and diffusion Length to the depletion region. The greater is the light intensity, the higher is photo generation rate and larger isI_{ph} . If I is the light intensity then the short circuit current is

$$I_{sc} = -I_{ph} = -KI$$

Where K is constant that depends on the particular device. The photo current does not depend on the voltage across the p-n junction . When a resistance is connected across the cell, the total current flow through the resistance is given by

$$I = I_d - I_{ph}$$

Where $I_d = I_0\,[\exp(\frac{eV}{nkT})\text{-}1]$ is the diode characteristics .

So, the total current through the resistor is:

$$I = -I_{ph} + I_0\,[\exp(\frac{eV}{nkT})\text{-}1]$$

Figure 3.4 shows I-V Characteristics of a typical solar cell.

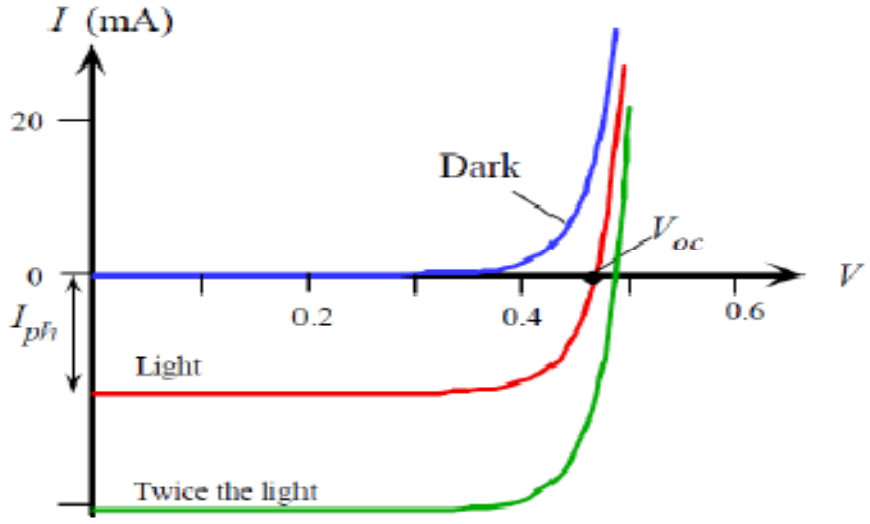


Figure 3.4: I-V Characteristics of a Typical Solar Cell

3.4.2. Equivalent Circuit

Figure 3.5 shows the equivalent circuit of a solar cell.

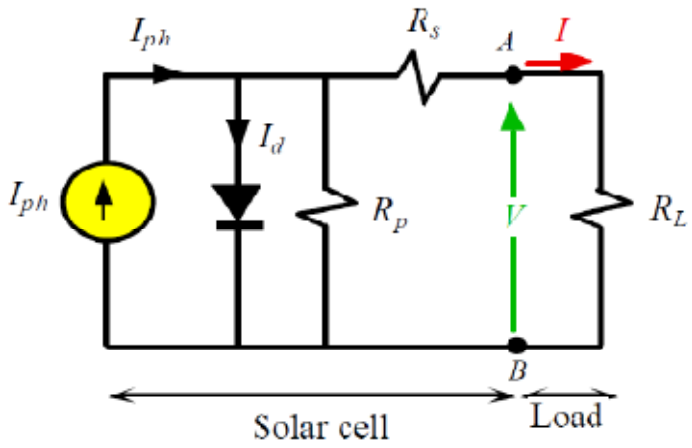


Figure 3.5: Equivalent Circuit of a Solar Cell

Series Resistance R_s due to all these electron paths in the n-layer surface region to finger electrodes.

Shunt Resistance R_p due to a fraction of the photo generated carriers which can flow through the crystal surfaces (edge of the device) or through grain boundaries in polycrystalline devices instead of flowing in the external load R_L

3.4.3. Efficiency and Fill Factor

Figure 3.6 shows solar cell which drives a load.

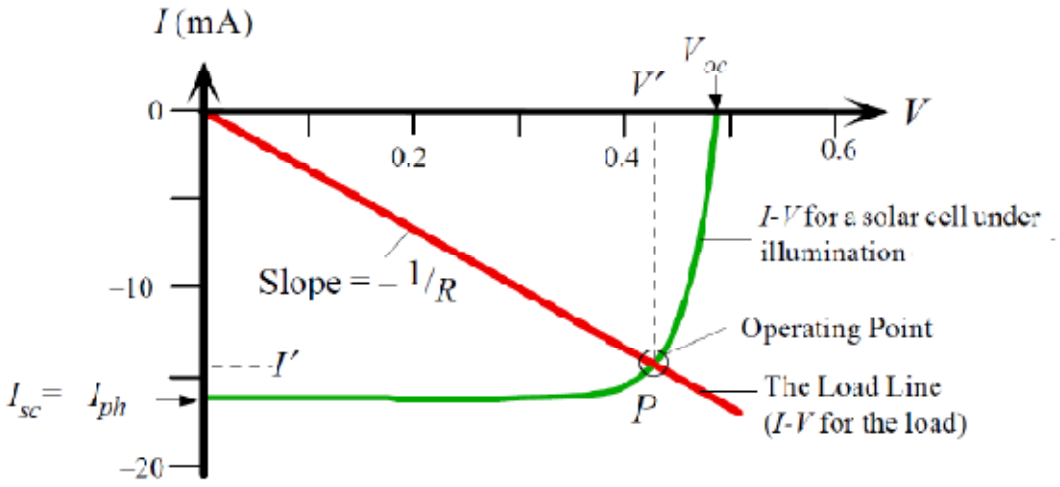


Figure 3.6: Solar Cell Driving a Load

Ideal Conversion Efficiency, $\eta = \frac{Maximum\ Power\ Output}{Incident\ Input\ Power}$

Where, maximum power output, $P_m = V_m I_m$

The term Fill Factor (FF) is defined as:

$$FF = \frac{Maximum\ Power\ Output}{Desirable\ Goal\ Output} = \frac{V_m I_m}{I_{sc} V_{oc}}$$

So,

$$\eta = \frac{V_m I_m}{P(in)}$$

$$= \frac{FF \times I_{sc} \times V_{oc}}{P(in)}$$

3.5. Shockley–Queisser Limit

Figure 3.7 shows the Shockley–Queisser Limit

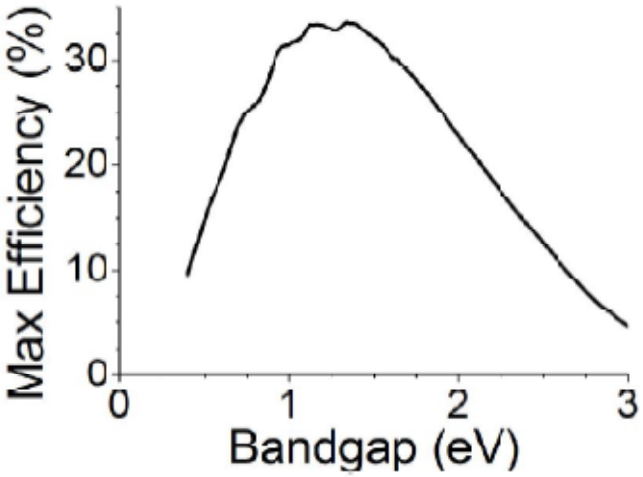


Figure 3.7: Shockley-Queisser Limit

The Shockley-Queisser Limit or detailed balance limit refers to the maximum theoretical efficiency of a solar cell using a p-n junction to collect power from the cell.

It was first calculated by William Shockley and Hans Queisser at Shockley Semiconductor in 1961.[19] The limit is one of the most fundamental to solar energy production and is considered to be one of the most important contributions in the field.

The limit places maximum solar conversion efficiency around 33.7% assuming a single p-n junction with a band gap of 1.4eV (using an AM 1.5 solar spectrum). That is, of all the power contained in sunlight falling on an ideal solar cell(about 1000W/m^2),only 33.7% of that could ever be turned into electricity. The most popular cell material, silicon, has a less favourable band gap (1.1eV, maximum efficiency of 29%).

The Shockley-Queisser limit only applies to cells with a single p-n junction; cells with multiple layers can outperform this limit. In this extreme, with an infinite number of layers, the corresponding limit is 86% using concentrated sunlight.

CHAPTER 4

THIN FILM PHOTO VOLTAICS

4.1. Thin Film

A thin film is a layer of material ranging from fractions of a nanometer (monolayer) to several micrometers in thickness. Thin film features mostly come from its thickness.

It needs substrate and characteristics depend on the surface condition of the substrate.

It is formed after decomposing the materials into atomic / molecular scale by physical and chemical measure.

Properties of Thin Film [20]:

1. Uniformity between neighbouring elements, Minimum defects> Low noise.

2. Minimum floating capacitance between neighbouring elements (thickness 0.1m-0.01m).

3. Strong adhesion , long term stability, temperature stability, tough terminal strength .

4. Linear temperature coefficient.

5. Selectable crystalline and non-crystalline.

Features of Thin Film:

1. High stability.

2. High frequency operation .

3. Miniature size.

4. Low cost.

4.2. Thin Film Photo Voltaic cells

A thin film solar cell (TFSC), also called a thin film photovoltaic cell (TFPV), is a solar cell that is made by depositing one or more thin layers (thin film) of photovoltaic material on a substrate. The thickness range of such a layer is wide and varies from a few nanometer to tens of micrometers.

Many different photovoltaic materials are deposited with various deposition methods on a variety of substrates. Thin film solar cell are usually categorized according to the photovoltaic material used:

1. Amorphous Silicon(a-Si) and thin film Silicon (TF-Si).
2. Cadmium Telluride (CdTe)
3. Copper Indium Galium Selenide (CIGS)
4. Dye-sensitized Solar cell(DSSC).
5. Organic solar cell.

4.3. Thin Film PV Cell Materials

The thin film photo voltaic cell (TFPV) consists of several layers of different materials in thin film form. In general the solar cell consists of substrate, Transparent Conducting Oxide(TCO) ,window layer (p or n type), absorber layer(i or p type) and metal contact layer. Each of the component materials has different physical and chemical properties and each affects the overall performance of the device in some form or other. A critical understanding of the behaviour of these individual components is essential for designing a thin film photovoltaic cell.

4.3.1. Substrate

The substrate is metal or metallic coating on a glass or polymer substrate which also acts as the contact. Substrate is a passive component in the device and is required to be mechanically stable, matching thermal expansion coefficient with deposited layer and insert during the device fabrication.[21]

Properties Required for a Substrate:

1. Rigidity.
2. Thermal management ability.
3. Proper electrical insulation to withstand high voltages without breakdown.
4. Dielectric Strength.
5. Low dielectric constant value(for high frequency operation).
6. Dissipation factor.
7. High electrical resistance(1014ohm-cm).
8. High thermal conductivity.
9. Good insulator at room temperature.
10. Good surface smoothness.
11. Coefficient of thermal expansion(CTE) matched.
12. Good mechanical strength .
13. Chemically stable.
14. Low porosity(to prevent entrapment of gases which causes film contamination).
15. Low cost.
16. Good uniformity.
17. Low weight.

Materials used for thin film:

1. Aluminium
2. Glass
3. Beryllium oxide based ceramic(Beryllia)

4. Aluminium nitrite
5. Si
6. SiC
7. Metals

4.3.2. Transparent Conducting Oxide(TCO)

Transparent Conducting Oxide in general are n-type degenerate semiconductor with good electrical conductivity and transparency in the visible spectrum. Thus, a resistance contact to the device and transmission of most of the incident light to the absorber layer is ensured. The conductivity of TCO depends on the carrier concentration and mobility.

An increase in carrier concentration may result in enhanced free carrier absorption which reduces the transparency of the TCO in the higher wavelength region. Hence increasing the mobility by improving crystalline properties is considered to be a pathway for a good TCO.[21]

Table 4.1: Typical resistivity and transmission (in the visible) for various TCO materials investigated for TFPV application.[22]

Material	Resistivity (? cm) x 10^4	Transparency (%)
SnO_2	8	80
In_2O_3:Sn(ITO)	2	>80
In_2O_3:Gn(IGO)	2	85
In_2O_3:F	2.5	85
Cd_2SnO_4(CTO)	2	85
Zn_2SnO_4(ZTO)	100	90
ZnO:In	8	85

It is usually chosen as Transparent Conducting Oxide (TCO). Indium Tin Oxide (ITO) or tin-doped indium oxide is a solid solution of Indium (III)oxide and tin (IV) oxide, typically 90% In_2O_3 ,10% SnO_2 by weight. It is transparent and colourless in the thin layers while in bulk form it is yellowish to grey. In the infrared region of the spectrum it is a metal like mirror.

4.3.3. Window Layer

The primary function of a window layer in a heterojunction is to form a junction with the absorber layer while admitting a maximum amount of light to the junction region and absorber layer, no photocurrent generation occurs in the window layer. For high optical throughput with minimal resistive loss the band gap of the window layer should be as high as possible and thin as possible to maintain low series resistance. It is also important that any potential 'spike' in the conduction band at the hetero junction be minimized for optical minority carrier transport.

For a-**Si** photovoltaic cells, depending on the device configuration, the n or p-layer is very thin and acts like a window layer that allows all the photons to be transmitted to the i-region. Because of very high absorbance of these films, very thin doped layer (10nm) is required. Alloy film such as a SiC: having excellent optical and good photoconductivity it has been used as the window layer.

4.3.4. Absorber

Copper Indium Gallium Selenide (CIGS):

The I-III-IV chalcopyrite materials have some very desirable properties for photovoltaic application. $CuInS_2$ having a band gap of 1.53 eV is consider an ideal material for photovoltaic application. The difficulties in controlling the sulfur during deposition and the relatively rapid diffusion of metal and impurity species, even at low temperatures slow down the development of this material. However, devices with efficiency 11.4% have been reported. Even through the efficiency and stability of the device are very promising, there are several factors that are favorable for large scale production of such devices.[23]

Cadmium Telluride (CdTe):

According to its optoelectronics and chemical properties, CdTe is an absorber material for high efficiency and low cost thin polycrystalline solar cell. CdTe is a direct band gap material with an energy gap 1.5 eV, and an absorption coefficient 10^5/cm in the visible range, which means that a layer thickness of a few micrometers is sufficient to absorb 90% of the incident photos. CdTe solar cell devices with efficiency the following requirements such as activation treatment that changes the bulk, interfacial and grain boundary properties, and the difficulty of forming an ohmic contact are needed to be fulfilled without the device. Considering these CdTe has deficiency.[24]

Amorphous, Micro/Nanocrystalline and Polycrystalline Silicon [25]:

Silicon is widely accepted as a thin-film solar material because: (a) it is abundant and non toxic; (b)it requires low process temperature, enabling module production on flexible and low cost substrate s; (c) the technological capability for large –area deposition exists; and (d) material requirements are low, 1.2mm, due to the inherent high absorption coefficient compared with crystalline silicon. The high absorption of light results from the inherent high disorder acts as recombination centers that severely reduce the carrier lifetime and pin the Fermi energy level so that the material cannot be doped either n or p-type. Incorporation of 10% hydrogen in the film during deposition greatly reduces the density of the defects to defects to 10^{16}/cm^3, yielding a new and exotic material, a-Si:H material which has a well defined optical threshold at 1.75 eV compared with the crystalline Si indirect band gap at 1.1 eV. The reduction in the defect density makes a-Si:H material suitable for doping and alloying with a range of materials and for junction device fabrication . Microcrystalline and polycrystalline silicon films have lower optical absorption in contrast to the high optical absorption in a-Si. Thus, in the former case, light trapping is necessary to extract the photon energy efficiently.

4.4. Hydrogenated Amorphous Silicon

4.4.1. Atomic Structure

Each Si atom is covalently bonded to four neighboring Si atoms. All bonds have the same length and the angles between the bonds are equal. The number of bonds that an atom has with its immediate neighbors in the atomic structure is called the coordination number or unit cell can be defined, from which the crystal lattice can be reproduced by duplicating the unit cell and stacking the duplicates next to each other. Such a regular atomic arrangement is described as a structure long range order. A diamond lattice unit cell represents the real lattice structure of single crystal silicon.[26] Fig 4.1 illustrates that a-Si:H has the scale, where most Si atoms have covalent bonds with four neighbors. The a-Si:H has the same short range as the single crystal silicon but it lacks the long range order. The small deviation in bonding angles and bonding lengths between the neighboring atoms in a Si:H lead to a complete loss of the locally order structure on a scale exceeding a few atomic distances. The resulting atomic structure of a Si:H is called the continuous random network.

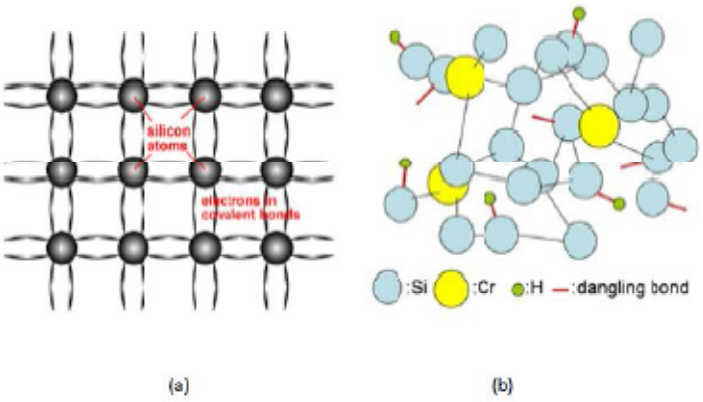


Figure 4.1: Atomic Structure of (a) Single Crystalline Silicon and (b)Amorphous Silicon

Due to the short range order in the continuous random network of a-Si:H, the common semiconductor concept of the energy states bands, represented by the conductor and valence bands, can still be used. The larger deviations in bonding angles and bonding lengths between the neighboring atoms in a Si:H result in the weak or strained bonds and the weak bonds can easily break and form defects in the atomic network.

It can be noted that in the continuous random network, the definition of a defect is modified with respect to the crystal structure. In a crystal any atom that is out of place in a lattice forms a defect. In the continuous random network an atom cannot be out of place. Here, a defect is the co-ordination defect. This happens when an atom has too many or too few bonds. In a Si:H the defects are mainly represented by Si atoms that are covalently bonded to only three Si atoms and have one unpaired electron, a so-called dangling bond. Since this configuration is the dominant defect in s-Si:H, the defects in a-Si-H, the defects in a-Si:H are often related to the dangling bonds.

When amorphous silicon is deposition in such a way that hydrogen can incorporate in the network, then the hydrogen atoms bond with most of the dangling bonds. it can be said that the dangling bonds are passivated by hydrogen. Hydrogen passivation reduces the dangling bond density from about $10^{21}cm^{-3}$ in pure a-Si to $10^{15} - 10^{16}cm^{-3}$in a-Si:H, i.e. less than one dangling bond per million Si atoms. In figure 4.1 some of the defects with unpassivated dangling bonds and with hydrogen passivated dangling bond are depicted. Device quality a-Si:H contains from 1 to 10 atomic percent of hydrogen.

In summary, the short range order in a-Si:H network and the hydrogen passivation of the dangling bonds are responsible for semiconductor properties of amorphous silicon.

4.4.2. Density of States

The periodic atomic structure of single crystal silicon results in the range of allowed energy states for electrons that are called energy bands and the excluded energy ranges, forbidden gaps or band gap. Figure 4.2 shows schematically the distribution of density of states for single crystal silicon, in which the valence and the conduction band are separated by a well defined band gap of 1.12 eV.[27] In case of a Si:H, there is a continuous distribution of density of states and no well defined band gap exits between the valence band and the conduction band.

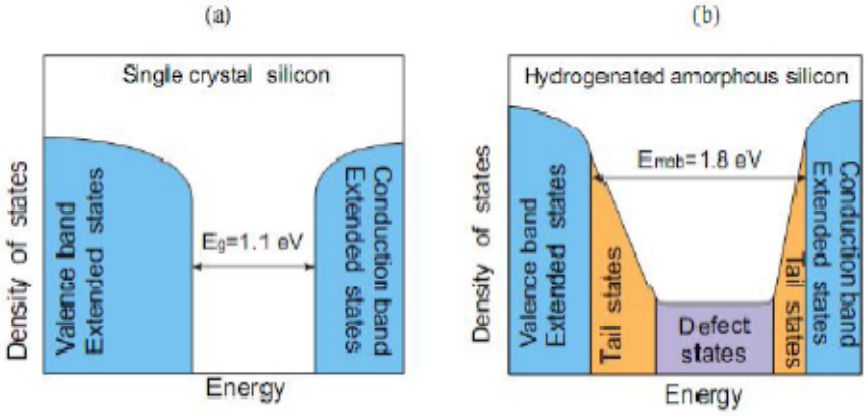


Figure 4.2: Distribution of Density of Allowed Energy States for Electron for(a)Single Crystal Silicon (b) a-Si:H

Due to the long range order disorder in the atomic structure of a-Si:H the energy states of the valence band and the conduction bands spread s into the band gap and form regions that are called band tail states. The band tail states represent the energy states of electros that form the strained bonds in the a-Si:H network .the width of the band tails is a measure for the amount of disorder in a a-Si:H material. More disorder in a-Si:H means that the band tails are broader. In addition, the dangling bonds introduce allowed energy states that are located in the central region between the valence band and conduction band states.

The schematic representation of carries in the localized staes in a-Si:H used to define its band gap. This gap is denoted by the term mobility gap, E_{mob}, because the presence of a considerable density of states in this gap conflicts the classical concepts of the band gap. the energy levels that separate the extended states from the localized states in a-Si:H are called the valence band and the conduction band mobility edges. The mobility gap of a-Si:H is larger than the band gap of single crystal silicon and has a typical value 1.8 eV. The localized tail states act as trapping centers and build up a space charge in a device, the dangling bond states act as very effective recombination centers and affect in particular the lifetime of the charge carries.

4.4.3. Optical properties

The optical properties of a-Si:H are usually characterized by its absorption coefficient and a value of the optical band gap. Fig 4.3 shows the absorption coefficient of a-Si:H that is fabricated at Delt university of technology as a function of photon energy. The absorption coefficient of c-Si:H is shown for reference. This figure demonstrates that a-Si:H absorbs almost 100 times more than c-Si in the visible part of the solar spectrum. The higher absorption is due to the disorder in the atomic structure of a-Si:H that behaves like a direct band gap material. This means that 1 um thick a-Si:H layer is sufficient to absorp 90% of usable solar energy. In practice the thickness of a-Si:H solar cells is less than .5 um that 100 times less than the thickness of a typical single crystal silicon cell. This results an important savings in both material and energy in fabrication of a-Si:H solar cells.

Another advantage of a-Si:H is that the optical absorption can be slightly changed by varying its hydrogen content, and it can be greatly changed by alloying with carbon or germanium. The absorption coefficient of hydrogenated amorphous silicon carbide (a-Si:H) and hydrogenated amorphous silicon germanium that are fabricated at Delt

university of technology are also shown in Figure 4.3. This feature of easy alloying of a Si:H allows to design solar cell structures in which a-Si:H based materials with different absorption properties can be used as active layers.

In general ,a material with higher optical bandgap absorps less. The optical bandgap E_{opt} is determined by extrapolating a linear part of the following function[$\alpha(E) \times \eta(E) \times E]^{-(1+p+q)}$ Vs the photon energy E to $\alpha(E)$=0 , for $\alpha \geq 10^3 cm^{-1}$:

$$[\alpha(E) \times \eta(E) \times E]^{-(1+p+q)} = \text{B(E-}E_0\text{pt)} \qquad (4.1)$$

Where $\alpha(E)$ is the absorption coefficient, $\eta(E)$ is the refractive index,p and q are the constants that describe the shape of density of extended states distribution for the conduction band and valance band respectively and B is a prefactor.

When density states distribution near the band edges has a square root energy dependence as is commonly the case in crystalline semiconductor,equation(4.1) decribes the so called

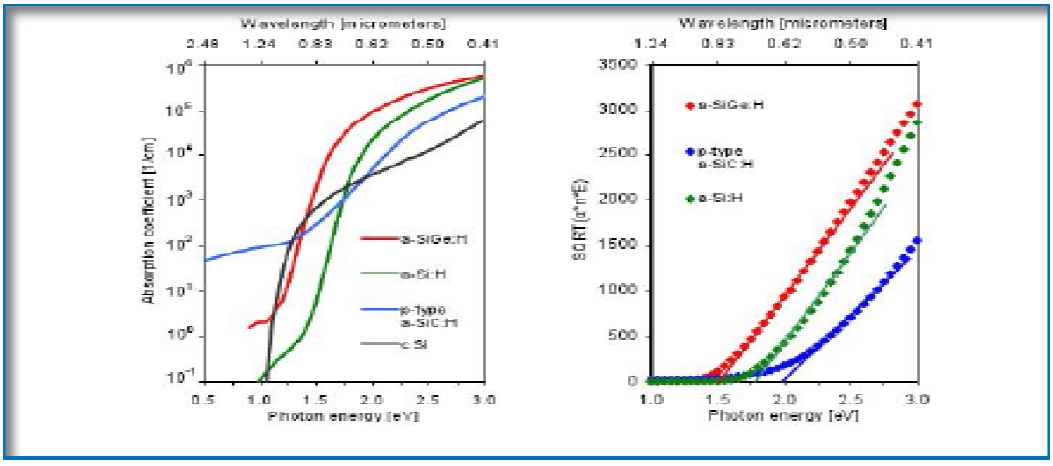


Figure 4.3(a)Absorption Coefficient as Function of Photon Energy for a-Si:H and a-SiGe:H Fabricated at Delt University of Technology. The Absorption Coefficient of c-Si is shown for reference.(b)Tauc Plot with Linear Extrapolation to determine the Tauc Optical Band Gap for a-Si:H, p-type a-SiC:H and a-SiGe:H.

tauc plot and the corresponding optical band gap is called the tauc optical gap. When the distribution near the band edges is assumed to be linear, E_{opt} is the cubic optical band gap. The tauc device quality intrinsic a-Si:H is in the range 1.7 to 1.8 eV, the cubic gap of the same material is usually .1 to 0.2 eV smaller than tauc gap. The tauc with linear extrapolation to determine the tauc optical gap for a-Si:H (E_{opt}=1.77 eV), p-type a-SiC:H(E_{opt}= 1.95 eV) and a-SiGe:H (E_{opt}=1.52 eV) is shown in Fig 4.3.

4.4.4. Electrical Properties

The electrical properties of a-Si:H are usually characterized in terms of dark conductivity and photoconductivity. The measurement of these two properties is a standard approach to obtain information about the quality of a-Si:H material for application in solar cells. Also it gives information about the mobility lifetime product and the influence of impurities in a-Si:H. The mobilities of the charge carriers in the extended states of a-Si:H are about two orders of magnitude lower than in single crystal silicon. Typically, the electron mobility in 10 cm^2/Vs, and hole mobility is 1 cm^2/Vs in intrinsic a-Si:H. the low values of electron and hole mobilities and high mobility gap of a-Si:H result in a low dark conductivity, which in device quality intrinsic a-Si:H is less than 10^{-10} $\Omega^{-1}cm^{-1}$. This material is further characterized by an excellent photoconductivity that is higher than , when measured using the am 1.5 light spectrum and the incident power of 1000mW/cm^2.

4.5. Typical Thin Film PV Cell Structure

Three forms of thin-film solar panels have been developed: Amorphous Silicon, Cadmium Telluride, and CIGS technology. All three forms are highly-absorbent and can

operate effectively at a thickness of about 1 micron, which means they are less expensive than the thick crystalline silicon alternative.[28]

The film PV cell differs from traditional crystalline silicon in that it is arranged spontaneously and thinly layered, whereas crystalline is almost grid-like in pattern and thick. Figure 4.4 shows a typical structure of (a)c-Si Solar Cell (b)a-Si:H Solar Cell and (c)CIGS Solar Cell.

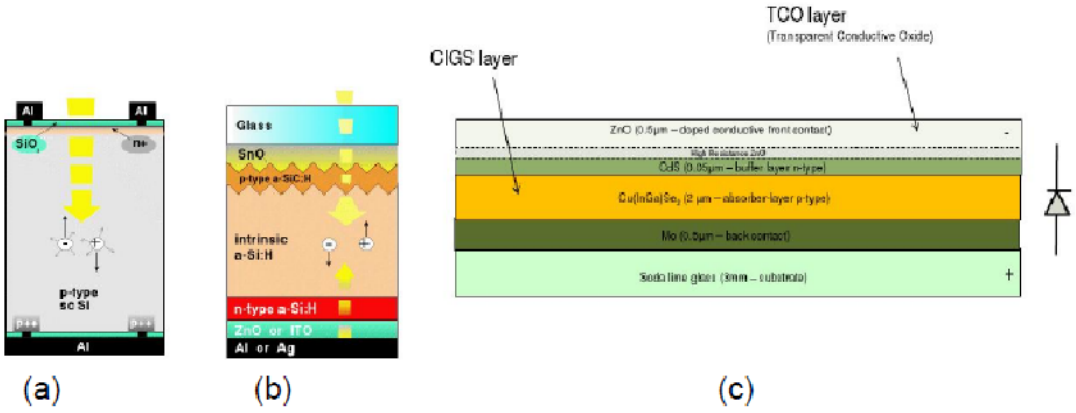


Figure 4.4: A Typical Structure of (a)c-Si Solar Cell (b)a-Si:H Solar Cell and (c)CIGS Solar Cell.

4.6. Tandem/Multi-junction PV Cell Structure

The tandem or cascade cells use two or more cells in tandem or in cascade to increase the absorbed photons from the incident light. The first cell is made from a wider gap material and only absorb photons with hν> E_{g1}. The second cell absorbs photons that pass the first cell and have hν> E_{g2}.[29]

Multi junction solar cells are cells containing several p-n junctions. Each junction is tuned to a different wavelength of light, reducing one of the largest inherent sources of losses, and thereby increasing efficiency.[30]

Figure 4.5 shows (a)Tandem Solar Cell (b) Structure of Multi-Junction Solar Cell.

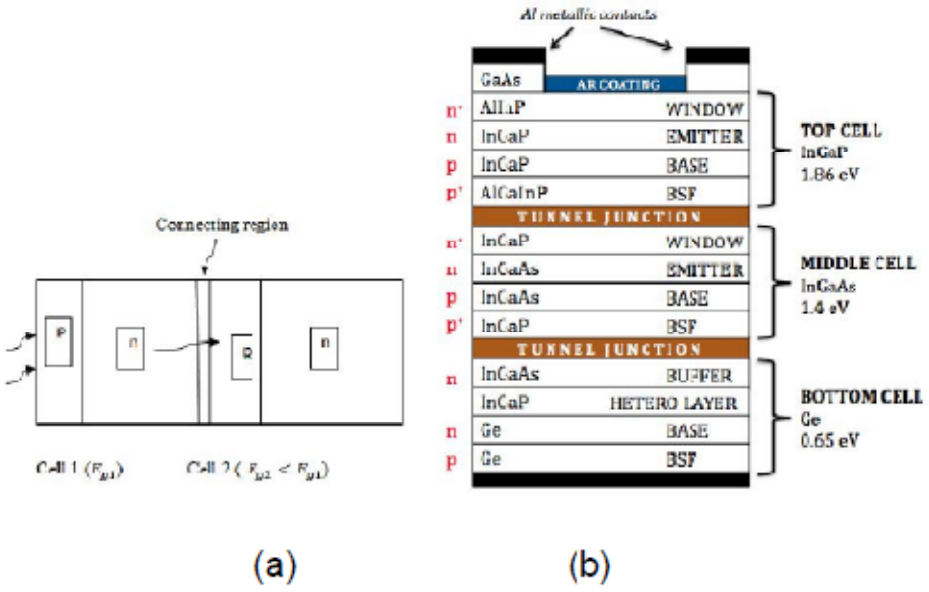


Figure 4.5:(a)Tandem Solar Cell (b) Structure of Multi-Junction Solar Cell

The choice of material for such sub-cell is determined by the requirements for lattice-matching, current-matching, and high performance optoelectronic properties.

CHAPTER 5
SIMULATION AND ANALYSIS OF THIN FILM

5.1. Overview of Simulation Software ATLAS

ATLAS is a device simulation framework. ATLAS enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC and time domain responses for all semiconductor based technologies in 2D and 3D. 2D simulation has been used for thin film.

Key Features:

1. Accurately characterize physics-based devices in 2D or 3D for electrical, optical, and thermal performance without costly split-lot experiments.
2. Solve yield and process variation problems for optimal combination of speed, power, density, breakdown, leakage, luminosity, or reliability.
3. Fully integrated with ATHENA process simulation software, comprehensive visualization package, extensive database of examples, and simple device entry.
4. Choose from the largest selection of silicon, III-V, II-VI, IV-IV, polymer/organic technologies including CMOS, bipolar, high voltage power device, VCSEL,TFT, optoelectronic, LASER, LED, CCD, sensor, fuse, NVM, ferroelectric, SOI, FinFET, HEMT, and HBT .

Physical Models Provided by ATLAS [31]:

1. DC, AC, small-signal and full time dependency
2. Drift diffusion transport models
3. Hydrodynamic transport models
4. Graded and abrupt hetero-junctions
5. Optoelectronic interactions with general ray tracing
6. Stimulated emission and radiation
7. Fermi-Dirac and Boltzmann statistics
8. Advanced mobility models
9. Heavy Doping Effects
10. Full Acceptor and donor trap dynamics
11. Ohmic, Schottky and insulating contacts
12. SRH, radiative, Auger and surface recombination
13. Band-to-Band and Fowler-Nordheim tunneling
14. Quantum Transport Models

15. Thermoionic emission currents etc.

ATLAS uses powerful numerical techniques, including:

1. Accurate and robust discretization techniques.
2. Gummel, Newton, and block-Newton nonlinear iteration strategies.
3. Efficient solvers, both direct and iterative, for linear sub-problems.
4. Powerful initial guess strategies.
5. Small-signal calculation techniques that converge at all frequencies.
6. Stable and accurate time integration

5.1.1. ATLAS Inputs and Outputs

Figure 5.1 shows the types of information that flow in and out of ATLAS. Most ATLAS simulations use two input files. The first input file is a text file that contains commands for ATLAS to execute. The second input file is a structure file that defines the structure that will be simulated.

ATLAS produces three types of output files. The first type of output file is the run-time output, which gives you the progress and the error and warning messages as the simulation proceeds. The second type of output file is the log file, which stores all terminal voltages and currents from the device analysis. The third type of output file is the solution file, which stores 2D and 3D data relating to the values of solution variables within the device at a given bias point. Figure 5.1 shows ATLAS inputs and outputs.

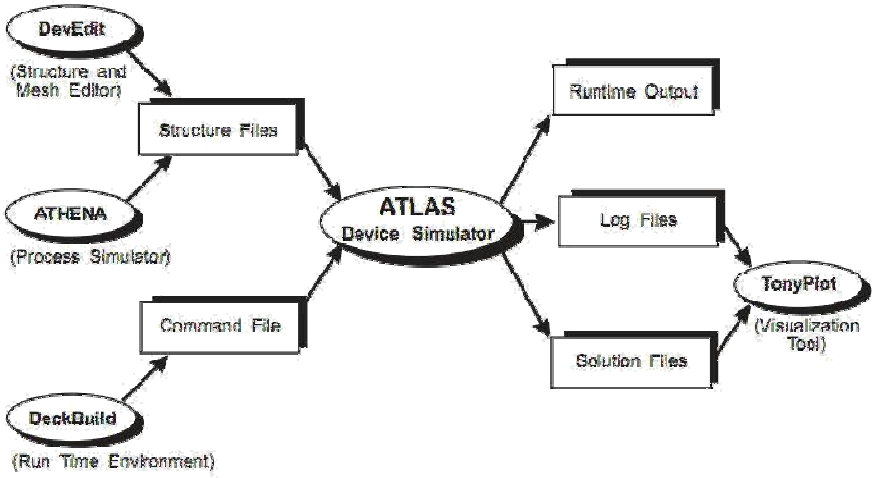


Figure 5.1: ATLAS Inputs and Outputs

5.2. Simulation and Analysis of results

In this section, simulation outputs are analyzed for different types of photovoltaic cells and following output parameters are compared:

1. J-V Characteristics
2. Power Curve
3. Short-circuit Current Density (Jsc)
4. Open Circuit Voltage (Voc)
5. Fil Factor (FF)
6. Efficincy (η)

Calculation of Jsc, Voc, FF and efficiency (η) are done by the following equations:

Jsc = value of current when V=0 in J-V curve

Voc = value of voltage when J=0 in J-V curve

Pm = peak value of power in power curve

$$FF = \frac{P_m}{V_{OC} \times J_{sc}}$$

So,

$$\eta = \frac{FF \times V_{oc} \times J_{sc}}{P_{in}}$$

For simulation purposes, AM1.5 solar spectrum condition has been used which means input optical power is approximately 1000KW/m^2 or 100mW/cm^2

5.2.1. A Typical Crystalline Solar Cell

First simulation done is of a typical solar cell structure[32]. The device used is a diode of n+ over a p substrate. The junction depth is approx 0.25um. A single contact is placed in the center of the structure. Typical solar cells will have this structure repeated many times across a large area. Here advantage is taken of the reflecting boundary conditions at the edges of the structure to simulate just one cathode contact. Figure 5.2 shows Mesh Structure of a Typical Solar Cell

Material: **Silicon**

Contact Material(Anode and Cathode): **Aluminium**

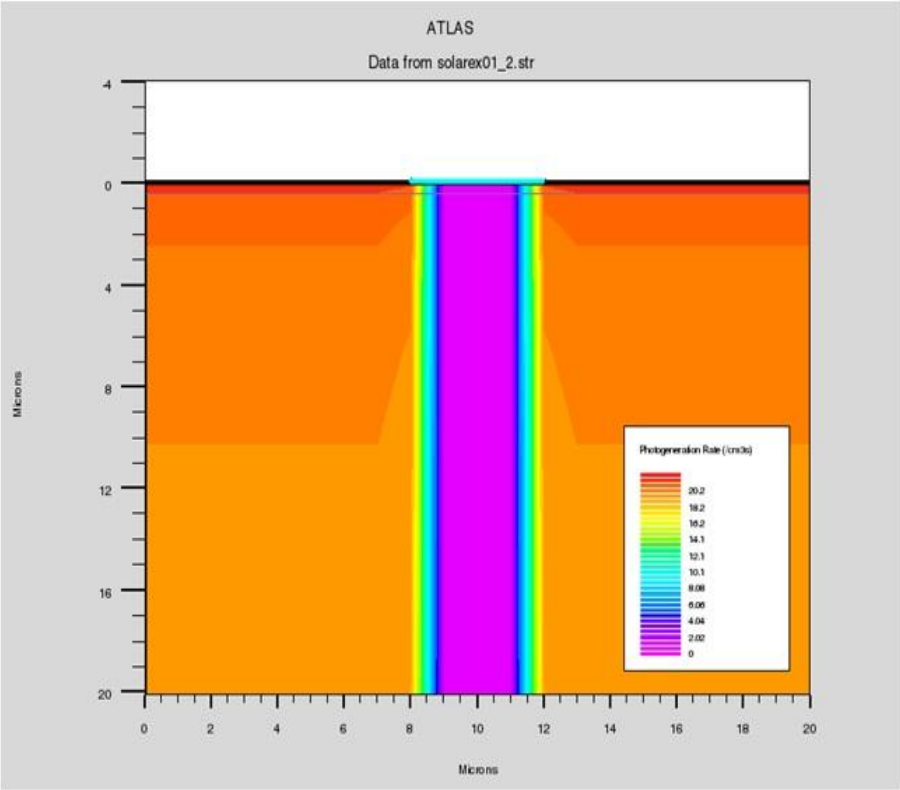


Figure 5.2: Mesh Structure of a Typical Solar Cell

Current vs Wavelength:

The range of wavelength used was 300nm to 1000nm.Plotting the resulting log file it is seen how the cathode current varies with wavelength. Figure 5.3 shows Current Vs Wavelength of a Typical Solar Cell.

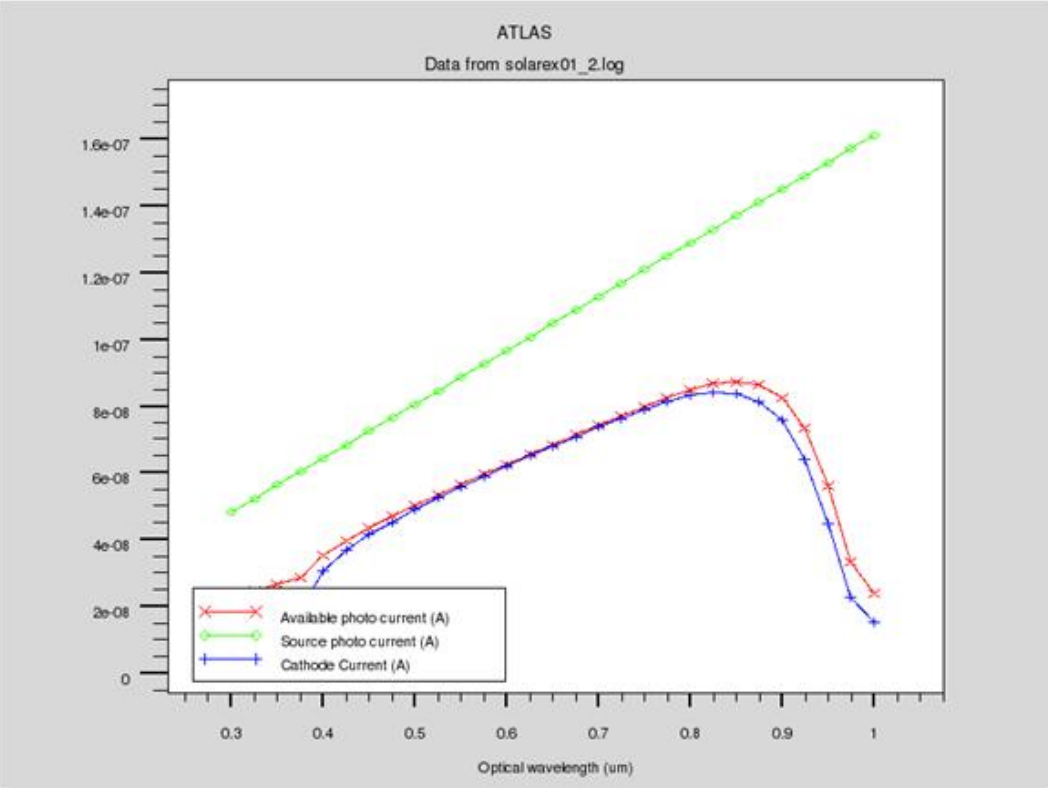


Figure 5.3: Current vs Wavelength of a Typical Solar Cell

Setting a plot Vs wavelength of source photocurrent (current available in the light beam), available photocurrent (current available for collection), and actual cathode current show how the device behaves. The losses between source and available photocurrent are caused by reflections and transmission. This dominates the losses at all except the shortest wave-lengths. The losses from available photocurrent to the actual simulated cathode current are due to recombination. These are very low except at the extremes.

J-V Characteristics: Figure 5.4 shows J-V Characteristics of a Typical Solar Cell.

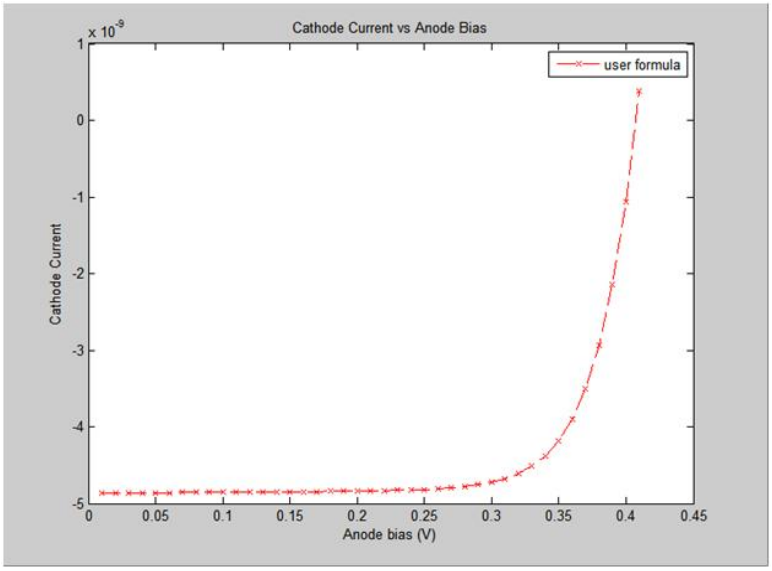


Figure 5.4: J-V Characteristics of a Typical Solar Cell

Power Curve: Figure 5.5 shows Power Curve of a Typical Solar Cell.

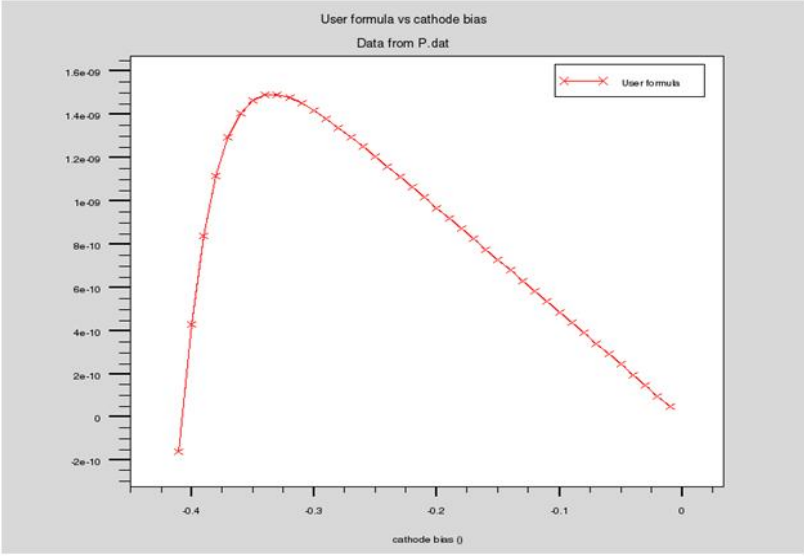


Figure 5.5: Power Curve of a Typical Solar Cell

Simulation Results:

Table 5.1: Extracted Data from Simulation of a Typical Solar Cell

Parameters	Value
Jsc(mA/cm^2)	24.3
Voc(V)	0.407
Pm(mW/cm^2)	7.4
FF	0.748
Efficiency (%)	7.4

5.2.2. Thin Film Tandem Solar Cell

The simulation shows IV characteristics of a tandem a-Si:H/uc-Si:H solar cell[33].

Structure: Figure 5.6 shows Mesh Structure of Thin Film Tandem Solar Cell**.**

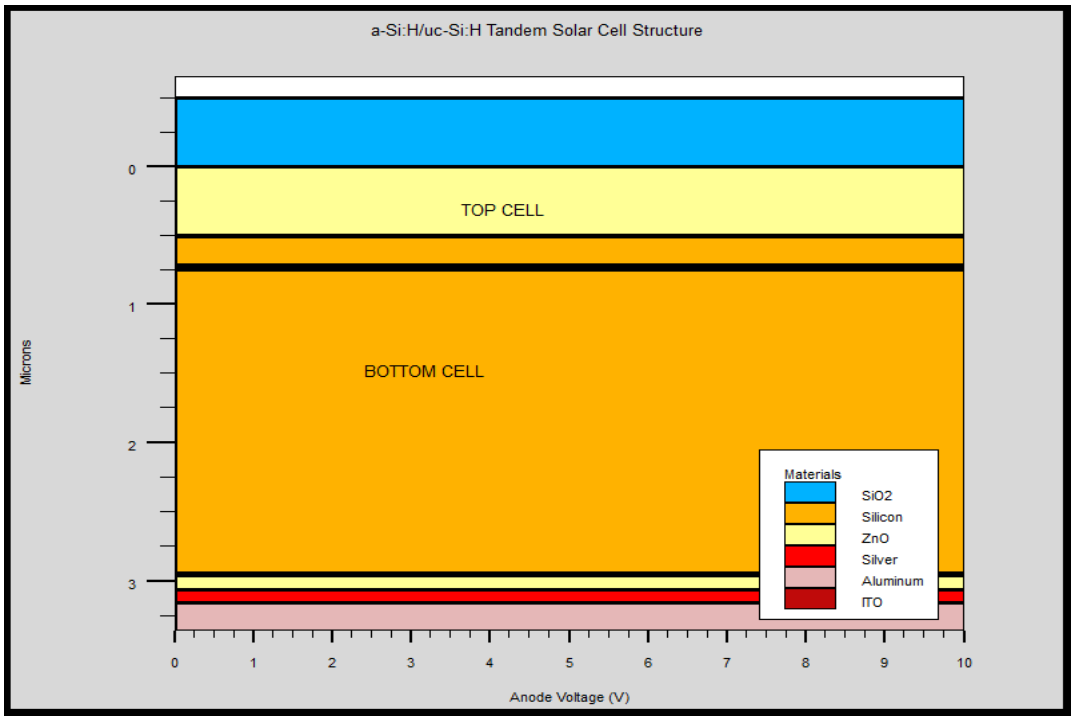


Figure 5.6: Mesh Structure of Thin Film Tandem Solar Cell**.**

The following structure is used in the simulation**: ZnO:Al(500nm)/p-a-Si:H(10nm)/i-a-Si:H(200nm)/n-a-Si:H(15nm)/p-uc-Si:H(10nm)/i-uc Si:H(2.2um)/p-uc-Si:H(15nm)/ZnO(100nm)/Ag.**

Top Cell: Amorphous Silicon

Bottom cell: Micro-Crystalline Silicon

Anode**: ZnO (Zinc Oxide**)

Cathode: **Aluminium**

Common**: ITO (Indium Tin Oxide)**

J-V Characteristics: Figure 5.7 shows J-V Characteristics of Thin Film Tandem Solar Cell.

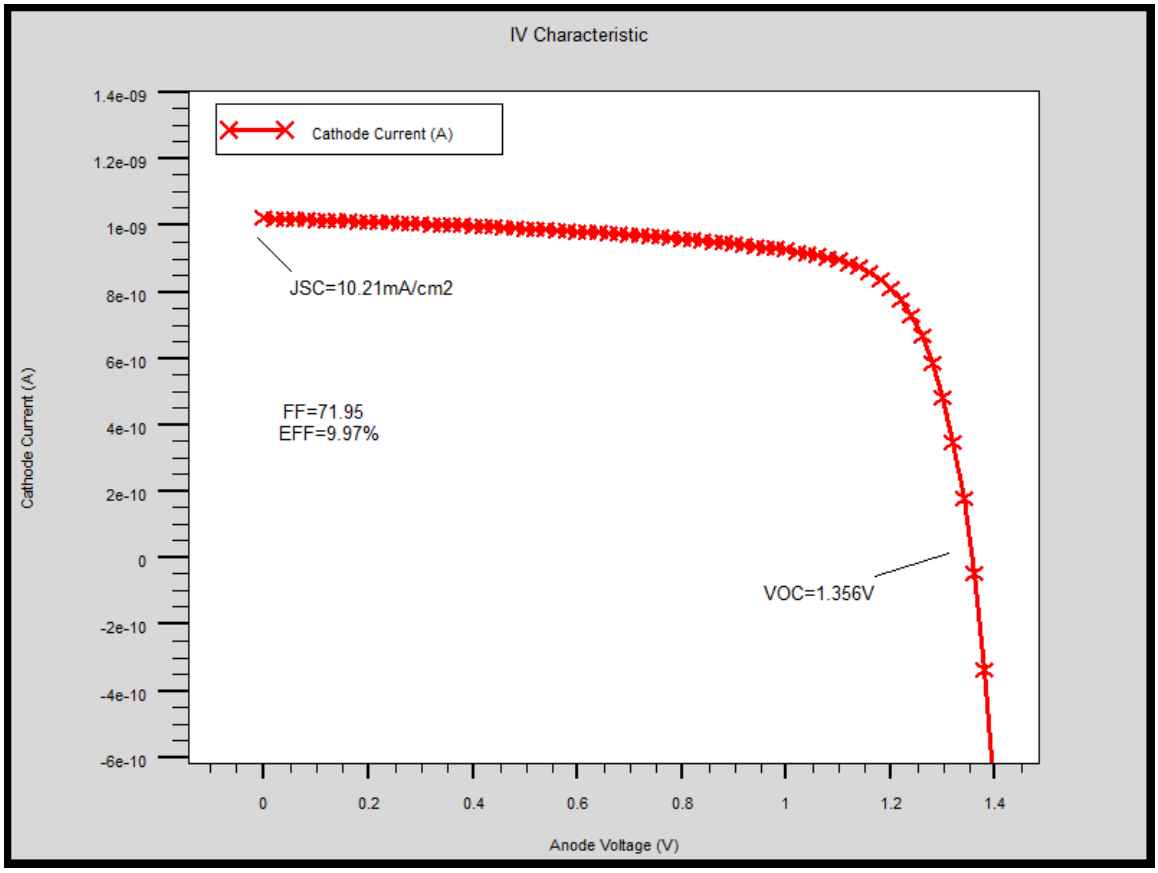


Figure 5.7: J-V Characteristics of Thin Film Tandem Solar Cell

Power Curve: Figure 5.8 shows Power Curve of Thin Film Tandem Solar Cell.

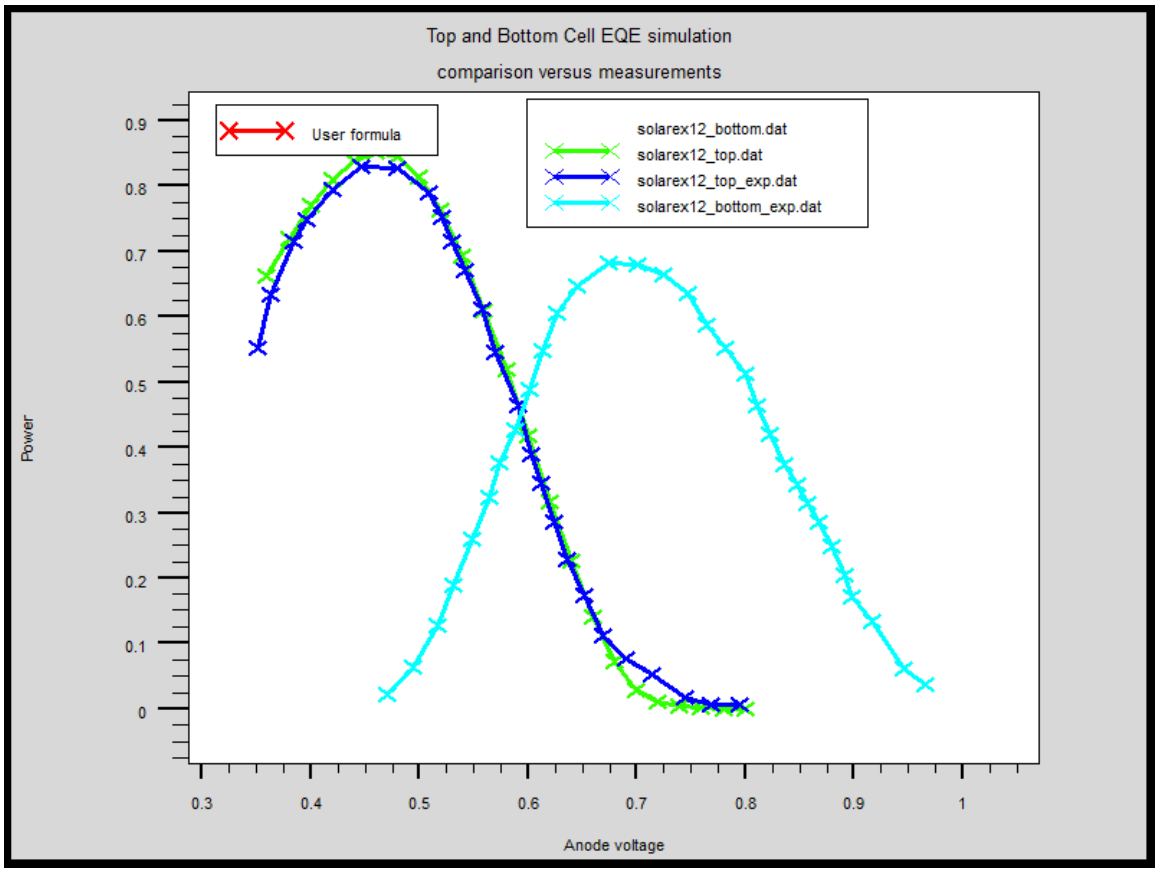


Figure 5.8: Power Curve of Thin Film Tandem Solar Cell

Simulation results:

Table 5.2: Extracted Data from Simulation of Thin Film Tandem Solar Cell

Parameters	Values
Jsc (mA/cm^2)	10.21
Voc(V)	1.356
Pm(mW/cm^2)	9.96
FF	0.7194
Efficiency (%)	9.96

5.2.3. Tandem CIGS Solar Cell[34]

The Thin-film solar cell module based on CIGS is a technology with great potential. Two reasons for this are low material consumption and relatively high efficiency. This shows CIGS solar cell module simulation and optimization. In a solar cell module several cells are connected in series. The cells are the active area of the module whereas the interconnections between cells are the dead area. The efficiency of the module is thus dependent on the number of cells in the module. Indeed there is a tradeoff between maximizing absorption and minimizing resistance of the interconnection

Structure: Figure 5.9 shows Mesh Structure of tandem CIGS Solar cell.

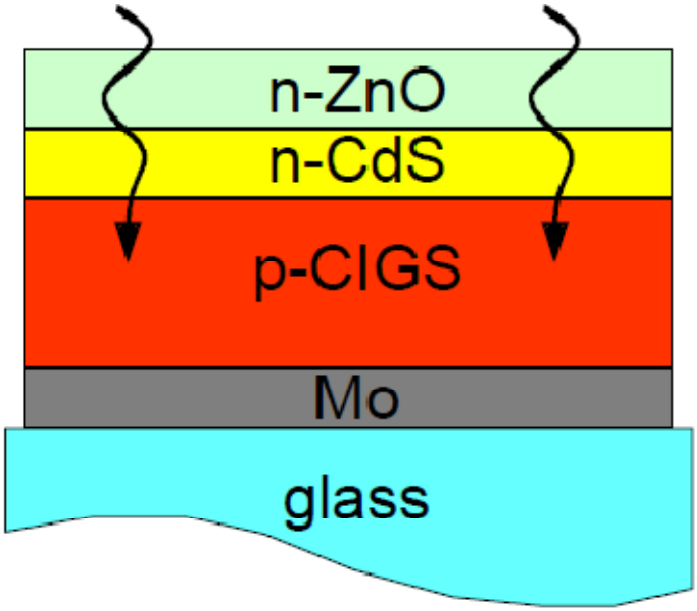


Figure 5.9: Mesh Structure of tandem CIGS Solar cell

Top Cell: CdS

Bottom cell: CIGS

Substrate: Lime Glass

Back Contact: Mo(Formation of MoSe2)

J-V Characteristics: Figure 5.10 shows J-V Characteristics of Tandem CIGS Solar Cell.

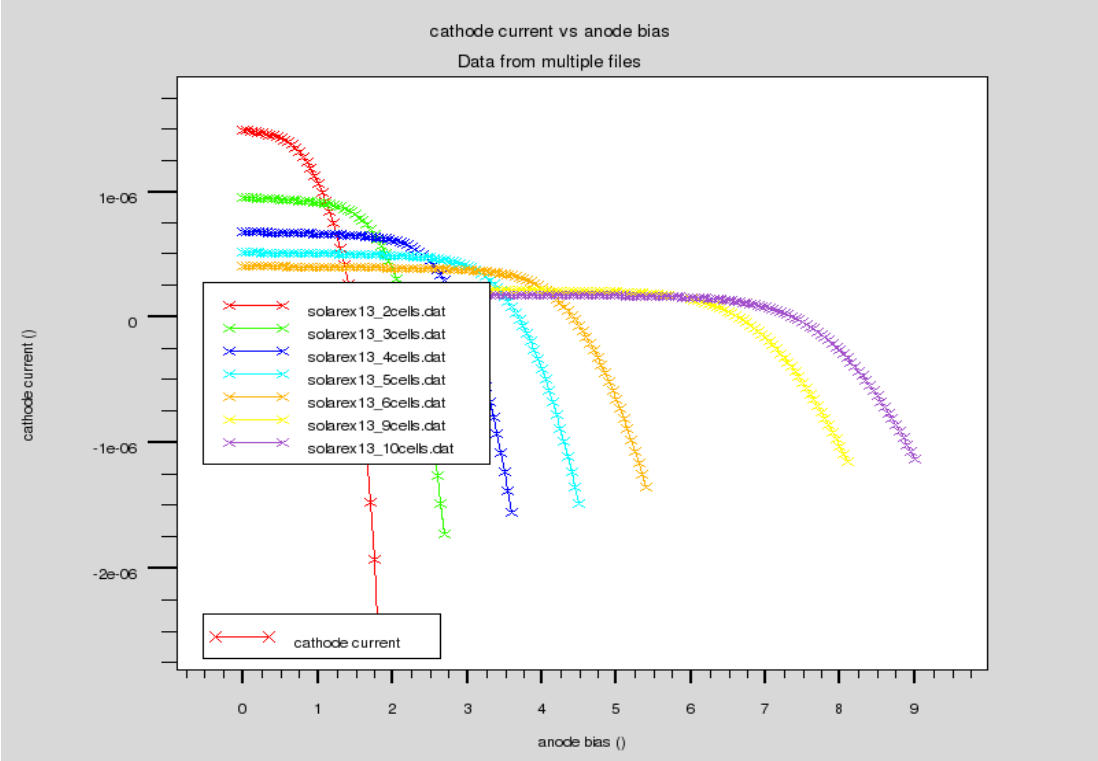


Figure 5.10: J-V Characteristics of Tandem CIGS Solar Cell

Voltage Curve: Figure 5.11 shows Voltage Curve of Tandem CIGS Solar Cell

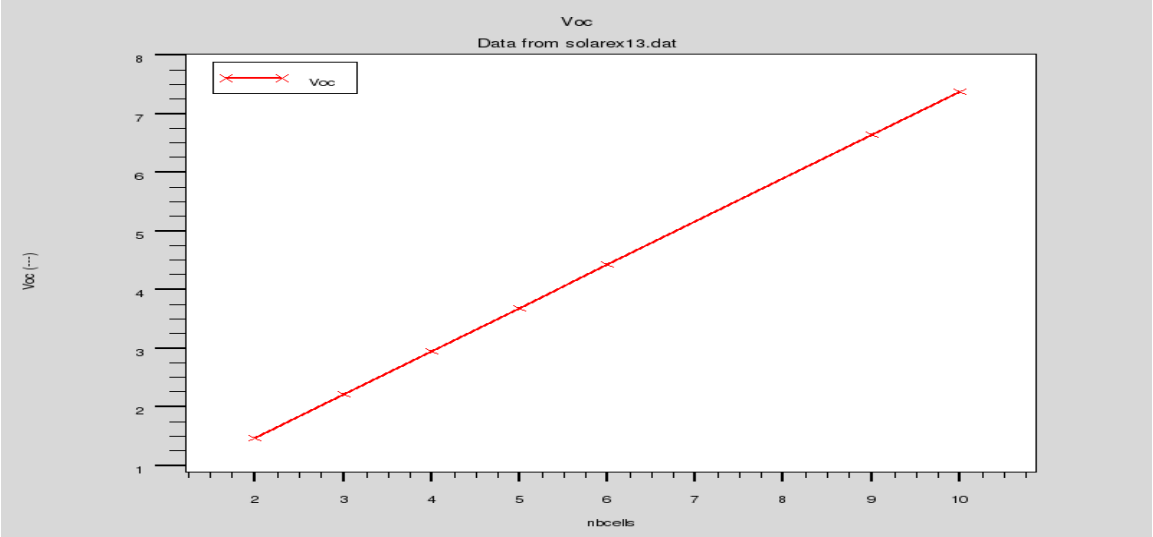


Figure 5.11: Voltage Curve of Tandem CIGS Solar Cell

Fill Factor Curve: Figure 5.12 shows Fill Factor Curve of Tandem CIGS Solar Cell.

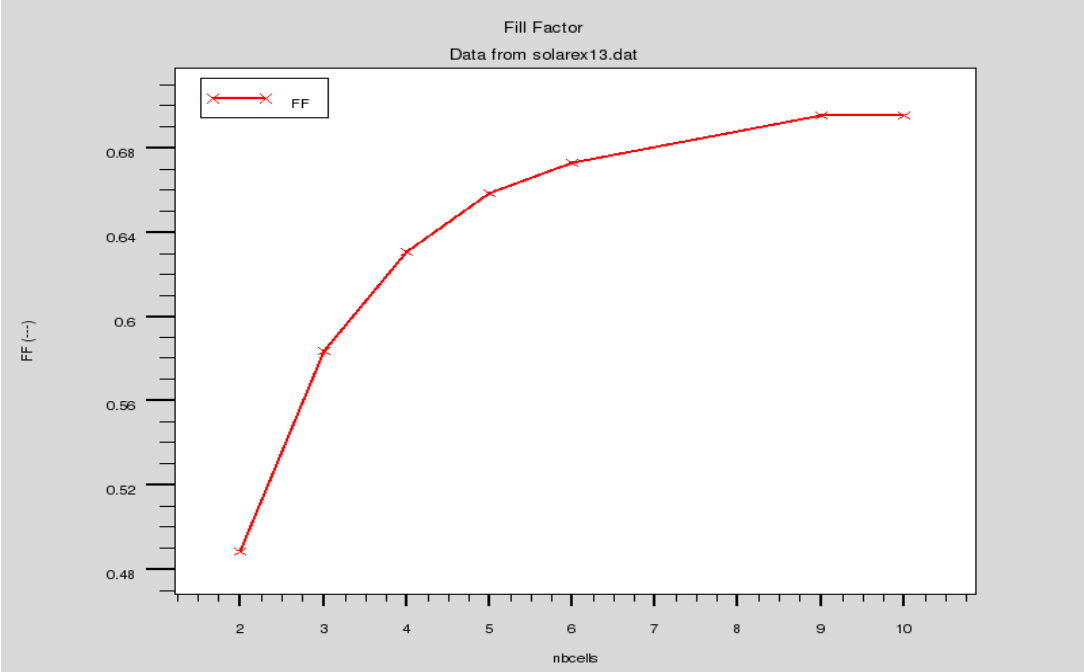


Figure 5.12: Fill Factor Curve of Tandem CIGS Solar Cell

Efficiency Curve: Figure 5.13 shows Efficiency Curve of Tandem CIGS Solar Cell

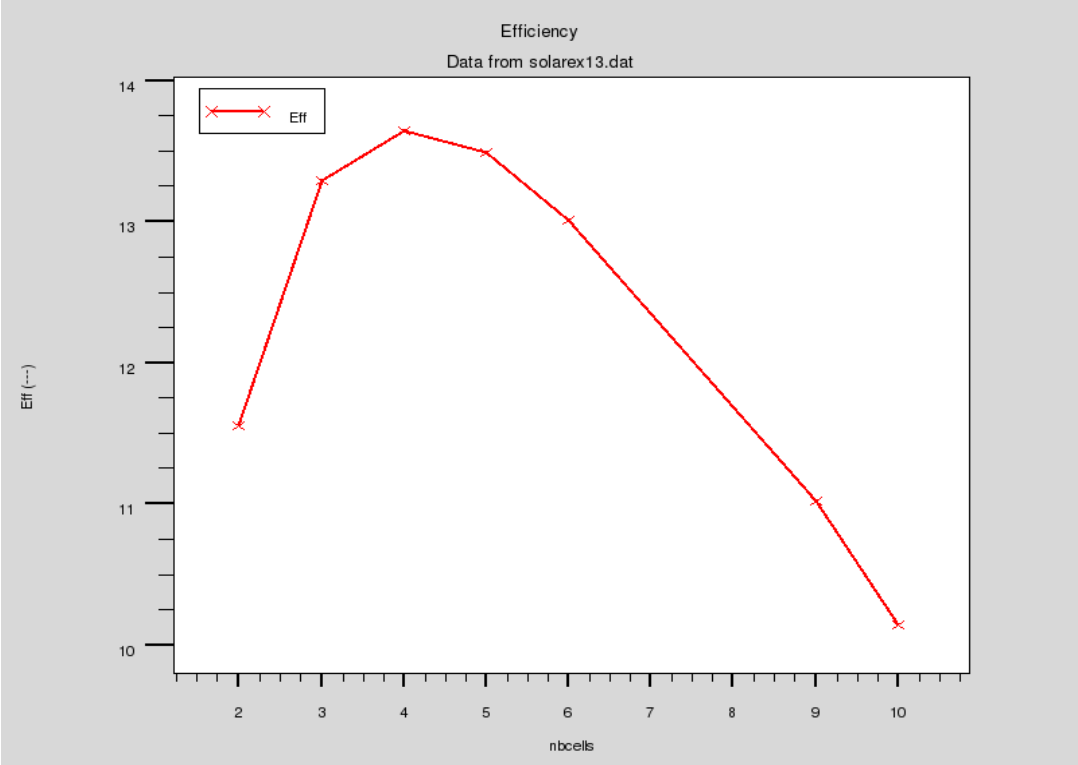


Figure 5.13: Efficiency Curve of Tandem CIGS Solar Cell

Simulation results:

Table 5.3: Extracted Data from Simulation of Tandem CIGS Solar Cell

Parameters	Value
Jsc (mA/cm^2)	13.29
Voc (V)	1.5
Pm(mW/cm^2)	13.75
FF	0.69
Efficiency (%)	13.75

5.2.4. Tandem Silicon Solar Cell with Pyramids and without Pyramids[35]

This shows that solar cell performance is increased by introducing pyramids at the top of the cell. A bell shape is obtained and for this specific case, a pyramid length of around 10um gives the higher efficiency. Simulation results show improvement of performance when pyramids are used.

Structure: Figure 5.14 shows Mesh Structure of Tandem Silicon Solar Cell with pyramids.

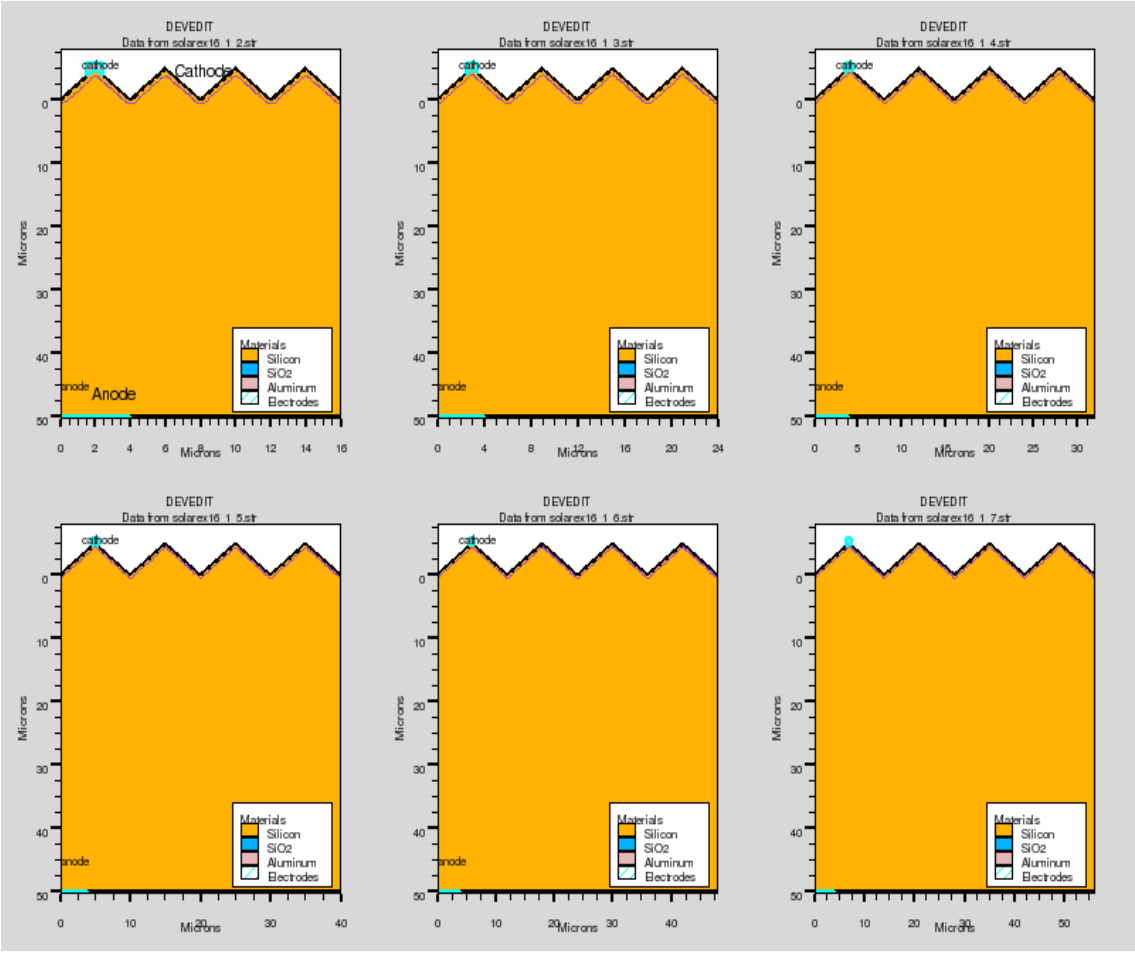


Figure 5.14: Mesh Structure of Tandem Silicon Solar Cell with pyramids

J-V Characteristics: Figure 5.15 shows J-V Characteristics of Tandem Silicon Solar Cell.

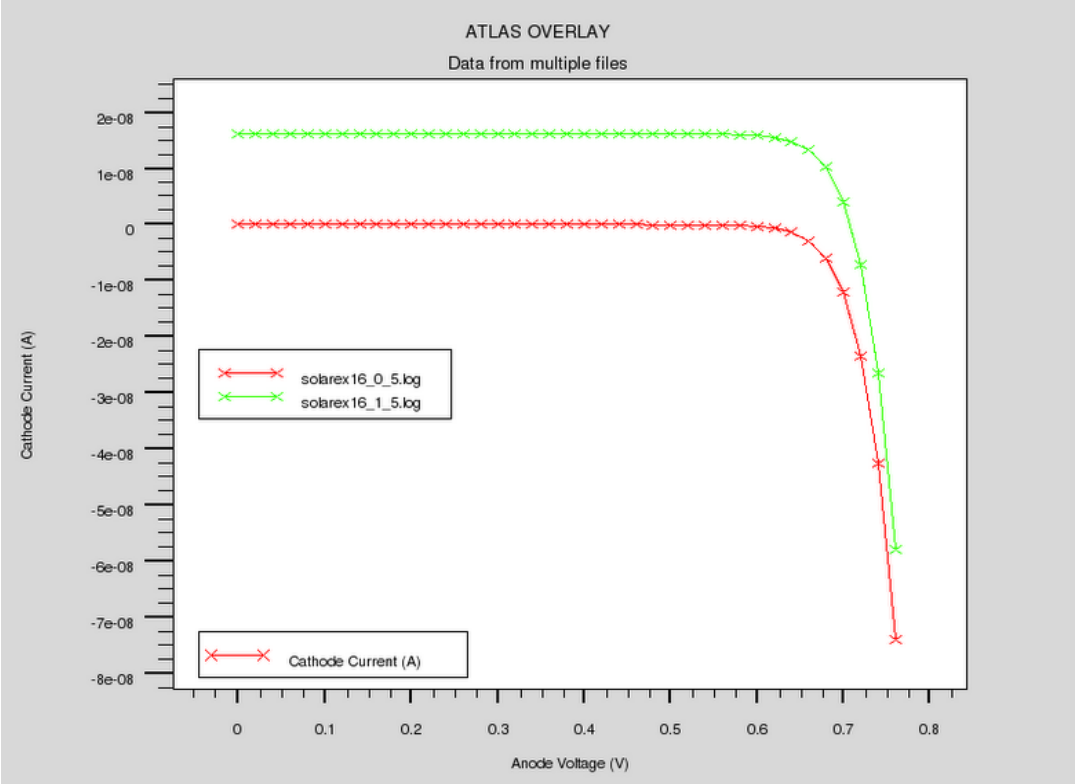


Figure 5.15: J-V Characteristics of Tandem Silicon Solar Cell

Efficiency Curve: Fig 5.16 shows Efficiency Curve of Tandem Silicon Solar Cell.

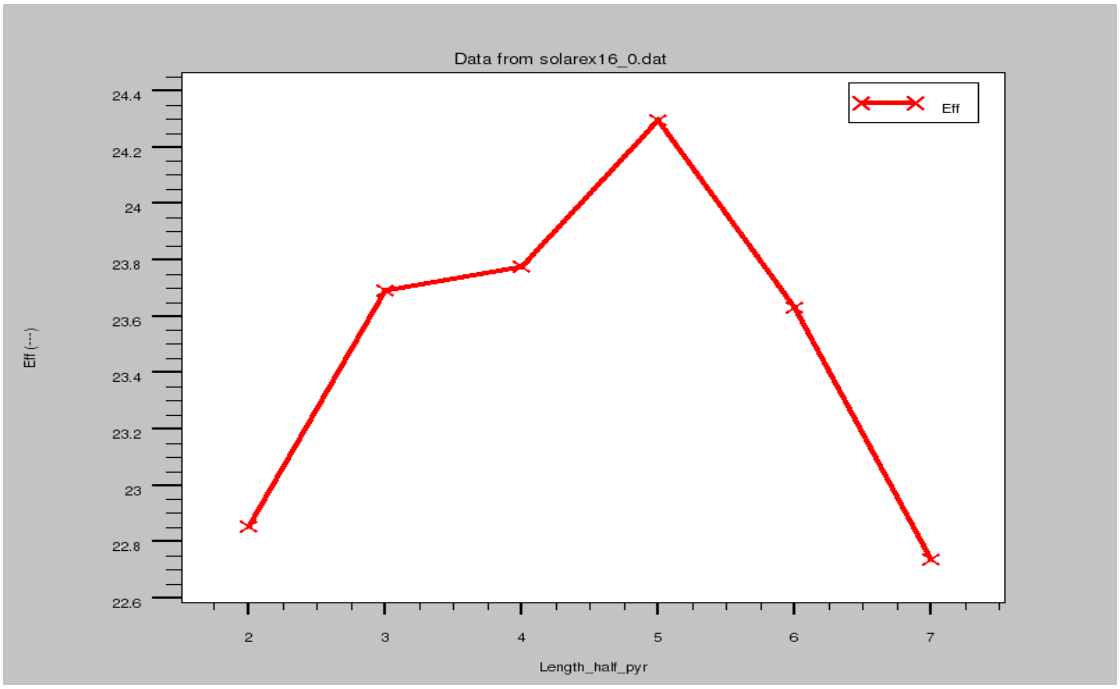


Figure 5.16: Efficiency Curve of Tandem Silicon Solar Cell

Simulation results:

Table 5.4: Extracted Data from Simulation of Tandem Silicon Solar Cell

Parameters	Value
Jsc (mA/cm^2)	34
Voc (V)	0.67
Pm (mW/cm^2)	19.135
FF	0.84
Efficiency (%)	19.135

(a) without Pyramids

Parameters	Value
Jsc (mA/cm^2)	40
Voc (V)	0.70
Pm (mW/cm^2)	24
FF	0.84
Efficiency (%)	24

(b) with Pyramids

5.3. Comparative Performance Analysis

Table5.5: Data Comparison

Parameters	Thin film tandem	Tandem CIGS	Tandem Si with pyramids
Jsc (mA/cm^2)	10.21	13.29	40
Voc (V)	1.356	1.5	0.70
FF	0.7194	0.69	0.84
Efficiency (%)	9.96	13.75	24

5.4. Observations from Simulation Results

From the simulation result following observations are made for tandem thin film solar cell of different materials:

Multi-junction solar cell has better efficiency than single junction solar cell,so we have analyzed multi-junction solar cell.

The short circuit current in thin film tandem is larger than tandem CIGS.Also the open circuit voltage and efficiency increase in tandem CIGS but fill factor decreases in tandem CIGS.

For the simulation of Tandem silicon solar cell with pyramids:

The short circuit current, Fill factor and Efficiency are better than other two tandem cells. Only the open circuit voltage is worse than the other two.

5.5. CAD Design Analysis

Figure 5.17,Figure 5.18,Figure 5.19,Figure 5.20,Figure 5.21 and Figure 5.22 represent the front view, left angle view,back view,right angle view,right side view and top view of CAD design of the solar tracking project structure, respectively which will give us a clear idea about the dual-axis tracker structure.

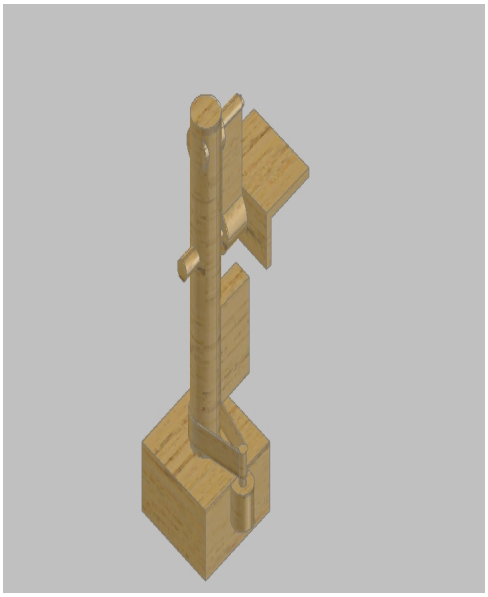


Figure 5.17: Front View

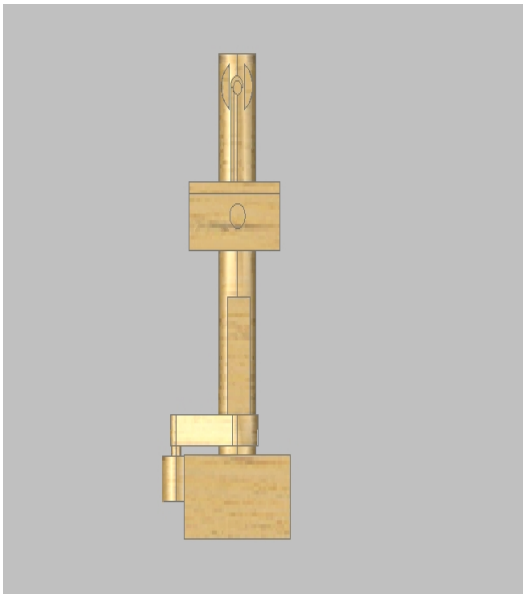


Figure 5.18: Left Angle View

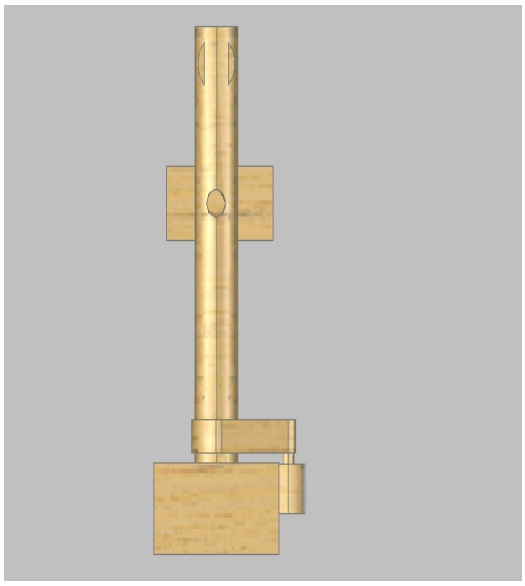


Figure 5.19:Back View

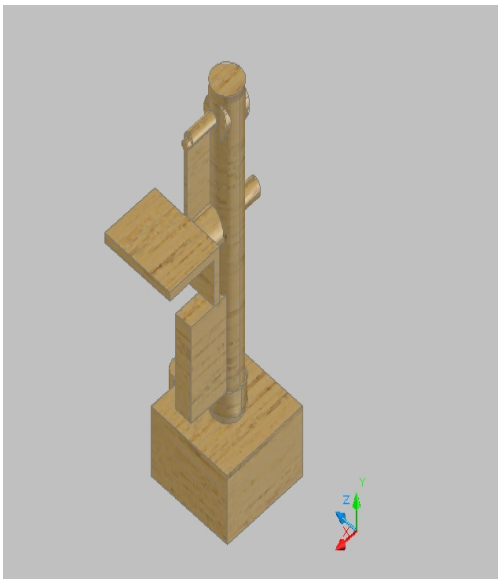


Figure 5.20: Right Angle View

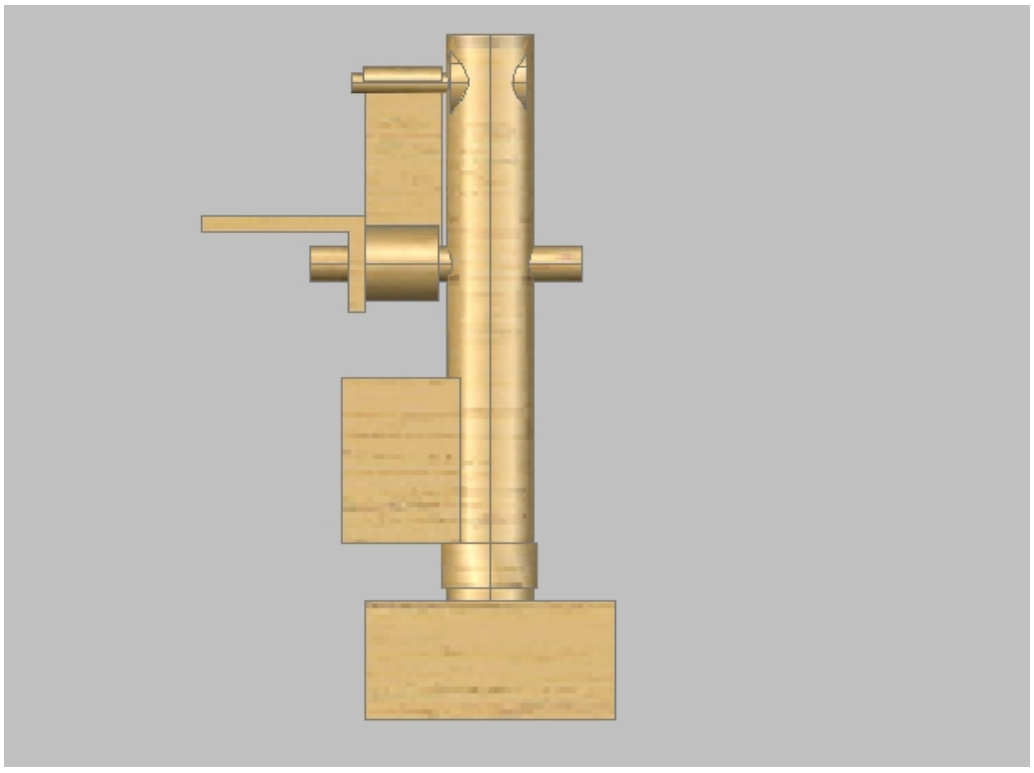


Figure 5.21: Right Side View

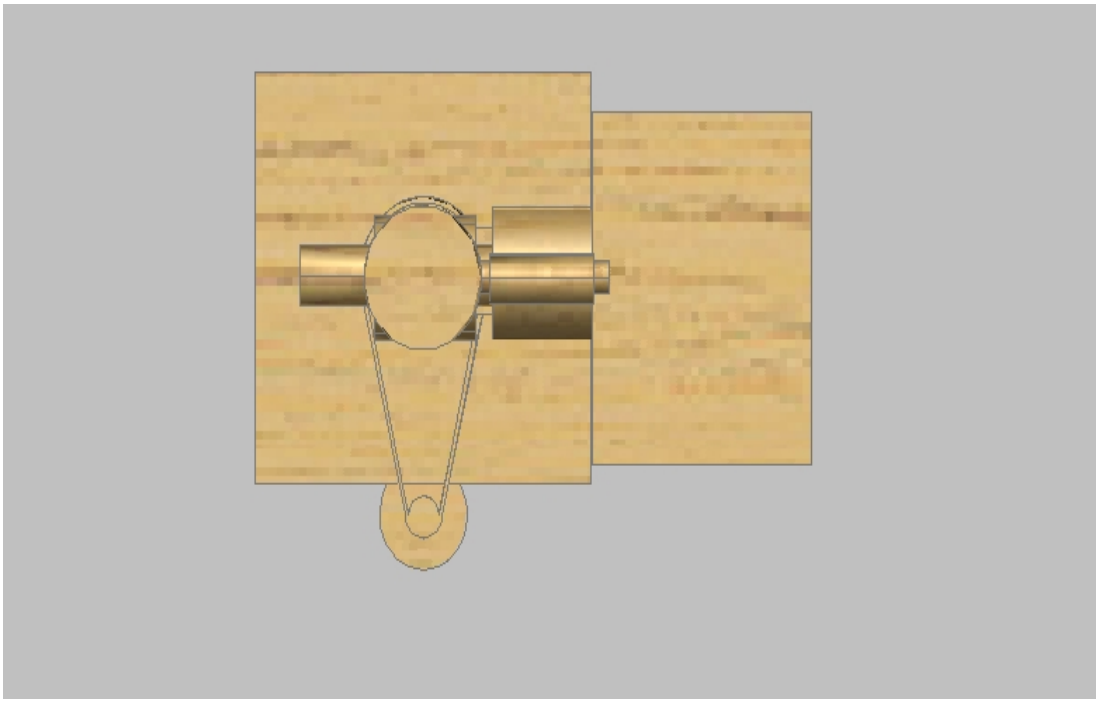


Figure 5.22: Top View

5.6. Structure in reality at different positions

Structure:

In this model solar tracking system there are 3 units .

They are-

a) A detector unit for detecting the surface angle, through which sun light coming to panel.
b) A Mechanical unit works for mechanical supports and all movement of solar panel.
c) A control unit to control mechanical motion and all other internal processing.

The equipments used in each unit are given below:

Detector Unit: In the structure of dual-axis solar panel 4 LDR sensors have been used. LDRs sense presence of light and transform it into voltage signal according to intensity of light. Two among the four LDRs are used for the horizontal sensing part & the rest are used for the vertical sensing part.

Mechanical Unit:

Gear Motor:

"Gear motor" refers to a combination of a motor plus a reduction gear train. These are often conveniently packaged together in one unit. The gear reduction (gear train) reduces the speed of the motor, with a corresponding increase in torque.

Two gear motors are used here. One motor rotates the central axis while the other one rotates the solar panel. Both the motors are bipolar.12V supply is used for motor power circuit.

Gear Coupling: Gear coupling have been used so that the motor doesn't have to bear the load of the motor directly.

Control Unit:

FPGA: ALTERA DE2 Educational FPGA board has been used to control the mechanical unit.

Verilog HDL: There are two types of hardware description language. Here, Verilog HDL has been used to operate the FPGA board.

Motor Drive: Motor drive L293D has been used to operate both the motors.

ADC: 4 ADC IC with the model number adc0804lcn is used here.

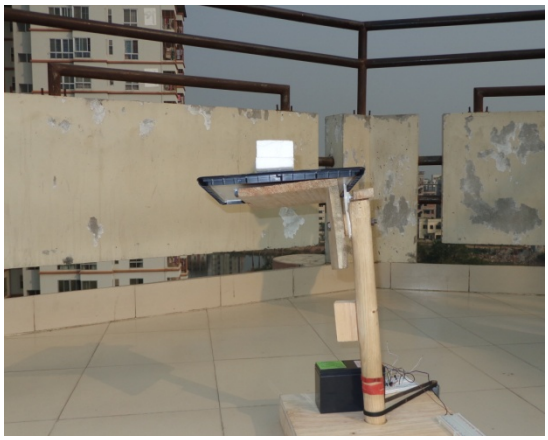


Figure 5.23: Different positions at Different Times of Daylight

Figure 5.24:Different positions at Different Times of Daylight

Figure 5.25: Different positions at Different Times of Daylight

CHAPTER 6

SOLAR TRACKER

6.1. Introduction

We have intended to make an FPGA automated solar tracking system which will hopefully increase the efficiency of the solar panel system available. Although higher initial cost involved we have tried to make the system as much cost effective as possible. This is just the beginning of this kind of implementation using 'FPGA', we can add different enhancements to make the system more more efficient so that it will work round the year.[36]

A device that orients a payload toward the sun is called solar tracker. Payloads can be various objects such as photovoltaic panels, reflectors, lenses or other optical devices. In flat-panel PV applications, we use trackers to minimize the angle of incidence between a photovoltaic panel and incoming sunlight. This increases the amount of energy. In standard photovoltaic applications, trackers are used in approximately 85% of commercial installations greater than 1MW during 2009 - 2012.

Solar trackers are used in concentrated solar thermal (CSP) and concentrated photovoltaic (CPV) applications to enable the optical components in the CPV and CSP systems. In concentrated solar applications it's optics accept the direct component of sunlight and must be appropriately oriented to collect energy. Tracking system are found in all concentrator applications.

6.2. Classification of Solar Tracker

A **solar tracker** can be of two types on the basis of the rotation of it. These two types are:

a) **Single-axis tracker**
b) **Dual-axis tracker**.

These two kind of trackers are discussed in brief at below.

a) Single-axis tracker:

Per day the sun travels through 360 degrees, but from the perspective of any fixed location the visible portion is 180 degrees during an average half day period (slightly more in spring and summer; slightly less, in fall and winter). After considering the Local horizon effects the effective motion becomes about 150 degrees. Between the dawn and sunset extremes a solar panel in a fixed orientation will see a motion of 75 degrees to either side, and thus, according to the table above, will lose 75% of the energy in the morning and evening. By rotating the panels to the east and west we can help recapture those losses. A tracker rotating in the east-west direction is known as a **Single-axis tracker**.

Single axis trackers have one degree of freedom that acts as an axis of rotation. The axis of rotation of single axis trackers is typically aligned along a true North meridian. It is possible to align them in any cardinal direction with advanced tracking algorithms. Some types are:

a) Horizontal single axis tracker (HSAT)
b) Vertical single axis tracker (VSAT)
c) Tilted single axis tracker (TSAT)
d) Polar aligned single axis trackers (PASAT)

Figure 6.1 and Figure 6.2 show Horizontal single axis tracker in California and Linear horizontal axis tracker in South Korea respectively.

Figure 6.1 : Horizontal single axis tracker in California [37]

Figure 6.2 : Linear horizontal axis tracker in South Korea.[38]

b) Dual-axis tracker

The sun also moves through 46 degrees north and south during a year. The same set of panels set at the midpoint between the two local extremes will thus see the sun move 23 degrees on either side, causing losses of 8.3% A tracker that accounts for both the daily and seasonal motions is known as a **Dual-axis tracker**.

Generally speaking, the losses due to seasonal angle changes is complicated by changes in the length of the day, increasing collection in the summer in northern or southern latitudes. This biases collection toward the summer, so if the panels are tilted closer to the average summer angles, the total yearly losses are reduced compared to a system tilted at the spring/fall solstice angle (which is the same as the site's latitude).

There is considerable argument within the industry whether the small difference in yearly collection between single and dual-axis trackers makes the added complexity of a two-axis tracker worthwhile. A recent review of actual production statistics suggested the difference was about 4% in total, which was far less than the added costs of the dual-axis systems. But still we can be hopeful about the future that the Dual-axis tracker will become cost effective.

Dual axis trackers have two degrees of freedom that act as axes of rotation. These axes are typically normal to one another. The axis that is fixed with respect to the ground can be considered a primary axis. The axis that is referenced to the primary axis can be considered a secondary axis. Some types are:

a) Tip–tilt dual axis tracker (TTDAT)
b) Azimuth-altitude dual axis tracker (AADAT)

Figure 6.3 shows Azimuth-altitude dual axis tracker - 2 axis solar tracker at Toledo in Spain.

Figure 6.3 :Azimuth-altitude dual axis tracker - 2 axis solar tracker, Toledo, Spain.[39]

6.3. Types of Solar Collector

Different types of solar collector and their latitude require different types of tracking mechanism. Solar collectors may be:

a) non-concentrating flat-panels, usually photovoltaic or hot-water,
b) concentrating systems, of a variety of types.

Solar collector mounting systems may be

a) Fixed (manually aligned) or
b) Tracking

6.3.1. Tracking System

Tracking systems may be configured as:

a) Fixed collector / moving mirror

b) Moving collector

Fixed mount

Domestic and small-scale commercial photovoltaic panels are usually fixed, often flush-mounted on an appropriately facing pitched roof. Advantages of fixed mount systems include the following:

i) Mechanical simplicity

ii) Tolerance to misalignment

iii) Indirect light

iv) Wind-loading

Floating ground mount

Solar trackers can be built using a “floating” foundation, which sits on top of the ground without the need for invasive concrete foundations.

Fixed collector / moving mirror

Many collectors cannot be moved, for example high-temperature collectors where the energy is recovered as hot liquid or gas. In such cases it is necessary to employ a moving mirror so that, regardless of where the Sun is positioned in the sky, the Sun's rays are redirected onto the collector.

Due to the complicated motion of the Sun across the sky, and the level of precision required to correctly aim the Sun's rays onto the target, a heliostat mirror generally employs a dual axis tracking system, with at least one axis mechanized. In different applications, mirrors may be flat or concave.

Moving collector

Trackers can be grouped into classes by the number and orientation of the tracker's axes. Compared to a fixed mount, a single axis tracker increases annual output by approximately 30% , and a dual axis tracker an additional 6%.

6.4. Drive Types

There are some drive types, namely:

a) Active tracker
b) passive tracker
c) Chronological tracker

Trackers add cost and maintenance to the system - if they add 25% to the cost, and improve the output by 25%, the same performance can be obtained by making the system 25% larger, eliminating the additional maintenance.

CHAPTER 7

FPGA AND VERILOG

7.1. FPGA

7.1.1. Introduction

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing—hence it is called field programmable. Also, Field Programmable Gate Array (FPGA) is digital integrated circuit (IC) that contain Configurable (programmable) blocks of logic along with configurable (programmable) interconnects between these blocks. Most of FPGAs are SRAM-based.[40]

Design Engineer configures (programs) this device to perform a tremendous variety of tasks. Depending on the way they are implemented, some FPGAs may only be programmed a single time, while others may be programmed over and over again. “Field programmable” portion of FPGA’s name refers to the fact that its programming takes place “in the field”, which means that FPGA is configured in the laboratory.

Figure 7.1 shows FPGA Fabric

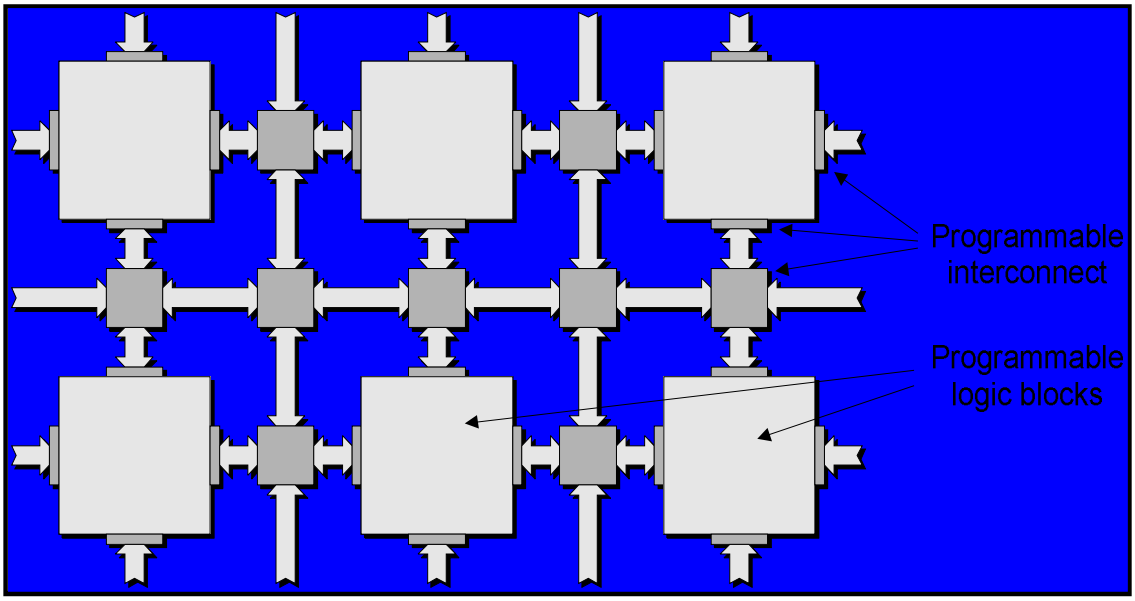


Figure 7.1: FPGA Fabric

7.1.2. Characteristics of FPGA

Some characteristics of FPGA are:

a) Not necessarily reprogrammable (anti-fuse, encryption)
b) Contains programmable logic
c) A “software PCB”
d) Number of Logic Cells (number of 4-input LUT’s and associated flip-flop).
e) Number (and size) of embedded RAM blocks.
f) Number (and size) of embedded Multipliers.
g) Number (and size) of embedded adders.
h) Number (and size) of MACs.
i) Availability of Hardware embedded Microprocessor Cores.
j) Number of I/O pins.

7.1.3. Basic Elements of FPGA

Normally FPGAs comprise of:

a) Programmable logic blocks which implement logic functions.
b) Programmable routing that connects these logic functions.
c) I/O blocks that are connected to logic blocks through routing interconnect and that make off-chip connections.

7.1.4. Anatomy of FPGA

a) A Xilinx Logic CELL:

The core building block in a modern FPGA from Xilinx is called *Logic CELL (LC)*. Figure7.2 shows Simplified View of a Xilinx LC.

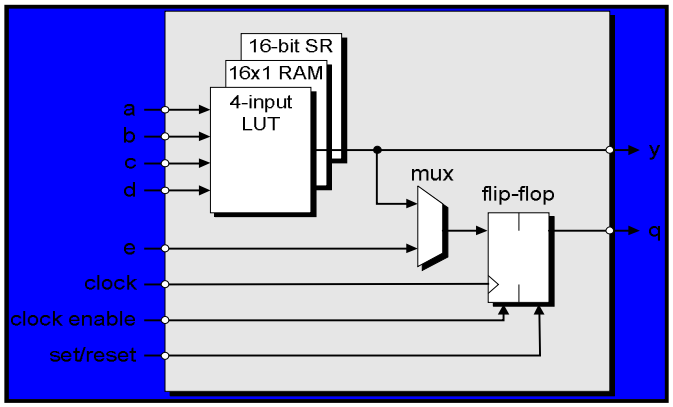


Figure7.2: Simplified View of a Xilinx LC

b) SLICE:

The next step up the hierarchy is the *Slice*. A Slice contains two Logic Cells. Figure 7.3 shows A Slice containing two Logic Cells.

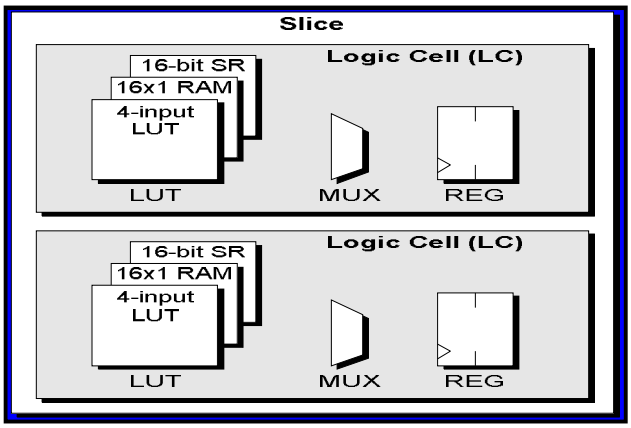


Figure7.3: A Slice containing two Logic Cells

c) Configurable Logic Blocks (CLBs):

One more up level of the slice is the CLB.CLB is a single configurable logic block connected to other CLBs using programmable interconnect. Each CLB can contain two or four slices. Figure7.4 shows CLB containing four Slices.

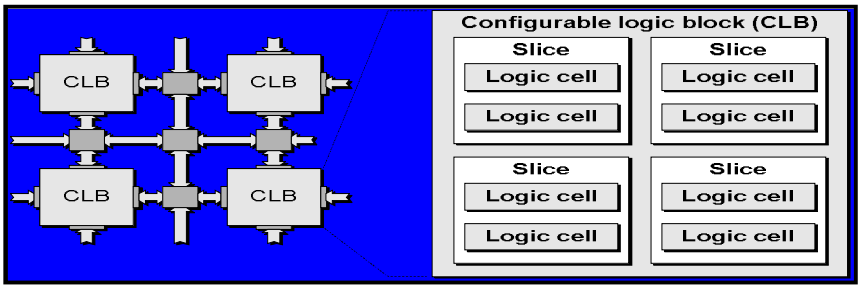


Figure7.4: CLB containing four slices

The logic block hierarchy is as follow:

LC → Slice (2 LC) → CLB (4 slices)

the fastest interconnect is between LCs in the slice, then slightly slower is the interconnects between slices in CLB, followed by the interconnects between CLBs.

d) **Embedded RAMs:**

A lot of applications require the use of memory. FPGA includes a relatively large chunk of embedded RAM called e-RAM or block RAM. The capacity of the block RAM can be varied from few hundred thousand bits to several million bits depending on the chip. The block can be used for a variety of purposes. Figure7.5 shows FPGA with columns of embedded RAM blocks

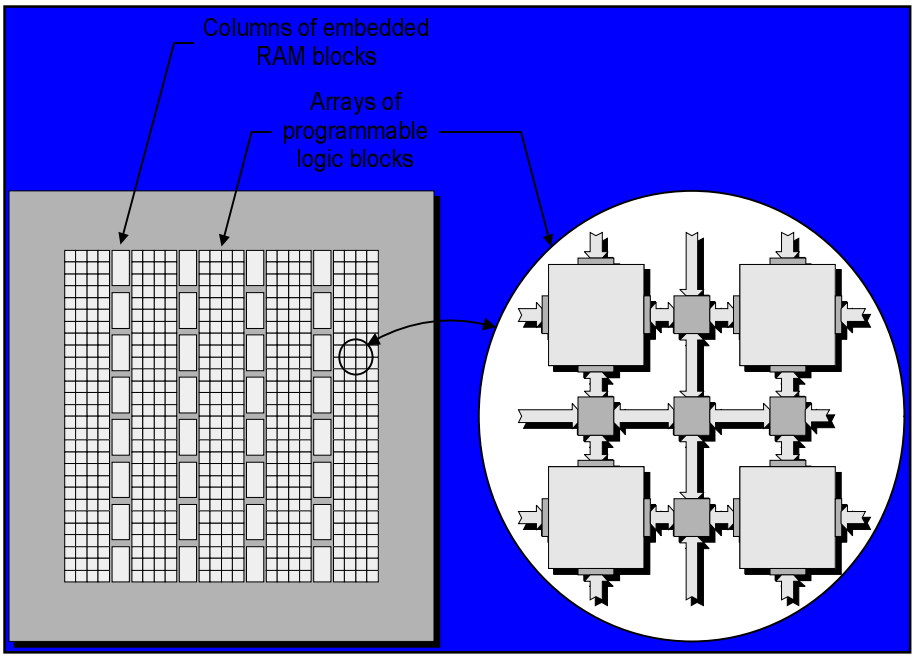


Figure7.5: FPGA with columns of embedded RAM blocks

e) Embedded Multipliers, Adders, MACs etc:

Some functions like multipliers are slow if they are implemented by connecting a large number of programmable logic blocks together, therefore many FPGA incorporate special hardwired multiplier blocks. Figure7.6 shows Columns of embedded RAM and Multipliers.

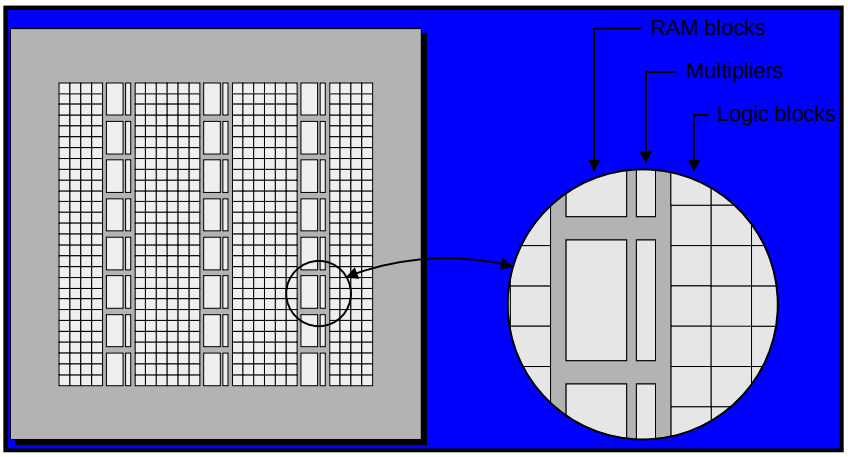


Figure7.6: Columns of embedded RAM and Multipliers

Some FPGAs provide imbedded adder blocks, and it may include and imbedded MAC (Multiply and Accumulate). Figure7.7 shows the functions forming the MAC.

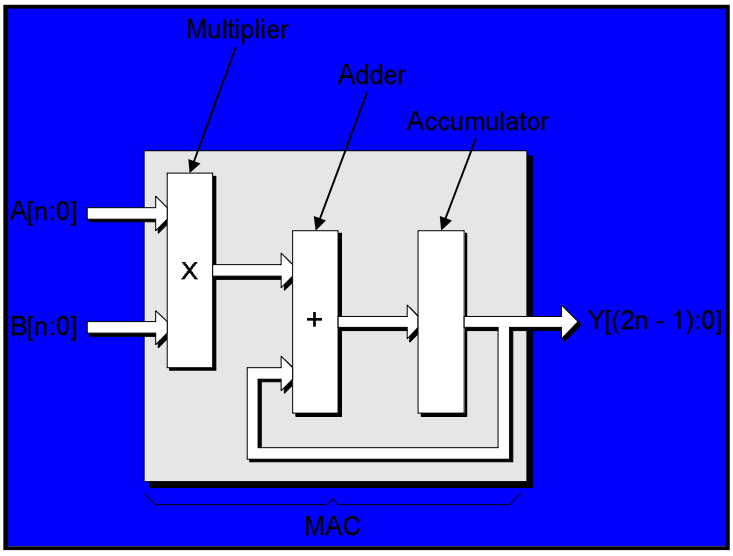


Figure7.7: The functions forming the MAC

f) **Embedded Processor Cores:**

Some FPGA also have in addition to RAM, Multipliers, a Hard Embedded Microprocessor. The embedded Microprocessor core can be outside the main fabric. Figure7.8 shows Simple Clock Tree.

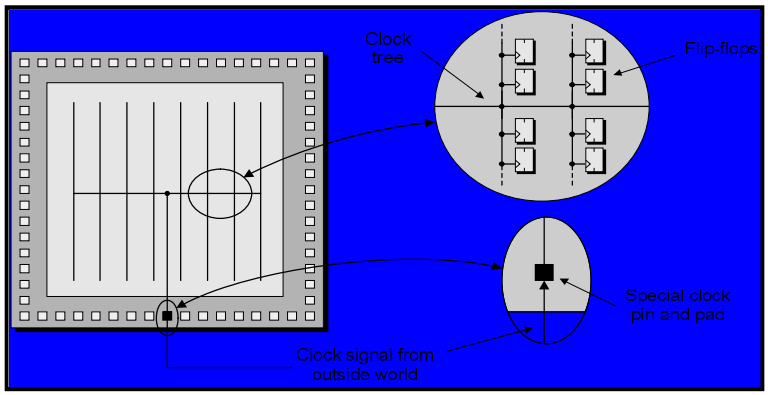


Figure7.8: Simple Clock Tree

When connecting many *flip-flops* one after another to the clock, a *skew* appears. Instead of configuring the clock pin to connect directly to clock tree, The Clock can be used to drive a special block usually called *Digital Clock Manager (DCM).* Figure7.9 shows Clock Manager generating daughter clocks. Each family of FPGA has its own type and number of *DCMs.*

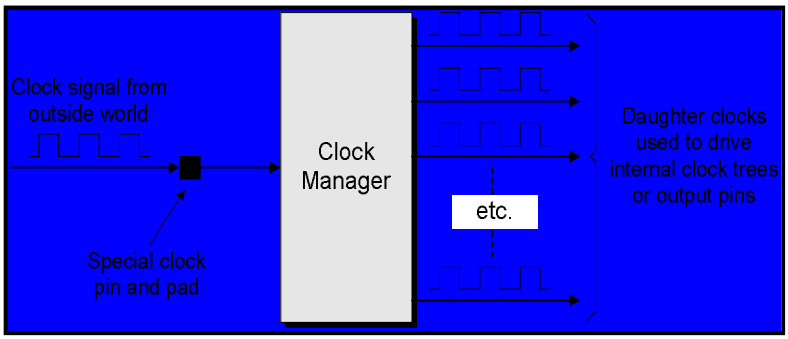
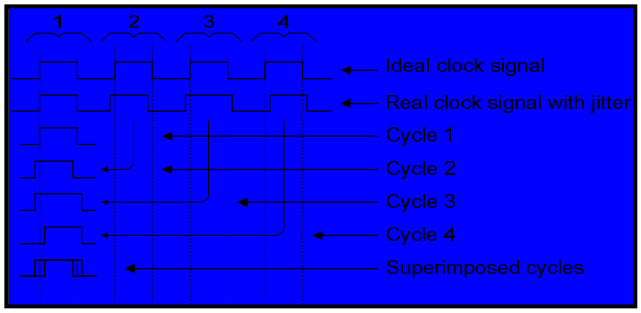


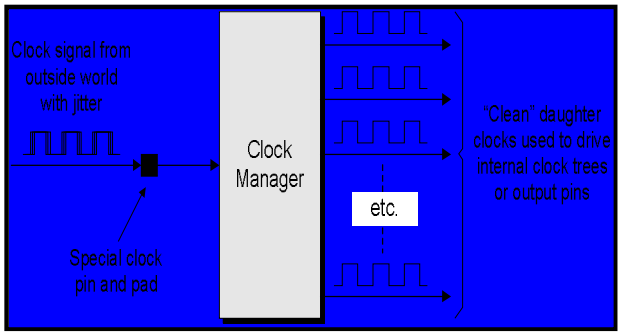
Figure7.9: Clock Manager generating daughter clocks

g) Clock trees and Clock Manager

i) Jitter Removal: Figure7.10 shows jitter removal.



→



Jitter Clock Manager can remove Jitter

Figure7.10: jitter removal

ii) Frequency Synthesis: Figure7.11 shows Frequency Synthesis using Clock Manager.

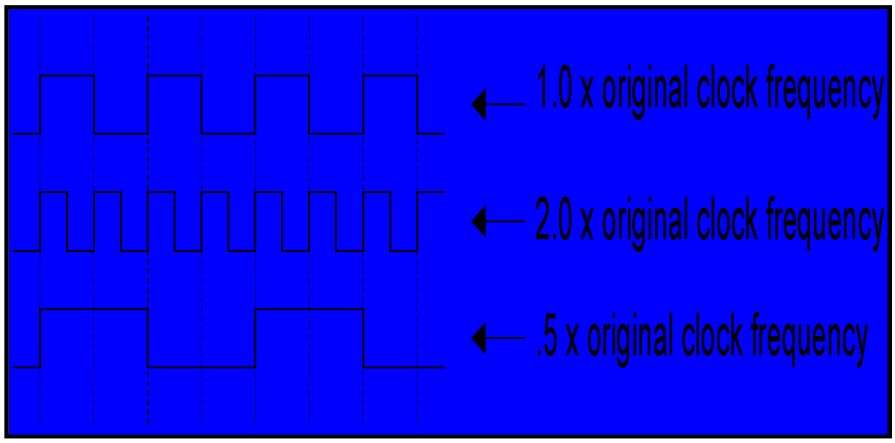


Figure7.11: Using Clock Manager to perform Frequency Synthesis

iii) Phase-Shift the daughter clocks: Figure7.12 shows Using Clock Manager to phase-shift the daughter clocks

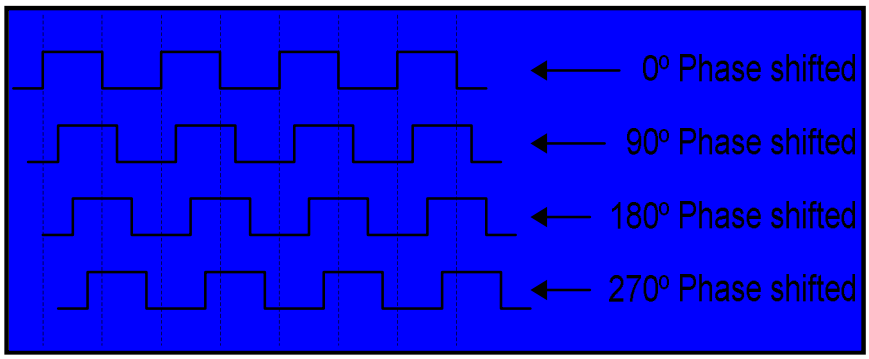


Figure7.12: Using Clock Manager to phase-shift the daughter clocks

h)General-Purpose I/O:

FPGA Packages can have up to 1000 or more pins, arranged across the base of the package. General Purpose I/O signals may be split into a number of Banks. Each Bank can be configured individually to support a particular I/O standard.Figure7.13 shows General Purpose I/O Banks.

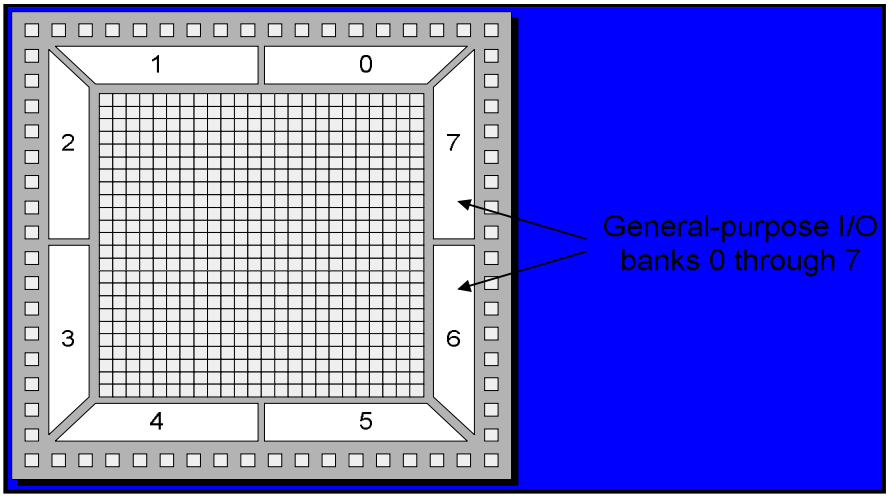


Figure7.13: General Purpose I/O Banks

7.2. Applications of FPGA

FPGA can be used to implement almost anything. FPGAs are currently occupying four major market segments:

a) **ASIC and Custom Silicon:** Today's FPGA can substitute any ASIC and custom silicon.

b) **Digital Signal Processing:** since FPGAs now can contain embedded Multipliers, dedicated Arithmetic routines, large amount of On-Chip RAM, then when all these are connected together it can outperform the fastest DSPs.

c) Embedded Microcontroller: FPGAs are becoming increasingly attractive for embedded control applications.

d) **Physical Layer Communications:** FPGAs are used as a glue logic that interface the physical layers communication chips and high level networking protocols layers.

e) **Reconfigurable Computing:** exploiting the reconfigurability provided by FPGA, several companies are building a huge FPGA-based reconfigurability computing engines for tasks simulation…etc.

7.3. Comparison between FPGA & Microcontroller:

FPGA is mainly for programmable logic but microcontroller is mainly for hard-core processing. Microcontroller is running sequentially regardless of how fast the controller is. In digital signal processor, the hard-core would enhance the hardware architecture by increasing pipelining to certain level of parallel instruction processing. Instead, FPGA is totally hardware based programmable. The parallel processing in FPGA is not depends to the pipelining, but it is hardware based parallel architecture. For general application, microcontroller is good enough for system implementation. However, in some critical arithmetic processing such as DSP algorithm would need real-time processing that is time critical. In this case, FPGA would be the best solution.

FPGA's are merely logic multithreading real time processing chips. For example, a microcontroller features certain set of peripherals like UART, SPI, PWM, Timers, and so on, and they are limited to it. Unless microcontrollers, FPGA don't feature built-in peripherals, instead, peripherals can be logically programmed. That's the power, FPGA are raw logic gates, that means we can make them do anything. For example, programmed to run like being a 1 UART chip, like a 100 channel PWM generators, 20

channel UART controller + 10 ether net, 40 timers, even we can program it to emulate a whole microcontroller or several microcontrollers in a single chip. (Depending on quantity of gates available).In fact FPGA's are often used in PCI bus cards to perform high speed time critical specialized tasks a microcontroller would just couldn't afford due to the architecture of it.

7.4. Verilog:

There are only two standardized and widely used HDLs: Verilog and VHDL.
Verilog began as a proprietary HDL promoted by a company called Cadence Data Systems, Inc., but Cadence transferred control of Verilog to a consortium of companies and universities known as Open Verilog International (OVI). Many companies now produce tools that work with standard Verilog. Verilog is easy to learn. It has a syntax reminiscent of C (with some Pascal syntax thrown in for favour). About half of commercial HDL work in the U.S. is done in Verilog. If we want to work as a digital hardware designer, it is important to know Verilog.

7.4.1. Facts of Verilog

Here are some facts about Verilog:

a) Developed by Gateway Design Automation
b) Bought by Cadence Design Systems
c) Now an IEEE standard : IEEE-1364
d) Pure language definition

7.4.2. Purpose of FPGA

The original purpose of Verilog (and VHDL) was to provide designers a unified language for simulating gate-level net lists. Therefore, Verilog combines a structural notation for describing net lists with a behavioral notation for saying how to test such net lists during simulation. The behavioral notation in Verilog looks very much like normal

executable statements in a procedural programming language, such as Pascal or C. The original reason for using such statements in Verilog code was to provide stimulus to the

66 Verilog Digital Computer Design: Algorithms into Hardware net list, and to test the subsequent response of the net list. The pairs of stimulus and response are known as test vectors. The Verilog that creates the stimulus and observes the response is known as the test code or test bench. For example, one way to use simulation to test whether a small machine works is to do an *exhaustive test*, where the test code provides each possible combination of inputs to the netlist and then checks the response of the netlist to see if it is appropriate.

CHAPTER 8
CONCLUSION AND SUGGESTIONS FOR FUTURE WORKS

8.1. Conclusion

In this thesis, multi-junction PV cells have been analyzed using different materials. From the output of the simulation , it is apparent that the efficiency of multi-junction PV cells varies with the change in material.

In conclusion, though multi-junction yields best performance, by consideration of production cost and ease of fabrication and future improvement, tandem Silicon solar cell with pyramids is an excellent choice for the solution of energy problem.

It has been tried to make an automated solar tracking system using FPGA which will increase the efficiency of the solar panel system . Although there is higher initial cost involved, it has been tried to make the system cost effective .This is just the beginning, different enhancements can be added to make the system more efficient so that it will work around the year.

8.2. Suggestions for future works

Hybrid solar cells combine advantages of both organic and inorganic semiconductors. The hybrid photovoltaic cells have a significant potential for not only low cost but also scalable solar power conversion. So, a very promising approach is hybrid thin film solar cell based on nanostructured silicon and polymer organic semiconductor.

There are always remains an infinite scope of improvement to a system design. Its only the time and financial constraints that impose a limit on the development. Following are the few enhancements that may add further value to the system:

1)During rains, rainfall sensors and a more advanced program can be used to keep the system working.

2)For making the system more reliable fault indicators can be added.

3)The computer and System Control Unit would have a wireless communication with the mechanical structure of solar panel.

4)To make emergency control better more powerful and an advanced FPGA would be used.

5)For small scale production, this model can be used directly, but for mass scale production unnecessary items must be reduced by customization.

6)For mass scale production, only one detector can be used to handle whole panels of the field. This detector will detect horizontal angle as well as vertical angle. For more accuracy some sensors may be added. So it is not required to use 2 or, more sensors with each panel to fix vertical angle.

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APPENDIX

SILVACO Codes Used for Simulations

1)Thin Film Tandem Solar Cell:

```
go atlas

# Structure Generation

mesh

x.m l=0 s=2.5
x.m l=10 s=2.5

y.m l=-0.5 s=10
y.m l=0 s=0.1
y.m l=0.5 s=0.002
y.m l=0.51 s=0.002
y.m l=0.61 s=0.02
……..

region num=1 material=oxide y.min=-0.5 y.max=0

#top cell: a-Si:H
region num=2 silicon y.min=0.5 y.max=0.51 name=a-si
region num=3 silicon y.min=0.51 y.max=0.71 name=a-si
region num=4 silicon y.min=0.71 y.max=0.725 name=a-si

#bottom cell: uc-Si
```

```
region num=5 silicon y.min=0.725 y.max=0.745 name=uc-si
region num=6 silicon y.min=0.745 y.max=2.945 name=uc-si
……..

elec num=1 name=cathode y.min=3.16 y.max=3.36 mat=Aluminum
elec num=2 name=anode y.min=0 y.max=0.5 mat=ZnO
elec num=3 name=com y.min=0.725 y.max=0.735 mat=ITO

doping region=2 uniform p.type conc=1e20
doping region=4 uniform n.type conc=1e20

# IV Simulation

interface optical diffusive dispersion=45 specular=1 scattered=44 \
y.min=0.495 y.max=0.505 absorption=0 region=2
```

tonyplot-overlay solarex12_bottom.dat solarex12_top.dat solarex12_top_exp.dat solarex12_bottom_exp.dat -set solarex12_2.set

"Details are not here".

2) Tandem CIGS Solar Cell:

```
go atlas
mesh auto width=1e12
x.m loc=0 s=1
x.m loc=1 s=1
#
# Here we specify a standard n-p diode in between two electrodes.
# in this case we handle the electrode materials explicitly since
# we want to include their optical properties in the analysis using
```

```
# the transfer matrix method.  The specification of CONDUCTOR means
# we will solve the conduction equation in these regions.
#
region num=1 material=ZnO        bottom thick=0.44 ny=40 conductor
region num=2 material=CdS        bottom thick=0.04 ny=15 donor=1e18
region num=3 material=CIGS       bottom thick=0.36 ny=40 accep=2e16
region num=4 material=Molybdinum bottom thick=0.3  ny=30 conductor
#
# Standare electrode names on top and bottom
#
elec num=1 name=cathode top
elec num=2 name=anode   bottom
……..
tonyplot -overlay solarex13_2cells.dat solarex13_3cells.dat solarex13_4cells.dat
solarex13_5cells.dat solarex13_6cells.dat solarex13_9cells.dat solarex13_10cells.dat
# Efficiency
tonyplot solarex13.dat -set solarex13_2.set
# Jsc
tonyplot solarex13.dat -set solarex13_3.set
# dead/active area
tonyplot solarex13.dat -set solarex13_4.set
# Voc
tonyplot solarex13.dat -set solarex13_5.set
# FF
tonyplot solarex13.dat -set solarex13_6.set
quit
```

“Details are not here.”

3) Tandem Silicon Solar Cell with Pyramids and without Pyramids:

```
go atlas
set Height_pyr=5
set Length_half_pyr=5
set Si_thick=50
set pyramid=1

line x loc=0.00 spac=$Length_half_pyr/5
line x loc=$Length_half_pyr spac=$Length_half_pyr/5

line y loc=0.00          spac=$Si_thick/10
line y loc=$Si_thick     spac=$Si_thick/10

initialize silicon two.d c.boron=7e16

Deposit silicon thickness=$Height_pyr div=10 c.boron=7e16

# If pyramid=0 ==> flat surface. Allow to compare results with pyramid=1
IF cond=($pyramid=1)

etch material=silicon  start x=$Length_half_pyr y=-$Height_pyr
etch                   cont  x=0 y=0
etch                   done  x=0 y=-$Height_pyr

IF.END

structure mirror right

go devedit
```

base.mesh height=2 width=0.5

bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.001 line.straightening=1 align.points when=automatic

constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
max.width=1000 min.height=0.0001 min.width=0.0001
constr.mesh id=1 x1=0 y1=1 x2=$Length_half_pyr*2 y2=-5 default max.height=0.2 max.width=0.2
……
Tonyplot solarex16_1_2.str solarex16_1_3.str solarex16_1_4.str solarex16_1_5.str solarex16_1_6.str solarex16_1_7.str -set solarex16_0.set
tonyplot solarex16_0.dat -set solarex16_1.set
tonyplot -overlay solarex16_0_5.log solarex16_1_5.log
quit

“Details are not here”