Design of a Phase Locked Loop by using 50nm CMOS Technology

This Thesis is submitted to the Department of Electrical, Electronics and Communication Engineering (EECE) of MILITARY INSTITUTE OF SCIENCE AND TECHNOLOGY (MIST) for fulfillment of the course "EECE-400" for the degree of Bachelor of Science in Electrical, Electronics and Communication Engineering.

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Declaration

We hereby declare that the work presented in this thesis has been done by us under the complete supervision of Dr. Pran Kanai Saha, Professor, Department of Electrical and Electronic Engineering, BUET, Dhaka. We also declare that this thesis entitled "**Design of a Phase Locked Loop by using 50nm CMOS Technology**" is a piece of original research work and only done by the members involved for the award of degree or diploma.

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The authors would like to extend their regards to them who directly and indirectly helped them in thesis work.

Abstract

Phase-locked loops are widely employed in radio, telecommunications, computers and other electronic applications. They can be used to demodulate a signal, recover a signal from a noisy communication channel, generate a stable frequency at multiples of an input frequency (frequency synthesis), or distribute precisely timed clock pulses in digital logic circuits such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a hertz up to many gigahertz.

This thesis contains discrete components involving the Phase Detector and Voltage Controlled Oscillator and Filter. The Phase Detector and the Voltage Controlled Oscillator are designed with 50nm CMOS technology. The Filter is designed with microstrip transmission line.

The Phase Detector, Voltage Controlled Oscillator and Band Pass Filter are designed and simulated using the softwares - LTSPICE, HSPICE, ADS. The simulated results are in good agreement. Process Scattering and Temperature variation have been applied in this thesis.

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Chapter 1

Introduction to Digital Communication

1.1 Digital Communication

Communication has been one of the deepest needs of the human race throughout recorded history. It is essential to forming social unions, to educating the young, and to expressing a myriad of emotions and needs. Good communication is central to a civilized society.

The various communication disciplines in engineering have the purpose of providing technological aids to human communication. One could view the smoke signals and drum rolls of primitive societies as being technological aids to communication, but communication technology as we view it today became important with telegraphy, then telephony, then video, then computer communication, and today the amazing mixture of all of these in inexpensive, small portable devices.

Initially these technologies were developed as separate networks and were viewed as having little in common. As these networks grew, however, the fact that all parts of a given network had to work together, coupled with the fact that different components were developed at different times using different design methodologies, caused an increased focus on the underlying principles and architectural understanding required for continued system evolution.

This need for basic principles was probably best understood at American Telephone and Telegraph (AT&T) where Bell Laboratories was created as the research and development arm of AT&T. The Math center at Bell Labs became the predominant center for communication research in the world, and held that position until quite recently. The central core of the principles of communication technology was developed at that center.

Perhaps the greatest contribution from the math center was the creation of Information Theory[10] by Claude Shannon in 1948. For perhaps the first 25 years of its existence, Information Theory was regarded as a beautiful theory but not as a central guide to the architecture and design of communication systems. After that time, however, both the device technology and the engineering understanding of the theory were sufficient to enable system development to follow information theoretic principles.

A number of information theoretic ideas and how they affect communication system design will be explained carefully in subsequent chapters. One pair of ideas, however, is central to almost every topic. The first is to view all communication sources, e.g., speech waveforms, image waveforms, and text files, as being represent-able by binary sequences. The second is to design communication systems that first convert the source output into a binary sequence and then convert that binary sequence into a form suitable for transmission over particular physical media such as cable, twisted wire pair, optical fiber, or electromagnetic radiation through space.

Digital communication systems, by definition, are communication systems that use such a digital sequence as an interface between the source and the channel input (and similarly between the channel output and final destination) (see Figure 1.1).
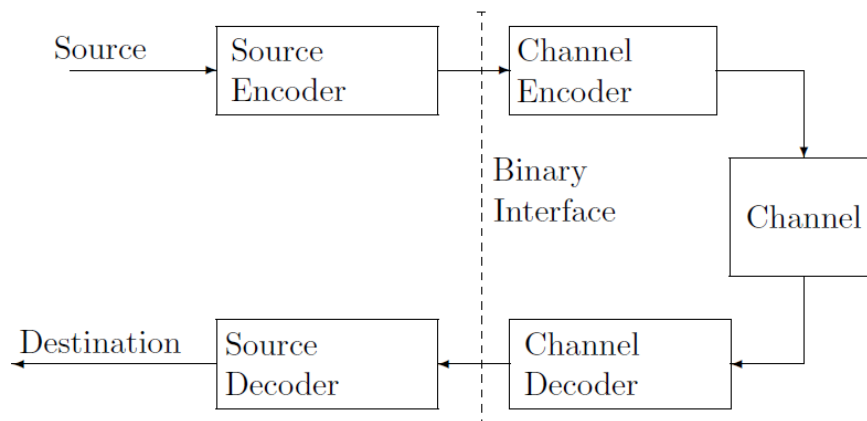
Figure 1.1: Placing a binary interface between source and channel. The source encoder converts the source output to a binary sequence and the channel encoder (often called a modulator) processes the binary sequence for transmission over the channel. The channel decoder (demodulator) recreates the incoming binary sequence (hopefully reliably), and the source decoder recreates the source output.

The idea of converting an analog source output to a binary sequence was quite revolutionary in 1948, and the notion that this should be done before channel processing was even more revolutionary. By today, with digital cameras, digital video, digital voice, etc., the idea of digitizing any kind of source is commonplace even among the most technophobic. The notion of a binary interface before channel transmission is almost as commonplace. For example, we all refer to the speed of our internet connection in bits per second.

There are a number of reasons why communication systems now usually contain a binary interface between source and channel (i.e., why digital communication systems are now

standard). These will be explained with the necessary qualifications later, but briefly they are as follows:

- ➢ Digital hardware has become so cheap, reliable, and miniaturized, that digital interfaces are eminently practical.

- ➢ A standardized binary interface between source and channel simplifies implementation and understanding, since source coding/decoding can be done independently of the channel, and, similarly, channel coding/decoding can be done independently of the source.

- ➢ A standardized binary interface between source and channel simplifies networking, which now reduces to sending binary sequences through the network.

- ➢ One of the most important of Shannon's information theoretic results is that if a source can be transmitted over a channel in any way at all, it can be transmitted using a binary interface between source and channel. This is known as the source/channel separation theorem.

Chapter 2

Components of PLL and their Characteristics

2.1 Transceiver

A transceiver is a device which consists of both a transmitter and a receiver which are joined together into a single circuit. When no connection is made between transmit and receive functions, the device is a transmitter-receiver. Transceivers are combination of handling circuitry of a significant amount of the transmitter and receiver. Example of other devices are transponders, transverters, and repeaters.

2.1.1 Radio technology

In radio terminology, a transceiver is a unit which consists of both a transmitter and a receiver. Amateur radio or "ham" radio operators can build their own equipment and it is now easier to design and build a simple unit containing both of the functions: transmitting and receiving. Almost all modern amateur radio equipment is now a transceiver but there is an active market for pure radio receivers, mainly for shortwave listening (SWL) operators. Examples of transceivers are walkie-talkie, or a CB radio.

2.1.2 RF Transceiver

The RF Transceiver uses Radio Frequency modules for high speed data transmission. The micro-electronic circuits in the digital-RF architecture work at high speeds maxing towards 100 GHz. The main goal in the design was to bring digital architecture closer to the antenna, both at the received and transmitted ends using software defined radio. The circuits with software-programmable digital processors permit conversion between digital baseband signals and analog RF.

2.1.3 Telephony

On a wired telephone, the handset contains the transmitter and receiver for the audio and at present times is usually wired to the base unit by tinsel wire. The whole unit is generally called to as a "receiver." On a mobile phone or other radiotelephone, the entire device is called a transceiver, for both audio and radio.

A cordless phone uses - audio and radio transceiver for the handset, and a radio transceiver in the base station. If a speakerphone is included in the wired telephone base or in a cordless base station, the base also becomes an audio transceiver along with the handset.

A modem functions similar to a transceiver; it sends and receives a signal, but a modem uses modulation and demodulation. It modulates a signal being transmitted and demodulates a signal being received.

2.1.4 The Ring Oscillator

The odd number of inverters in the circuit shown in Fig.(2.1) forms a closed loop with positive feedback and is called a ring oscillator. The oscillation frequency is given by, [1]

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})} \qquad \text{... (2.1)}$$

Assuming that the inverters are identical and n is the number (odd) of inverters in the ring oscillator. Since the ring oscillator is self-starting, it is often added to a test portion of a wafer to indicate the speed of a particular process run. The sum of the high-to-low and low-to-high delays is used to calculate the period of the oscillation because each inverter switches twice during a single oscillation period.
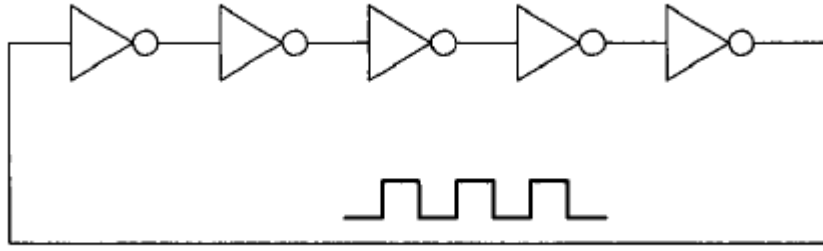
Figure 2.1: A five-stage ring oscillator.[1]

When identical inverters are used the capacitance on the inverter's input/output is the sum of an inverter's input capacitance with the inverter's output capacitance,

$$C_{tot} = \overbrace{C_{oxp} + C_{oxn}}^{C_{out}} + \overbrace{\frac{3}{2} \cdot (C_{oxp} + C_{oxn})}^{C_{in}} = \frac{5}{2} \cdot (C_{oxp} + C_{oxn})_s \qquad \dots (2.2)$$

Where again,

$$C_{oxp} = C'_{ox} \cdot W_p \cdot L_p \cdot (scale)^2 \quad \text{and} \quad C_{oxn} = C'_{ox} \cdot W_n \cdot L_n \cdot (scale)^2 \qquad \dots (2.3)$$

The delays then calculated using,

$$t_{PHL} + t_{PLH} = 0.7 \cdot (R_n + R_p) \cdot C_{tot} \qquad \dots (2.4)$$

2.1.5 Microstrip Transmission Line

Microstrip transmission line is the most used planar transmission line in Radio frequency (RF) applications. The planar configuration can be achieved by several ways, for example with the photolithography process or thin-film and thick film technology. As other transmission line in RF applications, microstrip can also be exploited for designing certain components, like filter, coupler, transformer or power divider.

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If a microstrip transmission line, as depicted in Fig. (2.2), is used for transport of wave with relative low frequency, the wave type propagating in this transmission line is a quasi-TEM wave. This is the fundamental mode in the microstrip transmission line.
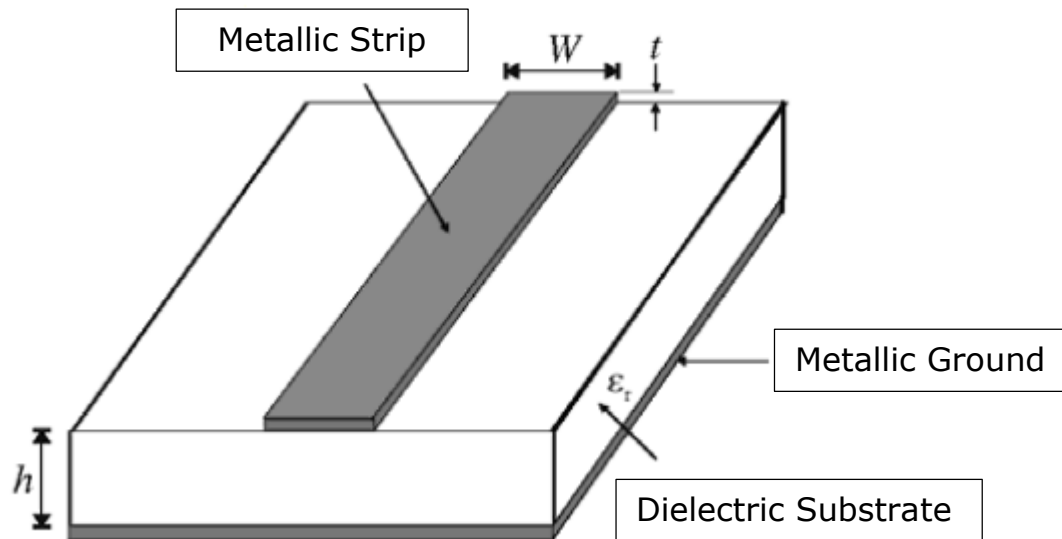
Figure 2.2: Microstrip transmission line. [1]

The width of the strip W together with the dielectric constant and the thickness of the substrate determine the characteristic impedance Z_o of the line.

2.2 Phase locked loop

The phase locked loop or PLL is a particularly flexible circuit building block.

The phase locked loop, PLL can be used for a variety of radio frequency applications, from frequency synthesizers to clock recovery and FM demodulation.

As a result the phase locked loop is found in many items of radio frequency equipment including radio receivers, test equipment and other items of radio frequency electronics.
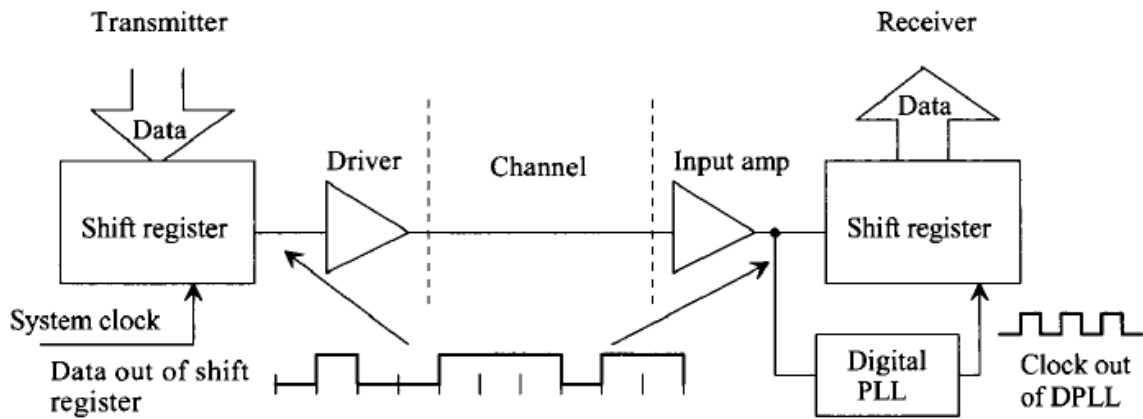
Figure 2.3: Block diagram of a communication system using a DPLL for the generation of a clock signal. [1]

2.2.1 Phase locked loop development

The phase locked loop, PLL, was not used in early radio equipment because of the number of different stages required. However with the advent of radio frequency integrated circuits, the idea of phase locked loops, PLLs, became viable. Initially relatively low frequency PLLs became available, but as RF IC technology improved, so the frequency at which PLLs would operate rose, and high frequency versions became available.

Phase locked loops are used in a large variety of applications within radio frequency technology. PLLs can be used as FM demodulators and they also form the basis of indirect frequency synthesizers. In addition to this they can be used for a number of applications including the regeneration of chopped signals such as the color burst signal on an analogue color television signal, for types of variable frequency filter and a host of other specialist applications

2.2.2 Phase locked loop concepts - phase

The operation of a phase locked loop, PLL, is based around the idea of comparing the phase of two signals. This information about the error in phase or the phase difference between the two signals is then used to control the frequency of the loop. To understand more about the concept of phase and phase difference, first visualize a radio frequency signal in the form of a familiar x-y plot of a sine wave. As time progresses the amplitude oscillates above and

below the line, repeating itself after each cycle. The linear plot can also be represented in the form of a circle. The beginning of the cycle can be represented as a particular point on the circle and as a time progresses the point on the waveform moves around the circle. Thus a complete cycle is equivalent to 360° or 2π radians. The instantaneous position on the circle represents the phase at that given moment relative to the beginning of the cycle.
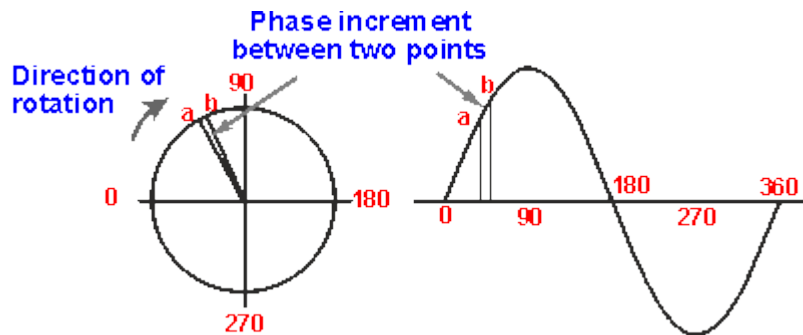
Figure 2.4: Phase increment on a signal

To look at the concept of phase difference, take the example of two signals. Although the two signals have the same frequency, the peaks and troughs do not occur in the same place. There is said to be a phase difference between the two signals. This phase difference is measured as the angle between them. It can be seen that it is the angle between the same point on the two waveforms. In this case a zero crossing point has been taken, but any point will suffice provided that it is the same on both.
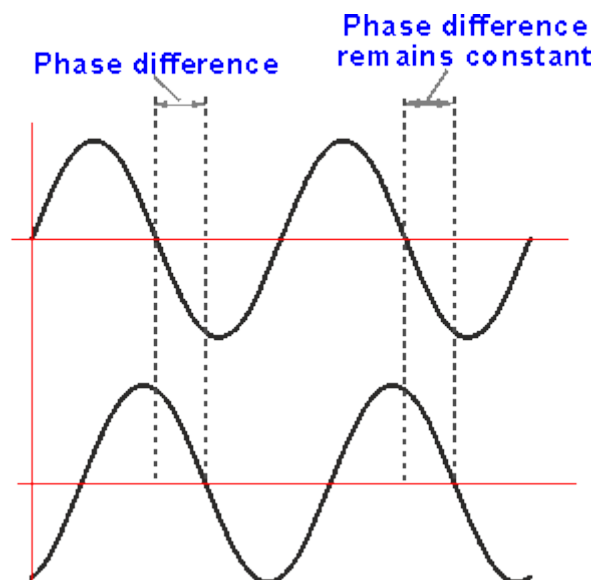
Figure 2.5: Phase difference between signals

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When there two signals have different frequencies it is found that the phase difference between the two signals is always varying. The reason for this is that the time for each cycle is different and accordingly they are moving around the circle at different rates.

It can be inferred from this that the definition of two signals having exactly the same frequency is that the phase difference between them is constant. There may be a phase difference between the two signals. This only means that they do not reach the same point on the waveform at the same time. If the phase difference is fixed it means that one is lagging behind or leading the other signal by the same amount, i.e. they are on the same frequency.

2.3 Phase locked loop components

A phase locked loop, PLL, is basically of form of servo loop. Although a PLL performs its actions on a radio frequency signal, all the basic criteria for loop stability and other parameters are the same.
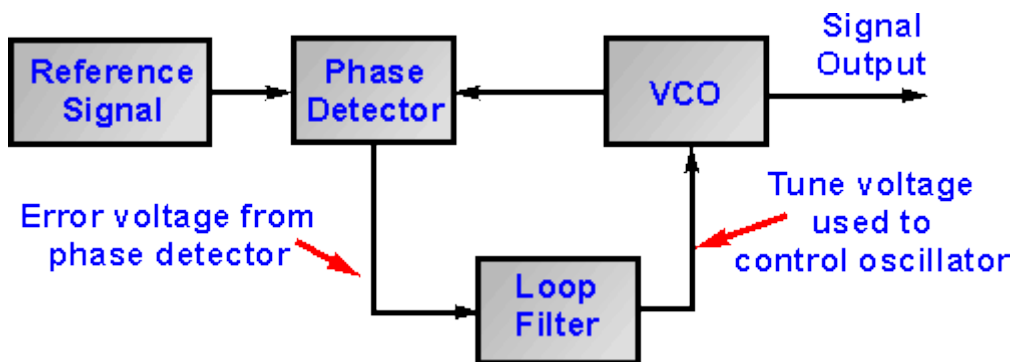
Figure 2.6: Phase locked loop basic diagram

A basic phase locked loop, PLL, consists of three basic elements:

➢ *Phase comparator / detector:* As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals.

➢ *Loop filter:* This filter is used to filter the output from the phase comparator in the PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line. It also governs many of the characteristics of the loop and its stability.

> *Voltage controlled oscillator (VCO):* The voltage controlled oscillator is the circuit block that generates the output radio frequency signal. Its frequency can be controlled and swung over the operational frequency band for the loop.

2.4 Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation can become more complicated

The basic phase locked loop is connected as shown in the diagram below. The reference signal and the signal from the voltage controlled oscillator are connected into the phase detector. The output from the phase detector is passed through the loop filter and then applied to the voltage controlled oscillator.

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

The phase locked loop, PLL, is one of the most versatile building blocks in radio frequency electronics today. Whilst it was not widely used for many years, the advent of the IC meant that phase locked loop and synthesizer chips became widely available. This made them cheap to use and their advantages could be exploited to the full.

2.5 PLL Phase Detector / Comparator

The phase detector is the core element of a phase locked loop, PLL. Its action enables the phase differences in the loop to be detected and the resultant error voltage to be produced.

There is a variety of different circuits that can be used as phase detectors, some that use what may be considered as analogue techniques, while others use digital circuitry. However the most important difference is whether the phase detector is sensitive to just phase or whether it is sensitive to frequency and to phase. Thus phase detectors may be split into two categories:

- ➢ Phase only sensitive detectors
- ➢ Phase / frequency detectors

2.5.1 Phase only sensitive detectors

Phase detectors that are only sensitive to phase are the most straightforward form of detector. They simply produce an output that is proportional to the phase difference between the two signals. When the phase difference between the two incoming signals is steady, they produce a constant voltage. When there is a frequency difference between the two signals, they produce a varying voltage.

The difference frequency product is the one used to give the phase difference. It is quite possible that the difference frequency signal will fall outside the pass-band of the loop filter. If this occurs then no error voltage will be fed back to the Voltage Controlled Oscillator (VCO) to bring it into lock. This means that there is a limited range over which the loop can be brought into lock, and this is called the capture range. Once in lock the loop can generally be pulled over a much wider frequency band.

To overcome this problem the oscillator must be steered close to the reference oscillator frequency. This can be achieved in a number of ways. One is to reduce the tuning range of the oscillator so that the difference product will always fall within the pass-band of the loop filter. In other instances another tune voltage can be combined with the feedback from the loop to ensure that the oscillator is in the correct region. This is approach is often adopted in microprocessor systems where the correct voltage can be calculated for any given circumstance.

2.5.2 The XOR Phase Detector

The XOR PD is simply an exclusive OR gate. When the output of the XOR is a pulse train with a 50% duty cycle (square wave), the DPLL is said to be in lock; or in other words, the clock signal out of the DPLL is synchronized to the incoming data, provided the following conditions are met. Consider the XOR PD shown in Fig. 2.7. Let's begin by assuming that the incoming data is a string of zeros and that a divide by two is used in the feedback loop. The output of the phase detector is simply a replica of the d_{clock} signal. Since the d_{clock} signal has a 50% duty cycle, it would appear that the DPLL is in lock. If a logic " 1 " is suddenly applied, there is no way to know if the clock signal is synchronized (the clock rising edge coincides with the center of the data bit) to the data. This leads to the first characteristic of an XOR PD;

1. The incoming data must have a minimum number of transitions over a given time interval.
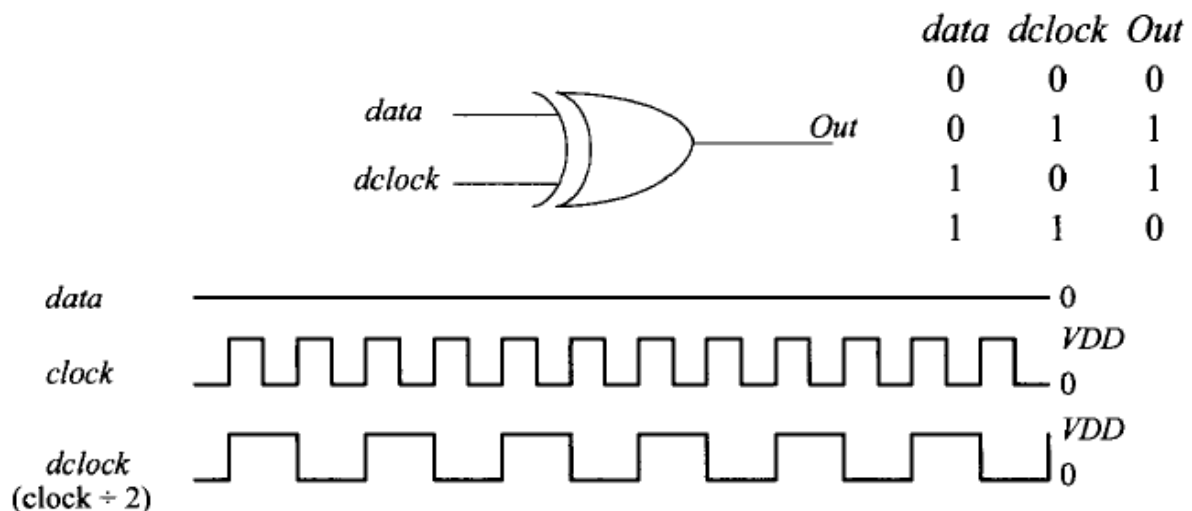

Figure 2.7: Operation of the XOR phase detector[1]

Now consider the situation when the output of the phase detector, with a string of zeros as the *data* input, is applied to a simple RC low-pass filter (Fig. 2.8). If RC »period of the clock signal, the output of the filter is simply *VDD/2*. This leads to the second characteristic of the XOR phase detector.
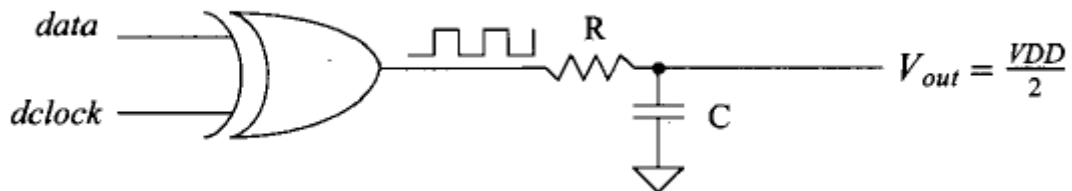
Figure 2.8: How the filtered output of the phase detector becomes VDD/2[1]

2. With no input data, the filtered output of the phase detector is *VDD/2*.

The voltage out of the loop filter is connected to the input of the VCO, as seen in Fig. 2.8. Consider the typical characteristics of a VCO shown in Fig. 2.9. The frequency of the square wave output of the VCO is $f_{center}$when $V_{jn}(=V_{center})$ is *VDD/2*(typically). The other two frequencies of interest are the minimum and maximum oscillator frequencies, f_{min} and f_{max} possible, with input voltage V_{min} and V_{max} , respectively. It is important that the VCO continues to oscillate with no input data. Normally, the VCO is designed so that the nominal data input rate and the VCO center frequency are the same. This minimizes the time it takes the DPLL to lock (and is critical for proper operation of the XOR PD).

Figure 2.9: Output frequency of VCO versus input control voltage. [1]

To characterize the phase detector , we can define the time difference between the rising edge of the d_{clock} and the beg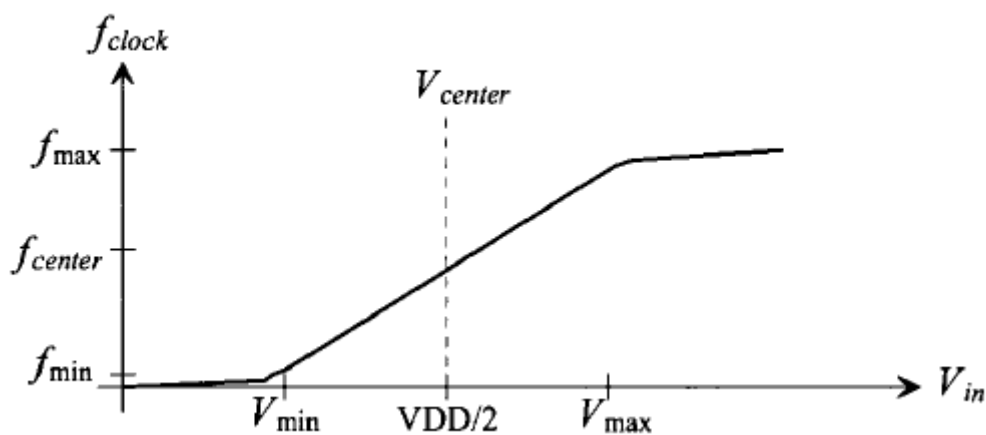inning of the *data* as *Δt*. The phase difference between the d_{clock} and *data*, $\varphi_{data} - \varphi_{dclock}$, is given by, [1]

$$\Delta\phi = \phi_{data} - \phi_{dclock} = \frac{\Delta t}{T_{dclock}} \cdot 2\pi \text{ (radians)} \qquad \text{... (2.5)}$$

or, in terms of the DPLL output clock frequency,

$$\Delta\phi = \frac{\Delta t}{2T_{clock}} \cdot 2\pi \qquad \text{... (2.6)}$$

$$f_{clock} = \frac{1}{T_{clock}} = 2f_{dclock} = \frac{2}{T_{dclock}} \qquad \text{... (2.7)}$$

When the loop is locked, the *clock* rising edge is centered on the data; the time difference, Δt, between the d_{clock} rising edge and the beginning of the data is simply $T_{clock}/2$ or $T_{dclock}/4$ (see Fig. 2.10c). Therefore, the phase difference between d_{clock} and the *data*, under-locked conditions, may be written as,

$$\Delta\phi = \frac{\pi}{2} \qquad \text{... (2.8)}$$

Note that the phase difference between clock and data when in lock is n. The average voltage out of the phase detector (Fig-2.10) may be expressed by,

$$V_{PDout} = VDD \cdot \frac{\Delta\phi}{\pi} = K_{PD} \cdot \overset{input}{\overbrace{\Delta\phi}} \qquad \text{... (2.9)}$$

where the gain of the PD may be written as,

$$K_{PD} = \frac{VDD}{\pi} \text{ (V/radians)} \qquad \text{... (2.10)}$$

As an aid in the understanding of these equations, consider the diagrams shown in Fig. 2.10. If the edges of the clock and data are coincident in time (Fig. 2.10a), the XOR output, V_{PDout},

is 0 V and the phase difference is 0. The loop filter averages the output of the PD and causes the VCO to lower its output frequency. This causes $\Delta\varphi$ to increase, thus increasing V_{PDout}. Depending on the selection of the loop filter, this increase could cause the rising edges to increase beyond, or *overshoot,* the desirable center point, as shown in Fig. 2.10b. In this case, the phase difference is $-\frac{3}{4}\pi$, and V_{PDout} is $\frac{3}{4}VDD$. Figure2.10c shows the condition when the loop is in lock and the phase difference is $\frac{\pi}{2}$.
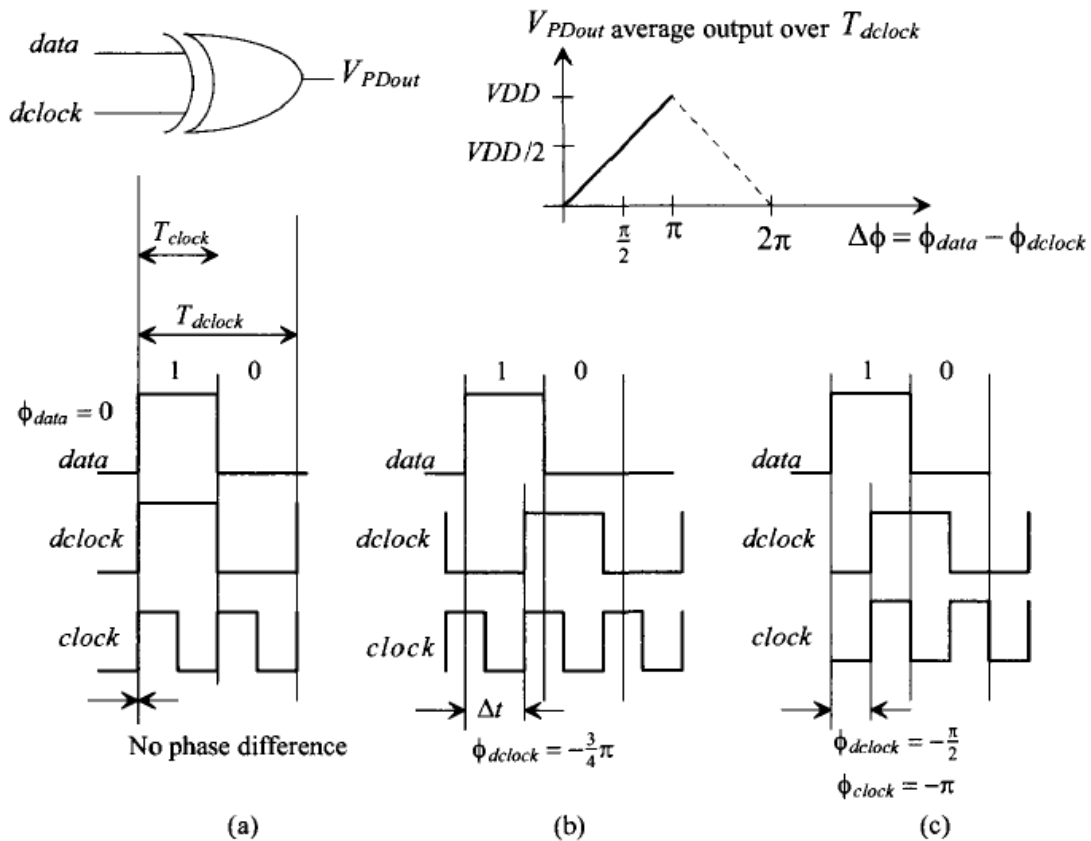
Figure 2.10: XOR PD output for various inputs (assuming input data area string of alternating ones and zeros). [1]

2.5.3 Phase-frequency detectors

Another form of detector is said to be phase-frequency sensitive. These circuits have the advantage that whilst the phase difference is between ± 180° a voltage proportional to the phase difference is given. Beyond this the circuit limits at one of the extremes. In this way no AC component is produced when the loop is out of lock and the output from the phase detector can pass through the filter to bring the phase locked loop, PLL, into lock.
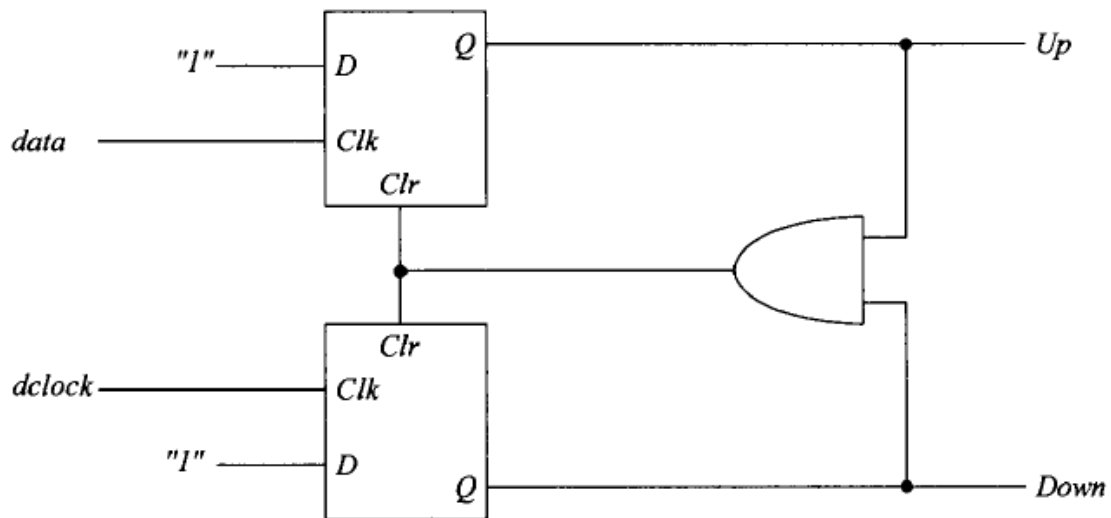
Figure 2.11: Phase frequency detector (PFD). [1]

2.5.4 Phase detector dead zone

One of the issues that faces the designers of very low phase noise synthesizers and phase locked loops, is a phenomenon referred to as the phase detector dead zone.

This occurs where digital phase detectors are used. It is found that when the loop is in lock and there is a small phase difference between the two signals, very short pulses are created by the phase detector logic gates. Being very short, these pulses may not propagate and add charge into the charge pump / loop filter. As a result the loop gain is reduced and this forces up the loop jitter / phase noise.

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Figure 2.12: Phase detector output characteristic

showing dead zone

To overcome this one solution is to add a delay in the phase detector reset path.

2.6 Voltage Controlled Oscillator Design for PLLs

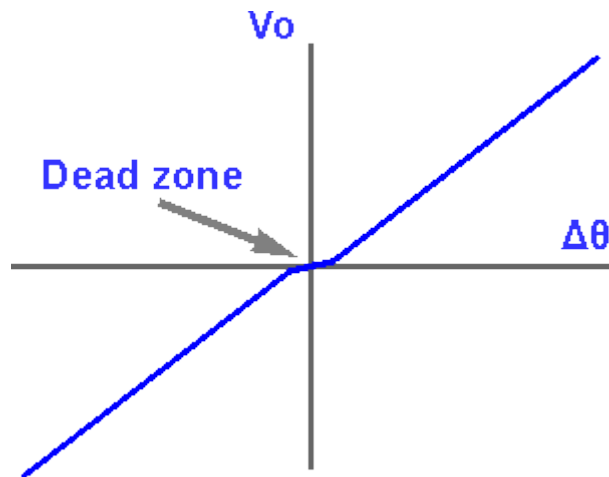Within a phase locked loop, PLL, or frequency synthesizer, the performance of the voltage controlled oscillator, VCO is of paramount importance. This is because the VCO Voltage Controlled Oscillator performance determines many of the overall performance characteristics of the overall synthesizer.

In order that the PLL or synthesizer can meet its full specification a well-designed voltage controlled oscillator is essential. Designing a really high performance voltage controlled oscillator, VCO, is not always easy as there are a number of requirements that need to be met. However by careful design, and some experimentation a good VCO design can be developed.

2.6.1 VCO performance

Just like any other circuit, with a VCO there are a number of design requirements that need to be known from the beginning of the design process. These basic requirements for the VCO will govern many of the decisions concerning the circuit topology and other fundamental aspects of the circuit. Some of the basic requirements are:

➢ **VCO tuning range:** It is obvious that the voltage controlled oscillator must be able to tune over the range that the loop is expected to operate over. This requirement is not always easy to meet and may require the VCO or resonant circuit to be switched in some extreme circumstances.

➢ **VCO tuning gain:** The gain of the voltage controlled oscillator is important. It is measured in terms of volts per Hz (or V/MHz, etc). As implied by the units it is the tuning shift for a given change in voltage. The voltage controlled oscillator gain affects some of the overall loop design considerations and calculations.
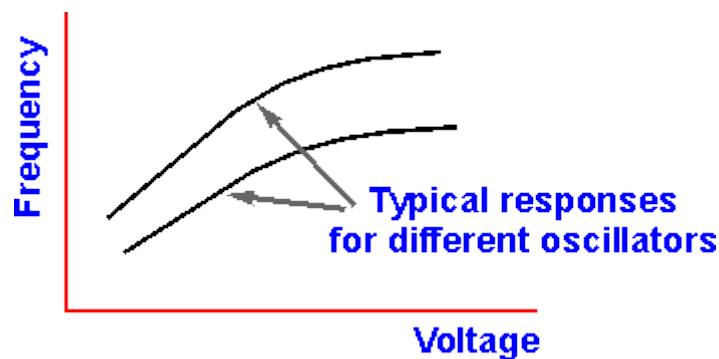
Figure 2.13: Voltage controlled oscillator V/f curves

The VCO response curves can be seen to be relatively straight at lower frequencies. However they normally flatten out at higher voltages where the changes in capacitance from the varactor diodes reduce.

➢ **VCO V/f slope:** It is a key requirement for any voltage controlled oscillator used in a phase locked loop that the voltage to frequency curve is monotonic, i.e. it always changes in the same sense, typically increasing frequency for increasing voltage. If it changes, as can happen in some instances normally as a result of spurious resonances, etc, this can cause the loop to become unstable. Accordingly, this must be prevented if the phase locked loop is to operate satisfactorily.

Figure 2.14: Voltage controlled oscillator V/f curves
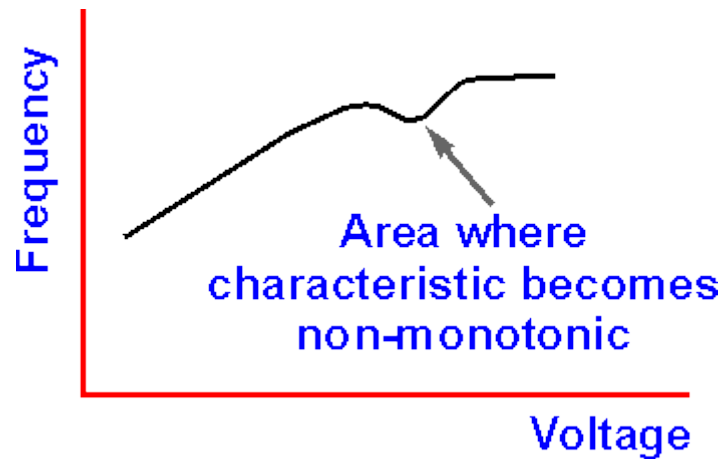
This curve shows a small dip and would result in the phase locked loop becoming unstable.

> ➤ ***Phase noise:*** The phase noise performance of the voltage controlled oscillator is of particular importance in some PLL applications - particularly where they are used in frequency synthesizers. Here the phase noise performance of the VCO determines many of the overall phase noise performance characteristics of the overall loop and the overall synthesizer if used in one.

These are some of the main requirements that need to be known from the outset of the design of the VCO. The overall tuning range and the gain are basic requirements that are part of the basic design of any PLL into which the VCO may be incorporated. So too is the phase noise characteristic. As phase noise is a basic parameter of any PLL or frequency synthesizer, so too is the characteristic of the VCO, and low phase noise VCOs are often required. For example the VCO performance may govern the overall design of the frequency synthesizer or PLL, if a given phase noise performance is to be met.

2.6.2 Choice of VCO active device

It is possible to use both bipolar devices and FETs within a VCO, using the same basic circuit topologies. The bipolar transistor has a low input impedance and is current driven, while the FET has a high input impedance and is voltage driven. The high input impedance of the FET is able to better maintain the Q of the tuned circuit and this should give a better level of

performance in terms of the phase noise performance where the maintenance of the Q of the tuned circuit is a key factor in the reduction of phase noise.

Another major factor is the flicker noise generated by the devices. Oscillators are highly non-linear circuits and as a result the flicker noise is modulated onto VCO as sidebands and this manifests itself as phase noise. In general bipolar transistors offer a lower level of flicker noise and as a result VCOs based around them offer a superior phase noise performance.

2.7 The Voltage-Controlled Oscillator

The gain of the voltage-controlled oscillator is simply the slope of the curves given in Fig.2.9. This gain can be written as, [1]

$$K_{VCO} = 2\pi \cdot \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ (radians/s} \cdot \text{V)}$$

… (2.11)

The VCO output frequency, f_{clock}, is related to the VCO input voltage by

$$\omega_{clock} = 2\pi \cdot f_{clock} = K_{VCO} \cdot V_{inVCO} + \omega_o \text{ (radians/s)}$$

… (2.12)

Where, ω_0 is a constant. However, the variable we are feeding back is not frequency but phase (hence the name of the circuit). The phase of the VCO clock output is related to f_{clock} by,

$$\phi_{clock} = \int \omega_{clock} \cdot dt = \frac{K_{VCO}}{j\omega} \cdot V_{inVCO} \text{ (radians)}$$

… (2.13)

where this signal can be related to the φ_{dclock} by,

$$\phi_{dclock} = \frac{1}{N} \cdot \phi_{clock} = \beta \cdot \phi_{clock}$$

… (2.14)

Where N is the divide by count and β is the feedback factor.

2.7.1 The Current-Starved VCO

The current-starved VCO is shown schematically in Fig. 2.15. Its operation is similar to the ring oscillator discussed earlier. MOSFETs M2 and M3 operate as an inverter, while MOSFETs Ml and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The drain currents of MOSFETs M5 and M6 are the same and are set by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. An important property of the VCO used in any of the CMOS DPLLs discussed in this chapter is the input impedance. The filter configurations we have discussed rely on the fact that the input resistance of the VCO is practically infinite and the input capacitance is small compared to the capacitances present in the loop filter.

Attaining infinite input resistance is usually an easy part of the design. For the charge-pump configuration, the input capacitance of the VCO can be added to C2.

To determine the design equations for use with the current-starved VCO, consider the simplified schematic of one stage of the VCO shown in Fig. 2.16. The total capacitance on the drains of M2 and M3 is given by, [1]

$$C_{tot} = C_{out} + C_{in} = \overbrace{C'_{ox}(W_p L_p + W_n L_n)}^{C_{out}} + \overbrace{\frac{3}{2}C'_{ox}(W_p L_p + W_n L_n)}^{C_{in}} \qquad \ldots (2.15)$$

which is simply the output and input capacitances of the inverter. This equation can be written in a more useful form as,

$$C_{tot} = \frac{5}{2}C'_{ox}(W_p L_p + W_n L_n) \qquad \ldots (2.16)$$

The time it takes to charge C_{tot} from zero to VSP with the constant-current Im is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}} \qquad \ldots (2.17)$$

while the time it takes to discharge C_{tot} from VDD to V_{sp} is given by

$$t_2 = C_{tot} \cdot \frac{VDD - V_{SP}}{I_{D1}} \qquad \ldots (2.18)$$

If we set $I_{D4} = I_{D1} = I_D$ (which we will label $I_{Dcenter}$ when $V_{inVCO} = VDD/2$), then the sum of t_1 and t_2 is simply,

$$t_1 + t_2 = \frac{C_{tot} \cdot VDD}{I_D} \qquad \ldots (2.19)$$

The oscillation frequency of the current-starved VCO for N (an odd number ≥ 5) of stagesis

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N \cdot C_{tot} \cdot VDD} \qquad \ldots (2.20)$$

Which is $= f_{center}$ (@ $V_{inVCO} = VDD/2$ and $I_D = I_{Dcenter}$)
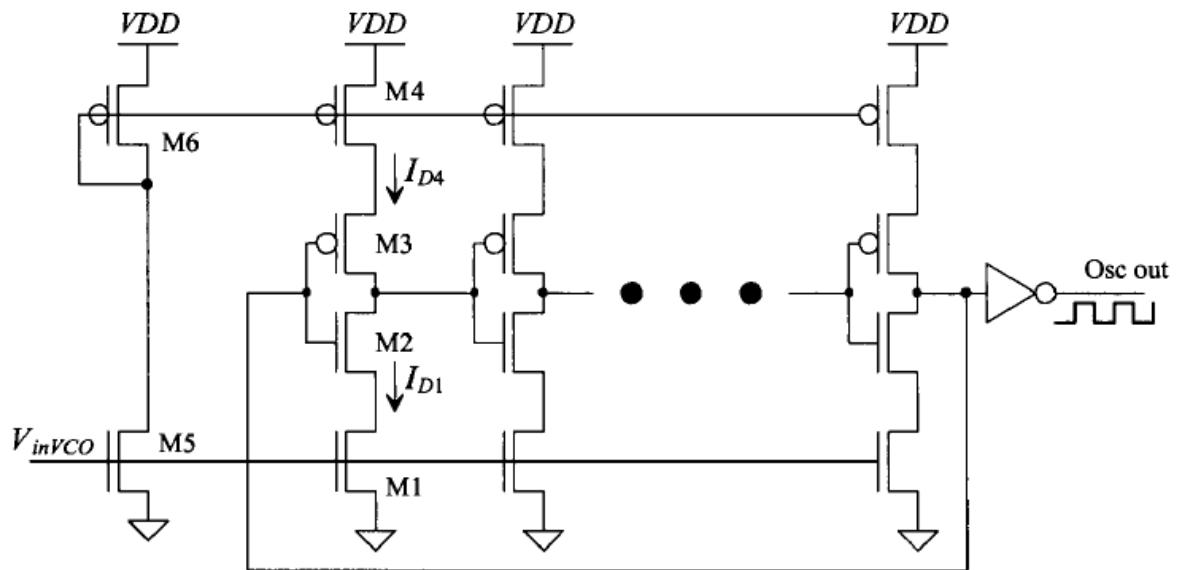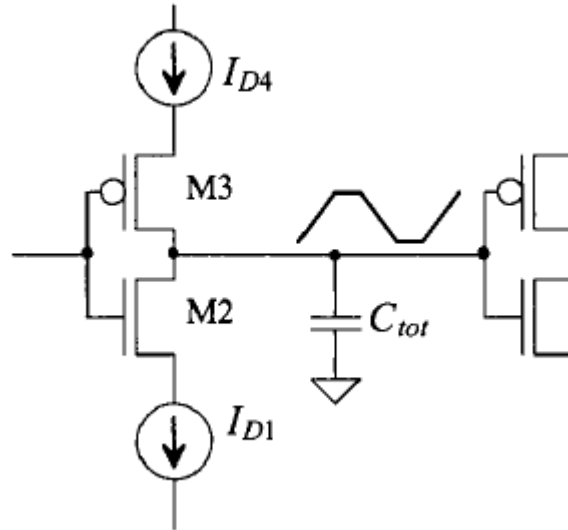

Figure 2.15: Current-starved VCO. [1]

Figure 2.16: Simplified view of a single stage of the current-starved VCO. [1]

The above equation gives the center frequency of the VCO when $I_D=I_{Dcenter}$. The VCO stops oscillating, neglecting sub threshold currents, when $V_{inVCO}< V_{THN}$. Therefore, we can define

$$V_{min} = V_{THN} \text{ and } f_{min} = 0 \qquad \qquad \text{... (2.21)}$$

The maximum VCO oscillation frequency, f_{max} is determined by finding I_D when $V_{inVCO}=VDD$. At the maximum frequency then, $V_{max} = VDD$

The output of the current-starved VCO shown in Fig. 2.15 is normally buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency or lower the gain of the oscillator enough to kill oscillations altogether.

The average current drawn by the VCO is,

$$I_{avg} = N \cdot \frac{VDD \cdot C_{tot}}{T} = N \cdot VDD \cdot C_{tot} \cdot f_{osc} \qquad \qquad \text{... (2.22)}$$

Or,

$$I_{avg} = I_D \qquad \qquad \text{... (2.23)}$$

The average power dissipated by the VCO is

$$P_{avg} = VDD \cdot I_{avg} = VDD \cdot I_D$$

<div align="right">… (2.24)</div>

If we include the power dissipated by the mirror MOSFETs, M5 and M6, the power is doubled from that given by above equation, assuming that $I_D = l_{D5} = I_{D6}$. For low-power dissipation we must keep I_D low, which is equivalent to stating that for low-power dissipation we must use a low-oscillation frequency.

2.7.2 Source-Coupled VCO

Another variety of VCO, source-coupled VCOs, is shown in Fig. 2.17. These VCOs can be designed to dissipate less power than the current-starved VCO of the last section for a given frequency. The major disadvantage of these configurations is the need for a capacitor, something that may not be available in a single-poly pure digital process without using parasitics for example, a metal 1 to metal2 capacitor, and a reduced output voltage swing. However, this configuration is useful when the VCO center frequency is set by an external capacitor; that is, the capacitor shown in the figure is bonded out.

To understand the operation, let's consider the NMOS source-coupled VCO of Fig. 2.17a. The operation of the CMOS source-coupled VCO of Fig. 2.17b is identical to (a) except for the fact that the load MOSFETs M3 and M4 pull the outputs to $VDD - V_{THN}$ (for the NMOS-load VCO) and VDD (for the PMOS-load VCO).
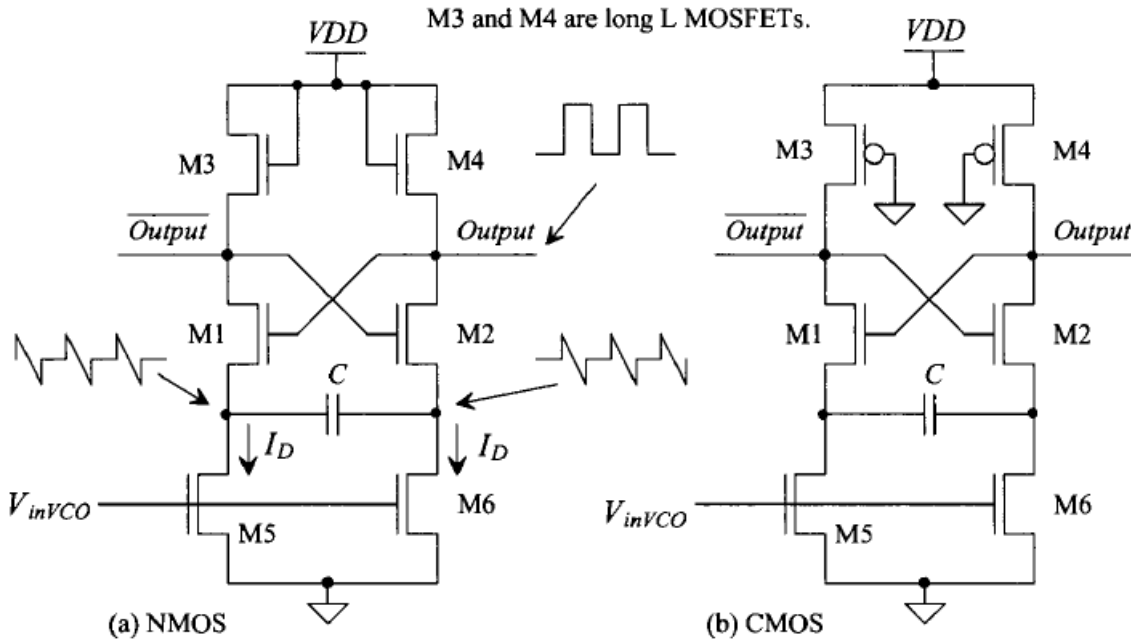
Figure 2.17: Source coupled voltage-controlled oscillators (also known as source coupled multi vibrators). [1]

For the circuit in Fig. 2.17a, MOSFETs M5 and M6 behave as constant-current sources sinking a current I_D. MOSFETs M1 and M2 operate as switches. If M1 is off and M2 is on, the drain of M1 is pulled to *VDD - V_{THN}* by M3. Since the gate of M2 is at *VDD— V_{THN}*, the source and drain (the *Output)* of M2 are approximately *VDD – 2.V_{THN}*. This is the minimum output voltage. The output voltage swing is limited to *V_{THN}*. A simplified schematic shown in Fig. 2.18 with M1 off and M2 on is helpful in determining the oscillator frequency. The *Output* gate of M1 is approximately *VDD – 2.V_{THN}* and is held at this voltage through M2 until M1 turns on and M2 turns off. Initially, at the moment when M1 turns off and M2 turns on, point X is *VDD - V_{THN}*. The current through C, *I_D,* causes point X to discharge down toward ground. When point X gets down to *VDD –3.V_{THN},* M1 turns on and M2 turns off. In other words, the voltage at point X changed a total of *2.V_{THN}* before switching took place.
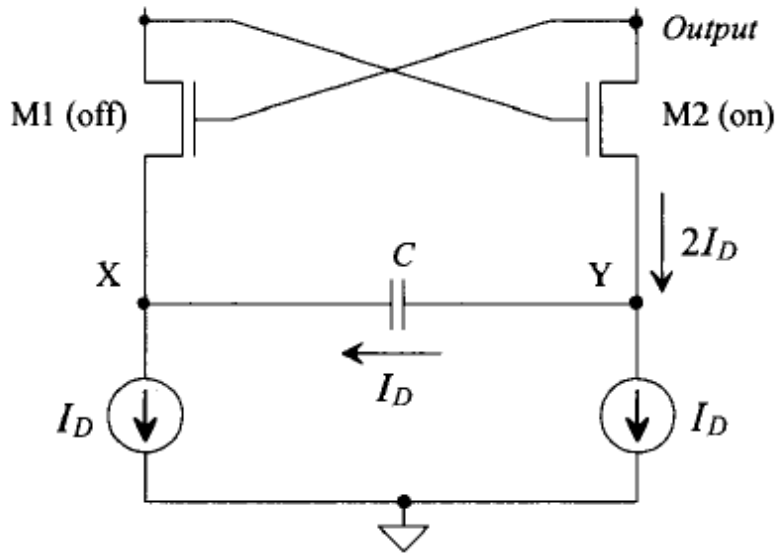
Note: C should be laid out with the same parasitic capacitance at X and Y.

Figure 2.18: Simplified schematic of source coupled oscillator, Ml is on and M2 is off. [1]

The time it takes point X to change *2-VTHN* is given by,

$$\Delta t = C \cdot \frac{2 \cdot V_{THN}}{I_D} \qquad \text{... (2.25)}$$

Since the circuit is symmetrical, two of these discharge times are needed for each cycle of the oscillation. The frequency of oscillation is given by,

$$f_{osc} = \frac{1}{2\Delta t} = \frac{I_D}{4 \cdot C \cdot V_{THN}} \qquad \text{... (2.26)}$$

The waveforms at the points X, Y, and *Output* are shown in Fig. 2.19 for continuous time operation.
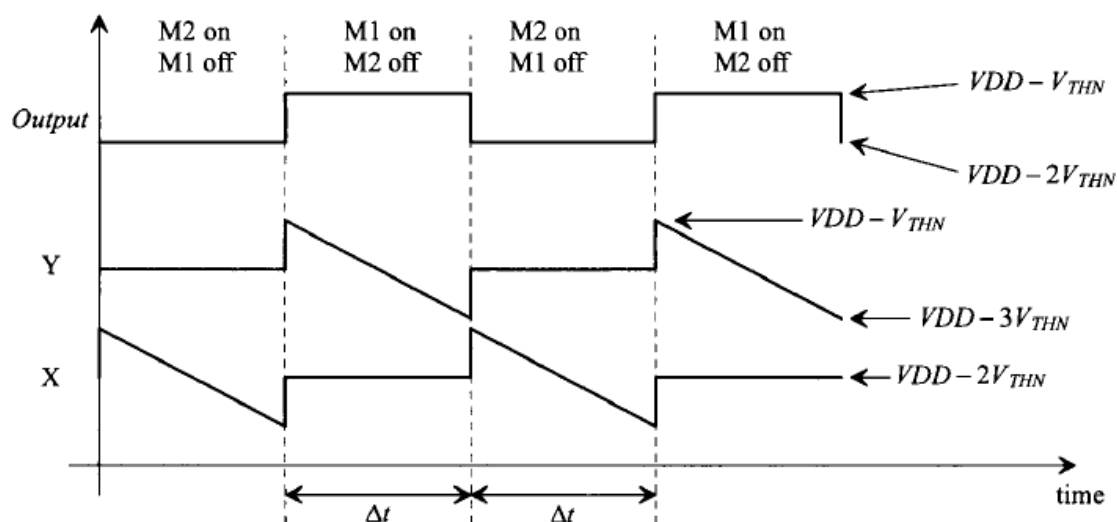

Figure 2.19: Voltage waveforms for the NMOS source-coupled VCO. [1]

2.8 PLL Loop Filter

Filters are an essential part of telecommunications and radar systems. The microwave filter is a two port network which used to control the frequency response by providing transmission at frequencies within the pass-band and attenuation in the stop-band of a filter.

2.8.1 Filter Types

➢ **Monolithic Crystal Filters**

2 Quartz resonator internally coupled utilizing piezoelectric effect.

➢ **Discrete Crystal Filter**

Single quartz resonator with external components utilizing the piezoelectric effect.

> **Notch filters**

Crystal or Discrete component filter that passes all frequencies except those in a stop band centered on a center frequency.

> **High Pass Filters**

Discrete component filter that passes high frequency but alternates frequencies lower than the cut of frequency.

> **Low Pass Filters**

Discrete component filter that passes low frequency signals but alternates signals with frequencies higher than the cut off frequency.

> **Band Pass Filter**

A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range.

> **Band Stop Filter**

In signal processing, a band-stop filter or band-rejection filter is a filter that passes most frequencies unaltered, but attenuates those in a specific range to very low levels. It is the opposite of a band-pass filter.

2.8.2 Design of Band Pass Filter

A general layout of a parallel coupled microstrip band-pass is shown in figure 3.1. The filter structure consists of open circuited coupled microstrip-lines. The characteristics of these coupled lines are

> Quarter wavelength
> (λ/4) long
> Equivalent to shunt resonant circuits

The coupling gaps correspond to the admittance inverters which are used to compute Even- and odd- mode characteristic impedances of parallel-coupled half-wave resonators. These even- and odd- mode impedances are then used to compute physical dimensions of the filter.

Now consider a band-pass filter composed of a cascade of $N + 1$ coupled line sections numbered from left to right, with the load on the right, but the filter can be reversed without affecting the response.
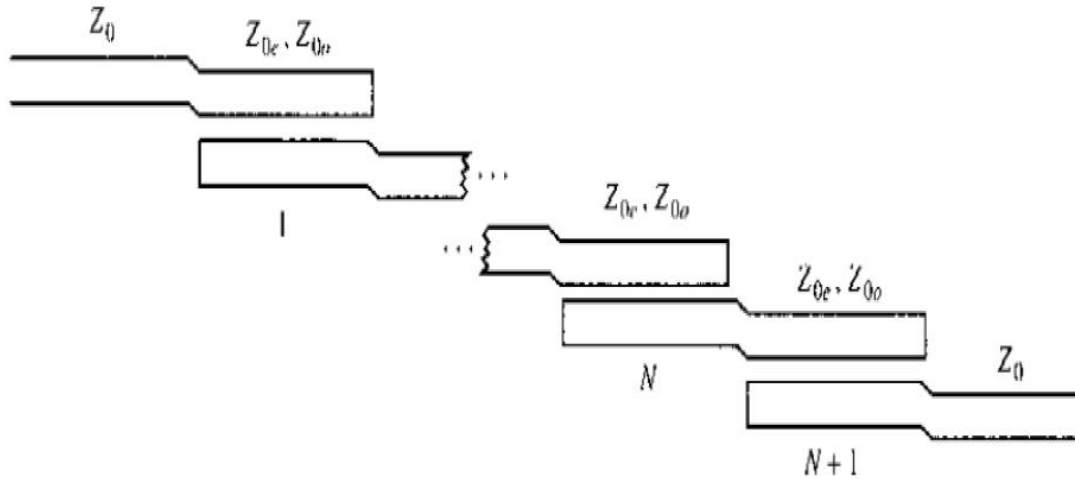

Figure 2.20 (a): Layout of an (N + 1)-section coupled line bandpass filter[2]
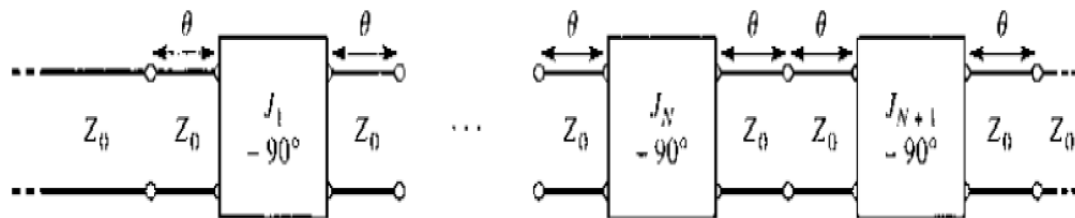

Figure 2.20 (b): Using an equivalent circuit each coupled line section[2]

Immittance inverters are used to transform a filter circuit into an equivalent form that can be easily implemented using various microwave structures. Making use of the properties of immittance inverters, bandpass filters may be realized by series (L-C) resonant circuits separated by impedance inverters (K) or shunt (L-C) parallel resonant circuits separated by admittance inverters (J). A low-pass prototype circuit is modified to include immittance inverters, then these low pass structures are converted to bandpass circuits by applying conventional low-pass to bandpass transformation.
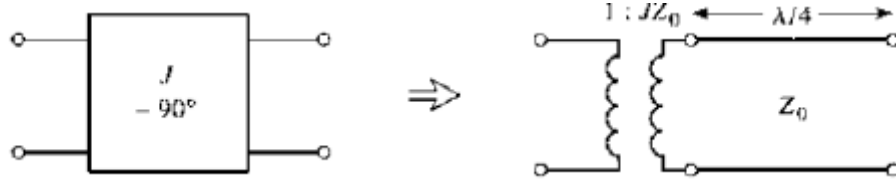
Figure 2.20 (c): Using an equivalent circuit each coupled line section[2]

The design equations for this type of filter are given by Equivalent circuit of the admittance inverters, [2]

$$\frac{J_{01}}{Y_0} = \sqrt{\frac{\pi}{2} \frac{FBW}{g_0 g_1}} \qquad \text{... (2.27)}$$

$$\frac{J_{j,j+1}}{Y_0} = \frac{\pi FBW}{2} \frac{1}{\sqrt{g_j g_{j+1}}} \quad ; \ j = 1 \text{ to } n\text{-}1 \qquad \text{... (2.28)}$$

$$\frac{J_{n,n+1}}{Y_0} = \sqrt{\frac{\pi FBW}{2 g_n g_{n+1}}} \qquad \text{... (2.29)}$$

Where n is a number of filter order, and are the element of a ladder-type low pass prototype with a normalized cut off $\Omega c = 1$, and FBW is the fractional bandwidth of band pass filter. are the characteristic admittances of J-inverters and is the characteristic admittance of the terminating lines. The reason for this is because the both types of filter can have the same low pass network representation. However, the implementation will be different. To realize the J-inverters obtained above, the even- and odd-mode characteristic impedances of the coupled strip line resonators are determined by

$$(Z_{Oe})_{j,j+1} = \frac{1}{Y_0}\left[1 + \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \qquad \text{... (2.30)}$$

$$(Z_{Oo})_{j,j+1} = \frac{1}{Y_0}\left[1 - \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \qquad \text{... (2.31)}$$

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The next step of the filter design is to find the dimensions of coupled microstrip lines that exhibit the desired even- and odd-mode impedances. Firstly, determine equivalent single microstrip shape ratios (w/h)s. Then it can relate coupled line ratios to single line ratios.

For a single microstrip line,

$$Z_{ose} = \frac{(Zoe)j,j+1}{2}$$ ... (2.32)

$$Z_{oso} = \frac{(ZOo)j,j+1}{2}$$ ... (2.33)

Now using single line equations to find (w/h)se and (w/h)so from Z_{ose} and Z_{oso}

For (w/h) <2 ,

$$\frac{W}{h} = \frac{8\exp(A)}{(\exp(2A)-2)}$$ ... (2.34)

Where,

$$A = \frac{Z_c}{60}\sqrt{\frac{\varepsilon_r+1}{2}} + \frac{\varepsilon_r-1}{\varepsilon_r+1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right)$$ ... (2.35)

For (w/h) > 2,

$$\frac{W}{h} = \frac{2}{\pi}\left[B - 1 - \ln(2B - 1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left\{\ln(B - 1) + 0.39 - \frac{0.61}{\varepsilon_r}\right\}\right]$$ ... (2.36)

Where,

$$B = \frac{377\pi}{2Z_c\sqrt{\varepsilon_r}}$$ ... (2.37)

(w/h)se and (w/h)so by applying Z_{ose} and Z_{oso} (as Z_c) to the single line microstrip equations.

Now it comes to a point where it reach the w/h and s/h for the desired coupled microstrip line using a family of approximate equations as following, [4][2]

$$\frac{w}{h} = \frac{1}{\pi}\left[\cosh^{-1}\frac{1}{2}\left(\left(\cosh\left(\frac{\pi s}{2h}\right)-1\right)+\left(\cosh\left(\frac{\pi s}{2h}\right)+1\right)\cosh\left(\left(\frac{\pi}{2}\right)\left(\frac{w}{h}\right)_{se}\right)\right)-\left(\frac{\pi s}{2h}\right)\right] \quad \ldots (2.38)$$

$$\frac{S}{h}=\frac{2}{\pi}\cosh^{-1}\left[\frac{\cosh\left(\left(\frac{\pi}{2}\right)\left(\frac{w}{h}\right)se\right)+\cosh\left(\left(\frac{\pi}{2}\right)\left(\frac{w}{h}\right)so\right)-2}{\cosh\left(\left(\frac{\pi}{2}\right)\left(\frac{w}{h}\right)so\right)-\cosh\left(\left(\frac{\pi}{2}\right)\left(\frac{w}{h}\right)se\right)}\right] \quad \ldots (2.39)$$

The effective dielectric constant is given by

$$\varepsilon_{reff}=\frac{\varepsilon r+1}{2}+\frac{\varepsilon r-1}{2}\frac{1}{\sqrt{1+12\frac{h}{w}}} \quad \ldots (2.40)$$

Once the effective dielectric constant of a microstrip is determined, the guided wavelength of the quasi-TEM mode of micro strip is given by

$$\lambda_g=\frac{\lambda}{\sqrt{\varepsilon_{reff}}}=\frac{c}{f\sqrt{\varepsilon_{reff}}} \quad \ldots (2.41)$$

Thus the length of the required resonator is

$$l = \frac{\lambda_g}{4} \quad \ldots (2.42)$$

The design of the PLL, loop filter is crucial to the operation of the whole phase locked loop. The choice of the circuit values here is usually a very carefully balanced compromise between a number of conflicting requirements.

The PLL filter is needed to remove any unwanted high frequency components which might pass out of the phase detector and appear in the VCO tune line. They would then appear on the output of the Voltage Controlled Oscillator, VCO, as spurious signals. To show how this

happens take the case when a mixer is used as a phase detector. When the loop is in lock the mixer will produce two signals: the sum and difference frequencies. As the two signals entering the phase detector have the same frequency the difference frequency is zero and a DC voltage is produced proportional to the phase difference as expected. The sum frequency is also produced and this will fall at a point equal to twice the frequency of the reference. If this signal is not attenuated it will reach the control voltage input to the VCO and give rise to spurious signals.

When other types of phase detector are used similar spurious signals can be produced and the filter is needed to remove them.

The filter also affects the ability of the loop to change frequencies quickly. If the filter has a very low cut-off frequency then the changes in tune voltage will only take place slowly, and the VCO will not be able to change its frequency as fast. This is because a filter with a low cut-off frequency will only let low frequencies through and these correspond to slow changes in voltage level.

Conversely a filter with a higher cut-off frequency will enable the changes to happen faster. However when using filters with high cut-off frequencies, care must be taken to ensure that unwanted frequencies are not passed along the tune line with the result that spurious signals are generated.

The loop filter also governs the stability of the loop. If the filter is not designed correctly then oscillations can build up around the loop, and large signals will appear on the tune line. This will result in the VCO being forced to sweep over wide bands of frequencies. The proper design of the filter will ensure that this cannot happen under any circumstances.

2.9 PLL Phase Locked Loop Gain

One of the key aspects of a phase locked loop is its stability. This is controlled by the loop response and the loop gain.

These two factors are linked, and one of the main configurables that enables the loop stability to be controlled is the loop filter performance..

While elements such as the gain of the various elements- VCO, phase detector, etc. are important, it may not be easy to change their performance.

Chapter 3

Design and Simulation

Following table shows the technology we have used for design purpose-

Table 3.1: Parameters Used in Simulation

Technology	Drawn	Scale factor	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS(short-channel)	10/1	50 nm	0.5 µm by 50 nm	3.4 k	625 aF
PMOS(short-channel)	20/1	50 nm	1 µm by 50 nm	3.4 k	1.25 fF

3.1   Phase detector

A schematic diagram of the phase detector is shown below-
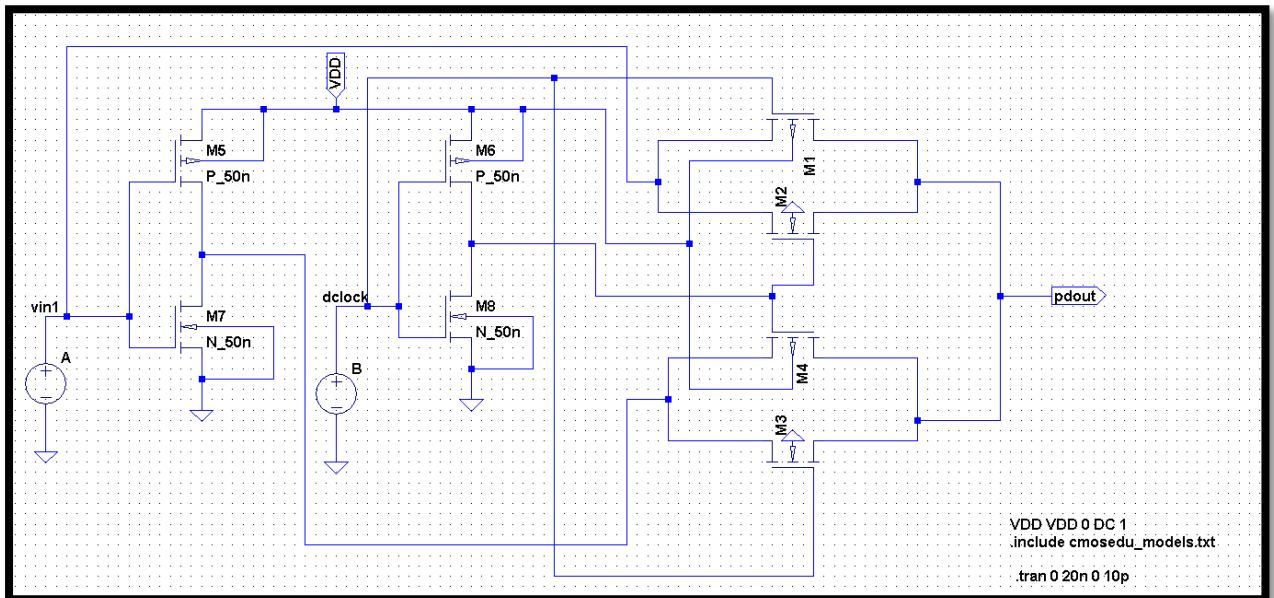
Figure 3.1: Phase Detector Schematic

The simulation result for the XOR phase detector when d_clock leads data by π-
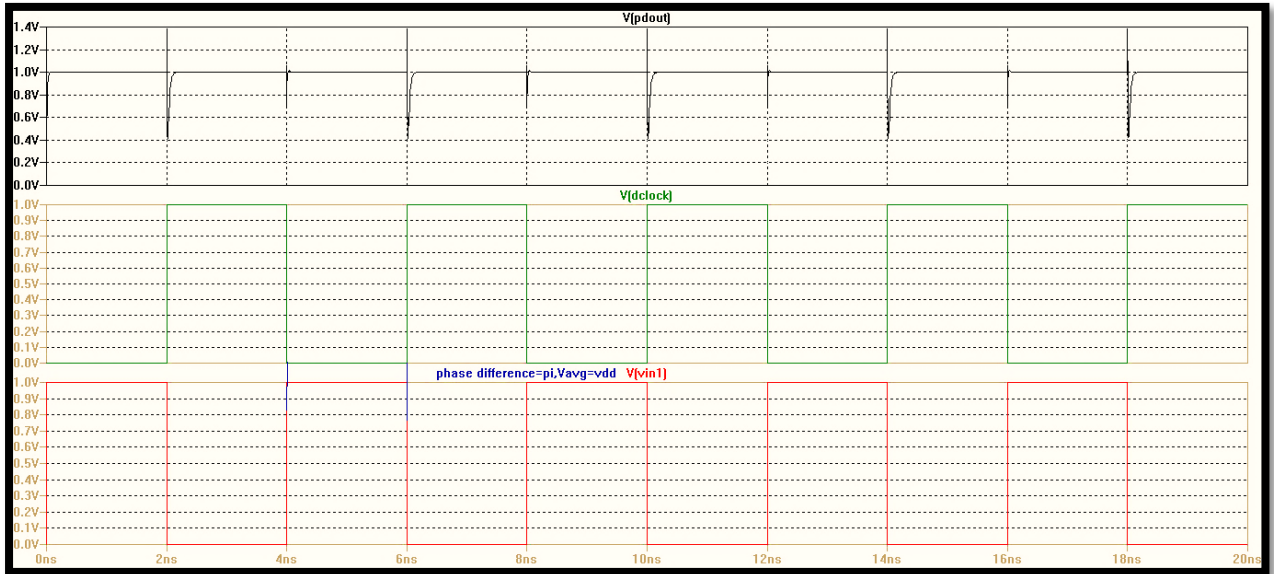
Figure 3.2: XOR Phase Detector with Phase Difference (π)

The simulation result for the XOR phase detector when d_clock leads data by $\frac{\pi}{2}$ −
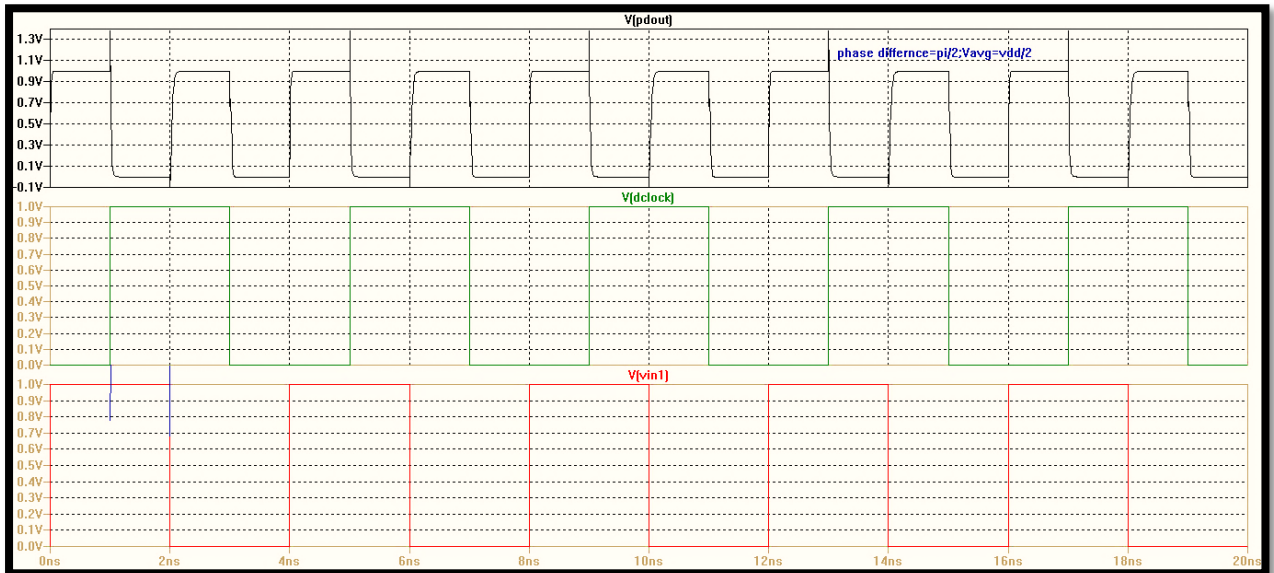
Figure 3.3: XOR Phase Detector with Phase Difference ($\frac{\pi}{2}$)

The simulation result for the XOR phase detector when there is no phase difference-
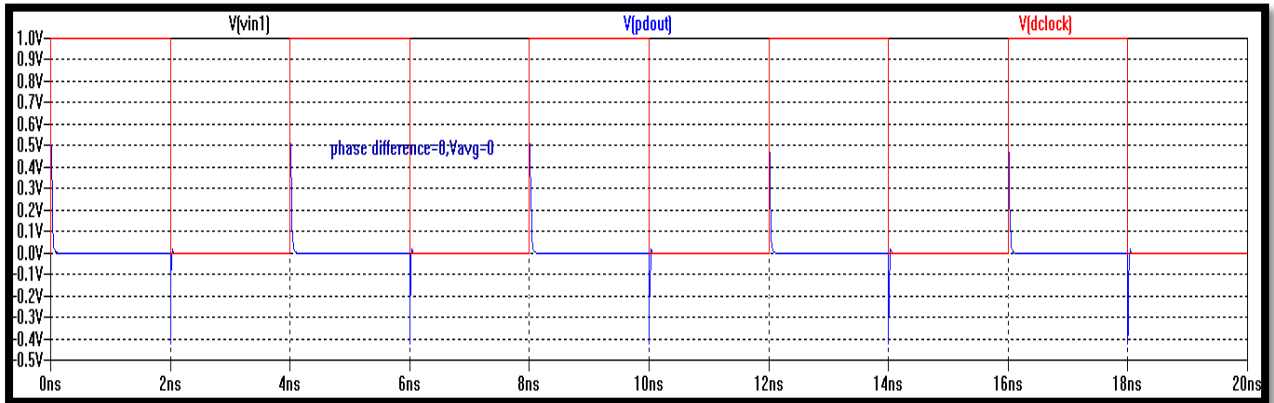

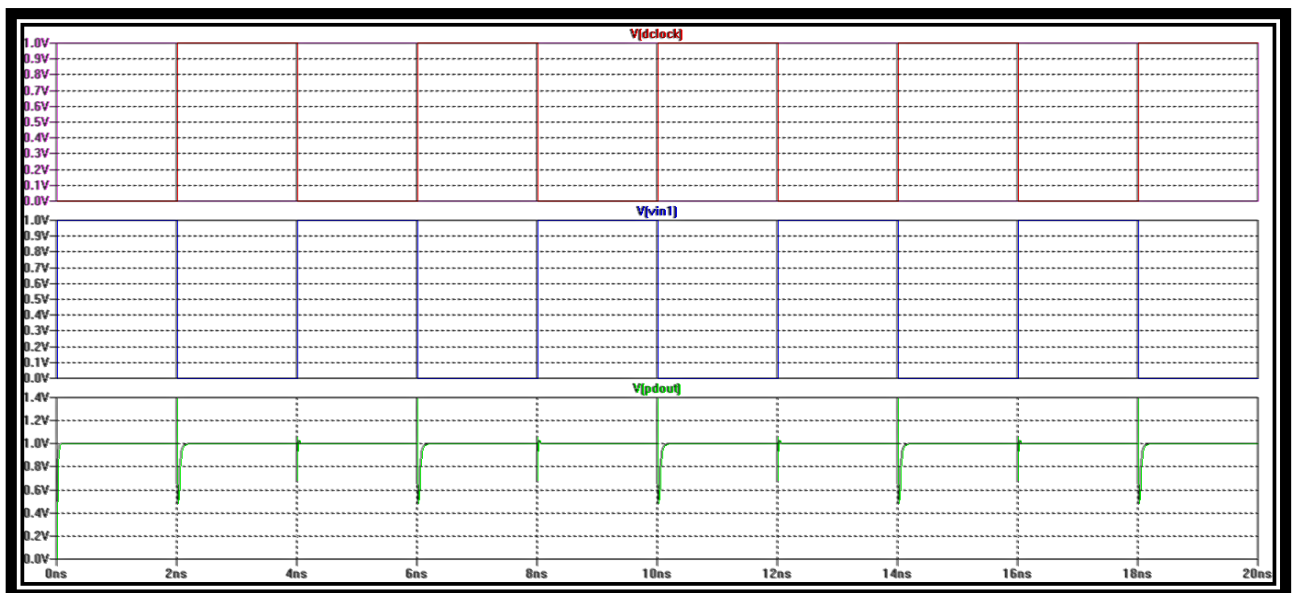Figure 3.4: XOR Phase Detector with Phase Difference (0)

Process Variation

Figure 3.5: Effect of Process Variation

There is no process scattering effect on the output voltage of PD as is depicted on the above figure.
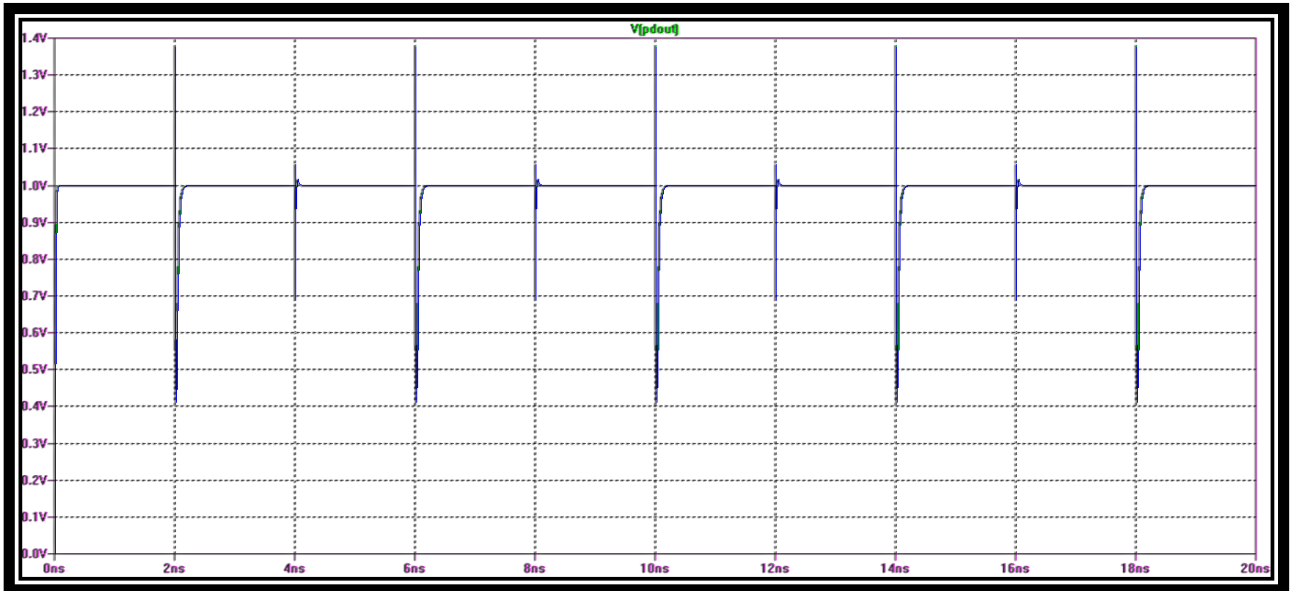
Temperature effect

Figure 3.6: Effect of Temperature Variation

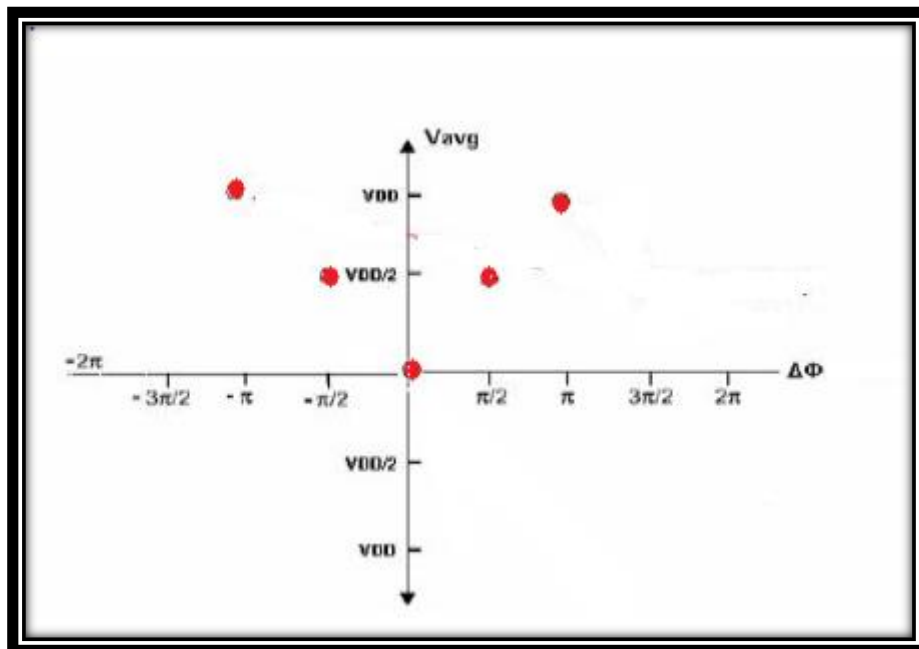We have found no impact on output voltage of PD due to temperature change.

Figure 3.7: XOR PD Characteristics

3.1.1 Power Dissipation

Total Power Dissipation = 54.5924 nW

3.2 Voltage controlled oscillator (VCO)

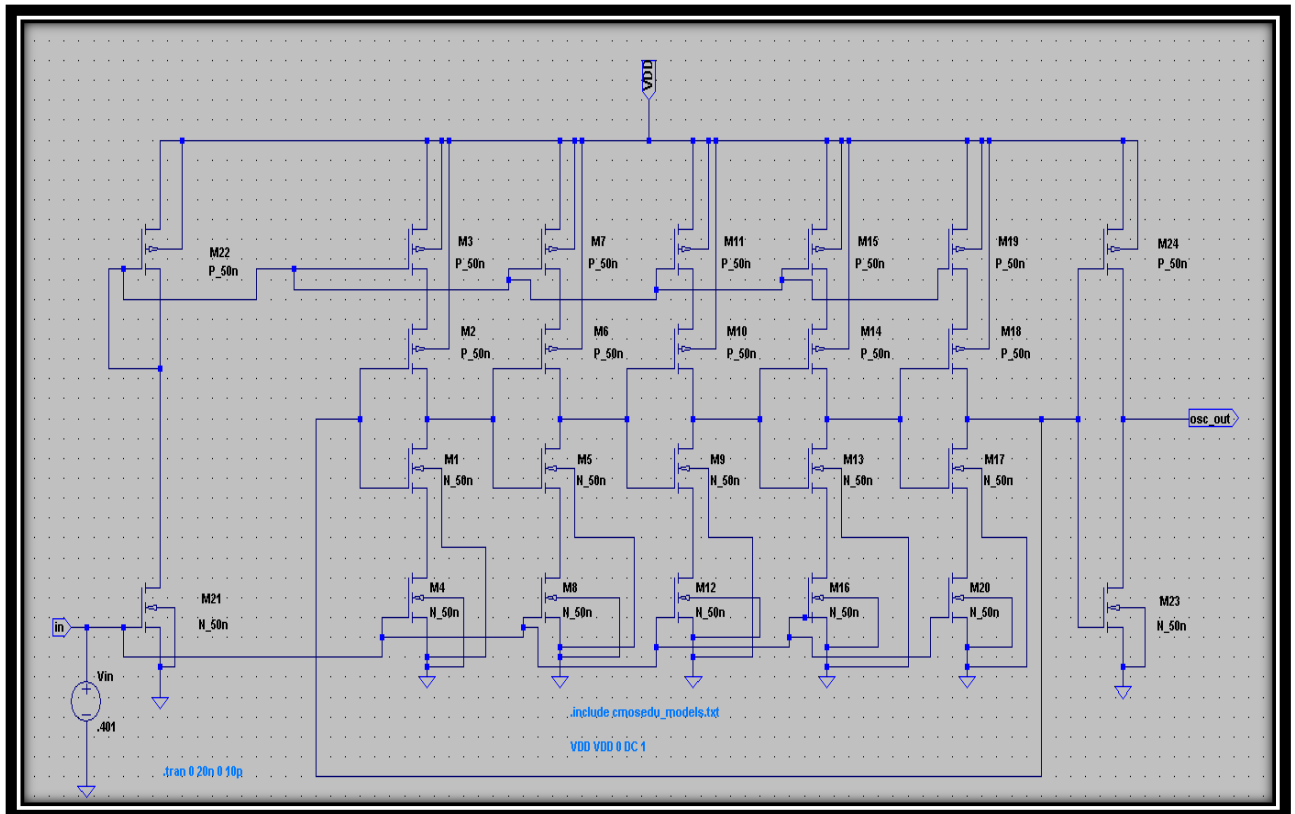A schematic diagram of the designed VCO is given below-

Figure 3.8: Schematic Diagram of VCO in LTSPICE

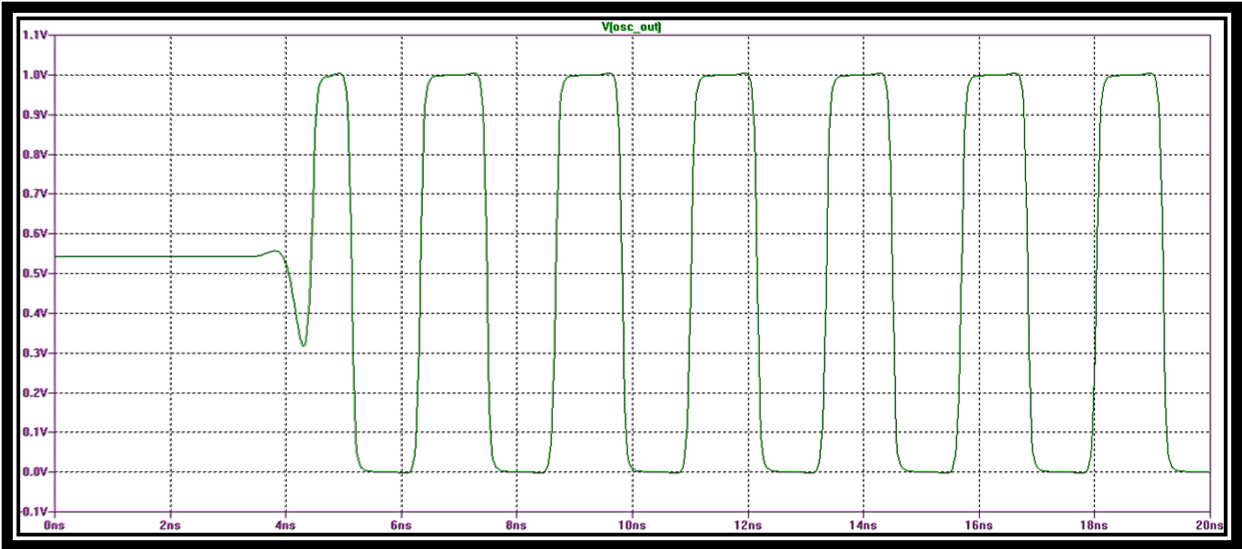Simulated output waveform using LTSpice-

Figure 3.9: VCO output waveform in LTSPICE

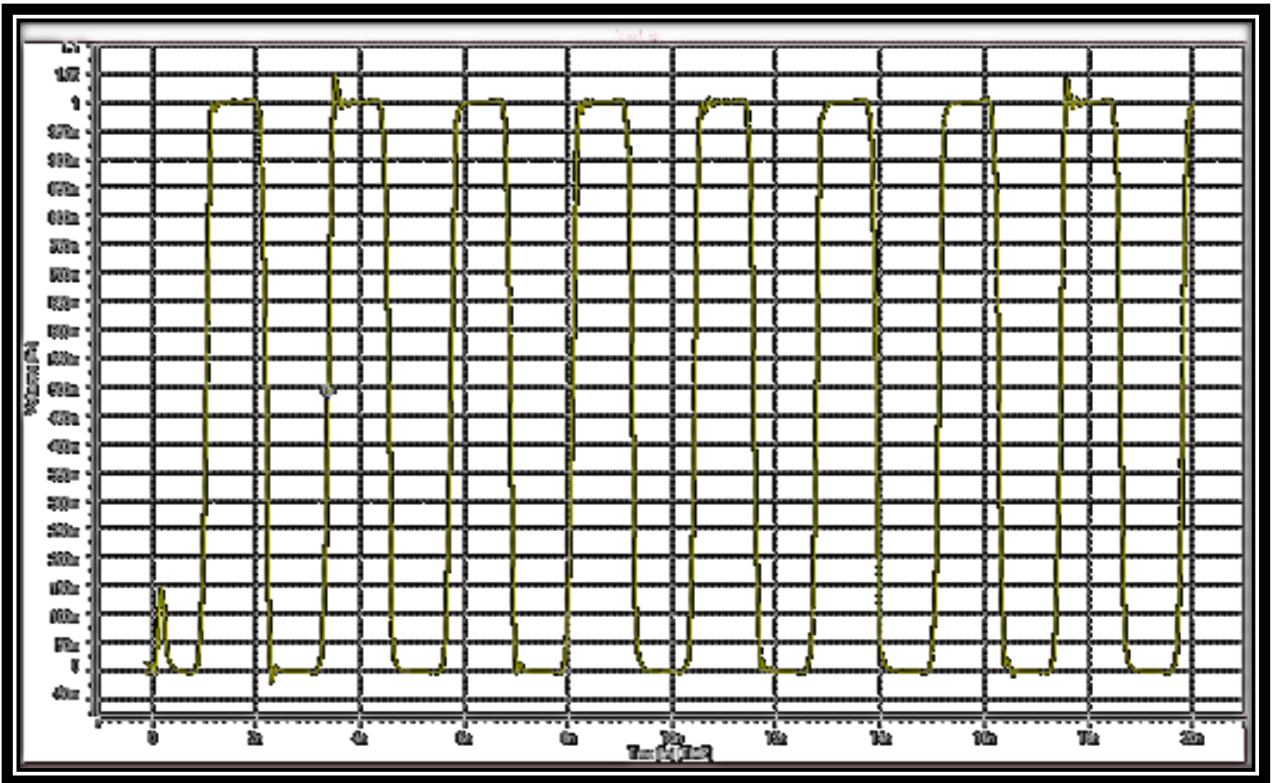Simulated output waveform using HSpice-

Figure 3.10: VCO output waveform in HSPICE

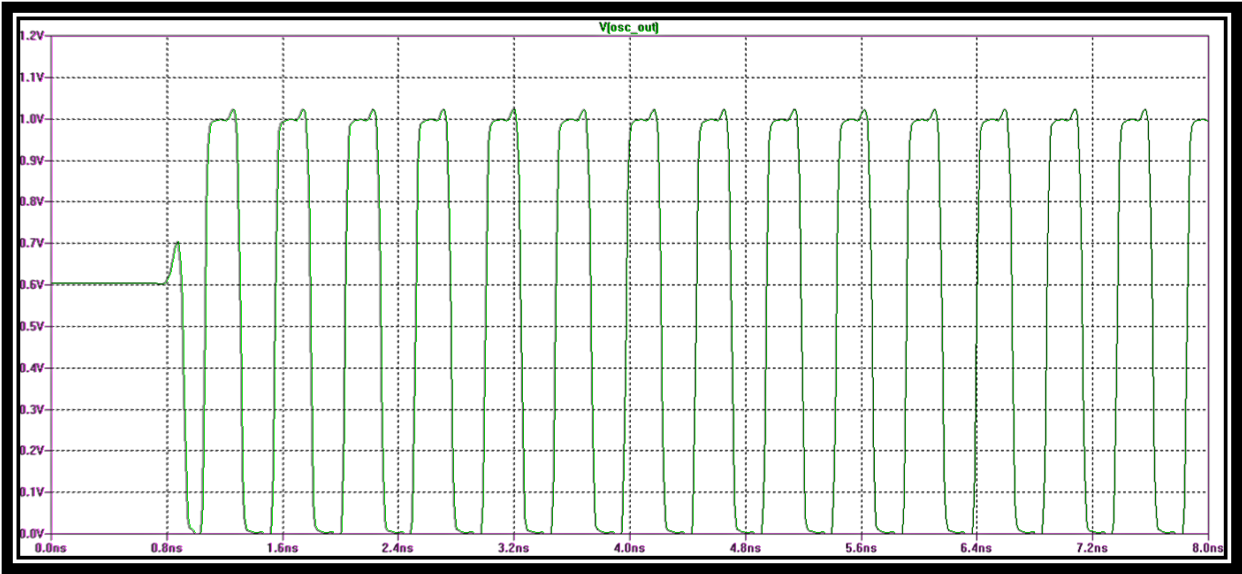Setting VDD at 0.9 V we get the following results-

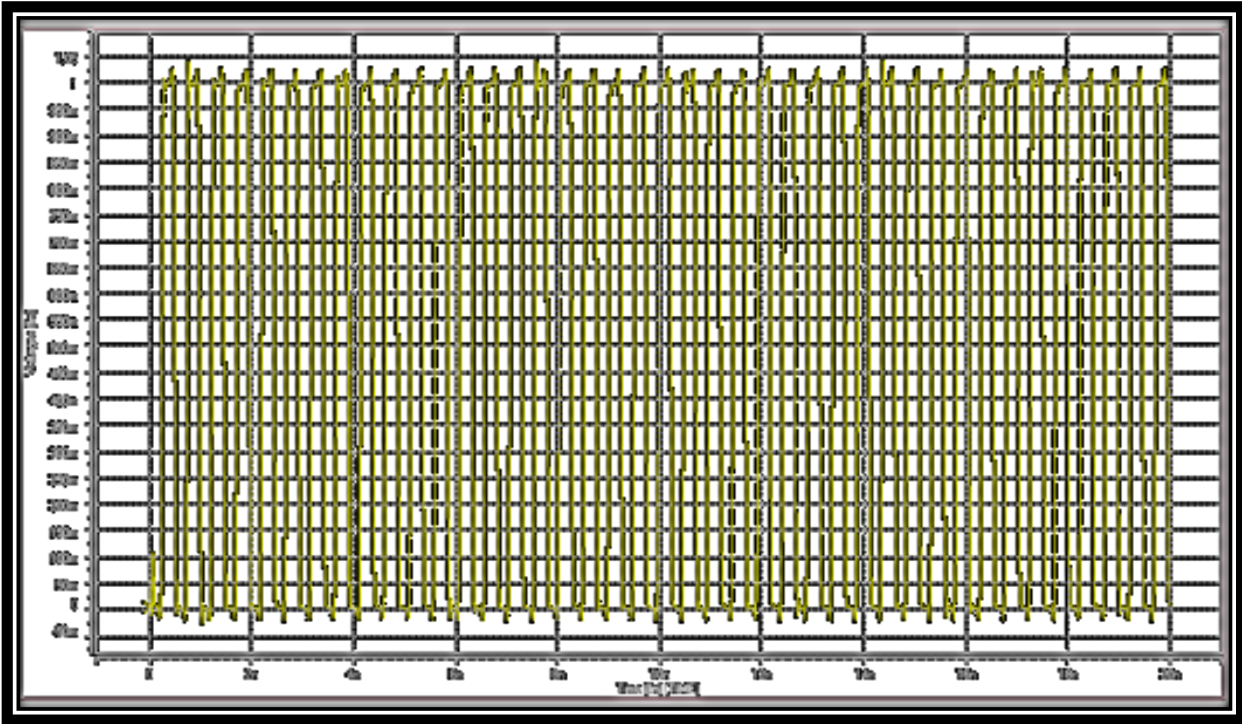Figure 3.11: VCO output waveform in LTSPICE (0.9V)

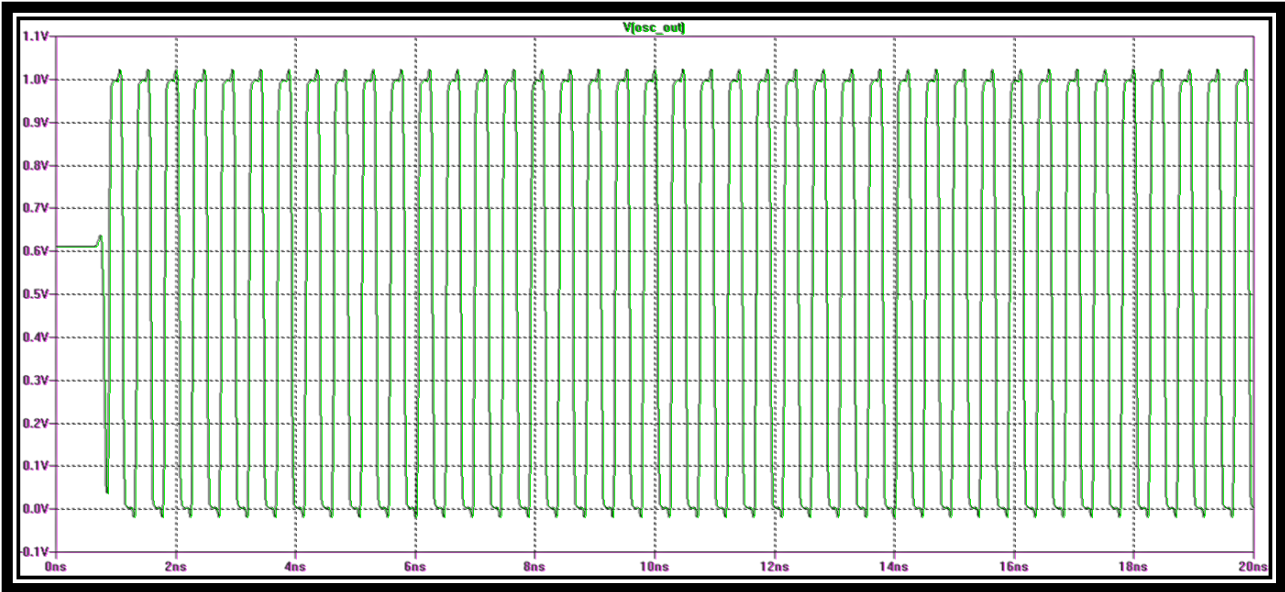Figure 3.12: VCO output waveform in HSPICE (0.9V)

As for VDD = 1.1 V -

Figure 3.13: VCO output waveform in LTSpice (1.1V)
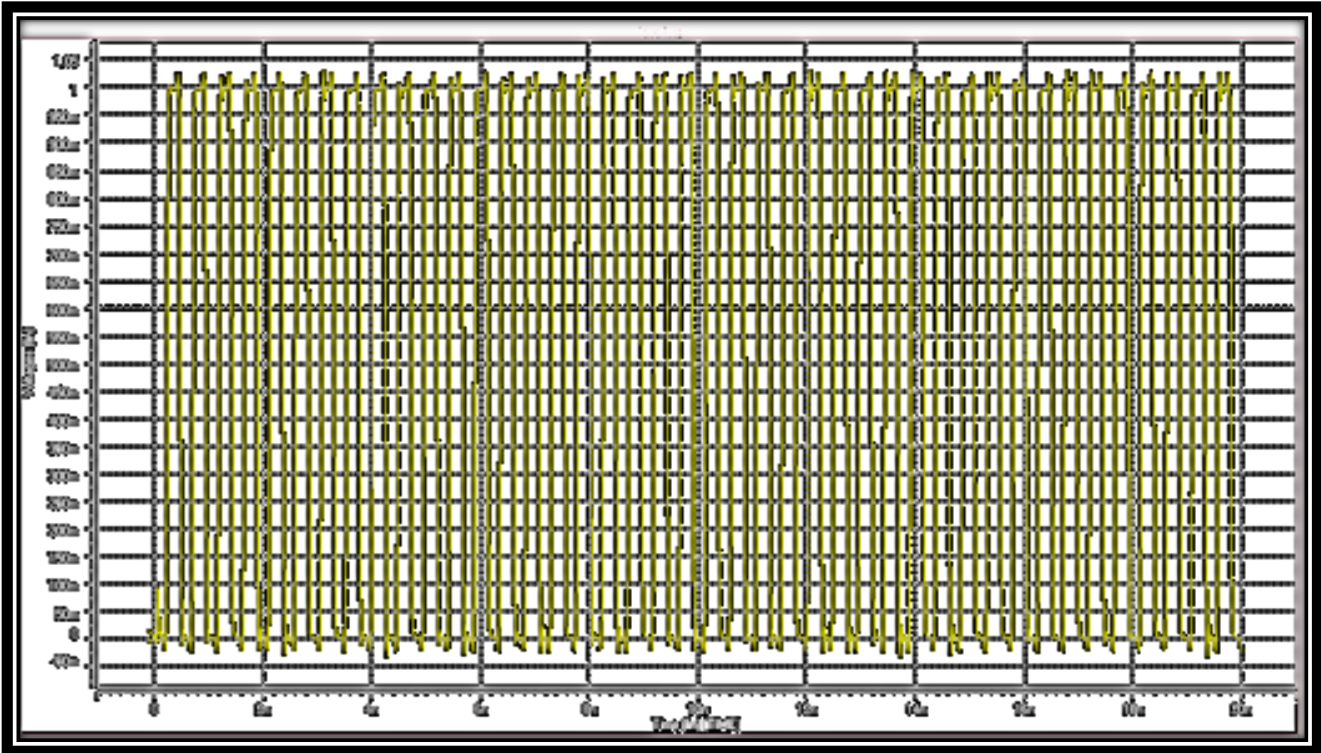
Figure 3.14: VCO output waveform in HSpice (1.1V)

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Plotting Voltage against Frequency we get the following result-

Figure 3.15: Frequency vs. Voltage graphical representation

Table 3.2: Data for Control voltage and frequency

Control Voltage	Frequency (LTSpice)	Frequency (HSpice)
(*V*)	(*GHz*)	(*GHz*)
0.573	1.42	1.40
0.6	1.54	1.54
0.7	1.8	1.81
0.8	1.92	1.96
0.9	2.07	2.04
1.00	2.08	2.08

Temperature Effect

We simulate the results of temperature effect on the VCO component by changing it from 50°C to 75°C-

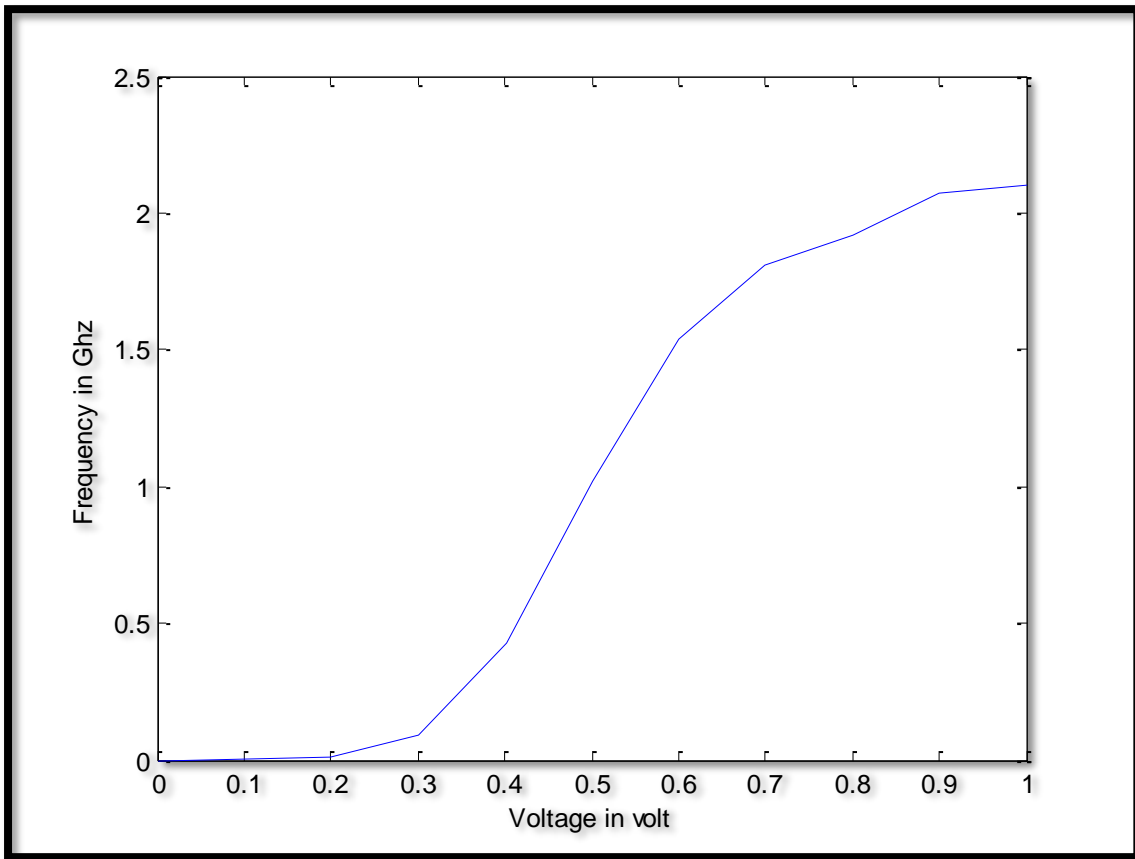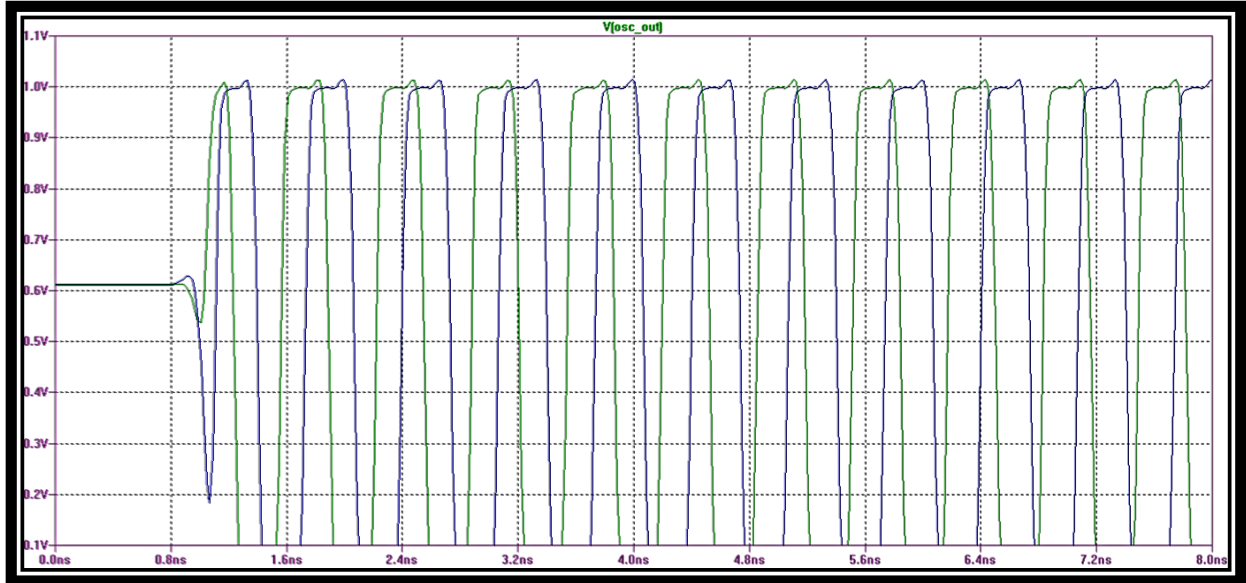Figure 3.16: Temperature variation for 50°C and 75°C (in LTSPICE)

Table 3.3: Effect of Temperature Variation on Frequency

Control Voltage (*V*)	Frequency at 50°C (*GHz*)	Frequency at 75°C (*GHz*)
0.573	1.41	1.40
0.6	1.49	1.51
0.7	1.75	1.72
0.8	1.89	1.86
0.9	1.95	1.92
1.0	2.0	1.94

VDD (±10% Variation)

To understand the effect of VDD variation we first increase it by 10%-

Figure 3.17: Observing the frequency at VDD (+10%) while Vin=1

Reducing the value of VDD by 10% we get-

Figure 3.18: Observation of the frequency at VDD (-10%) while Vin=1

Let us observe the results by the same variation with Vin set to 0.6 V starting with a 10% increase-
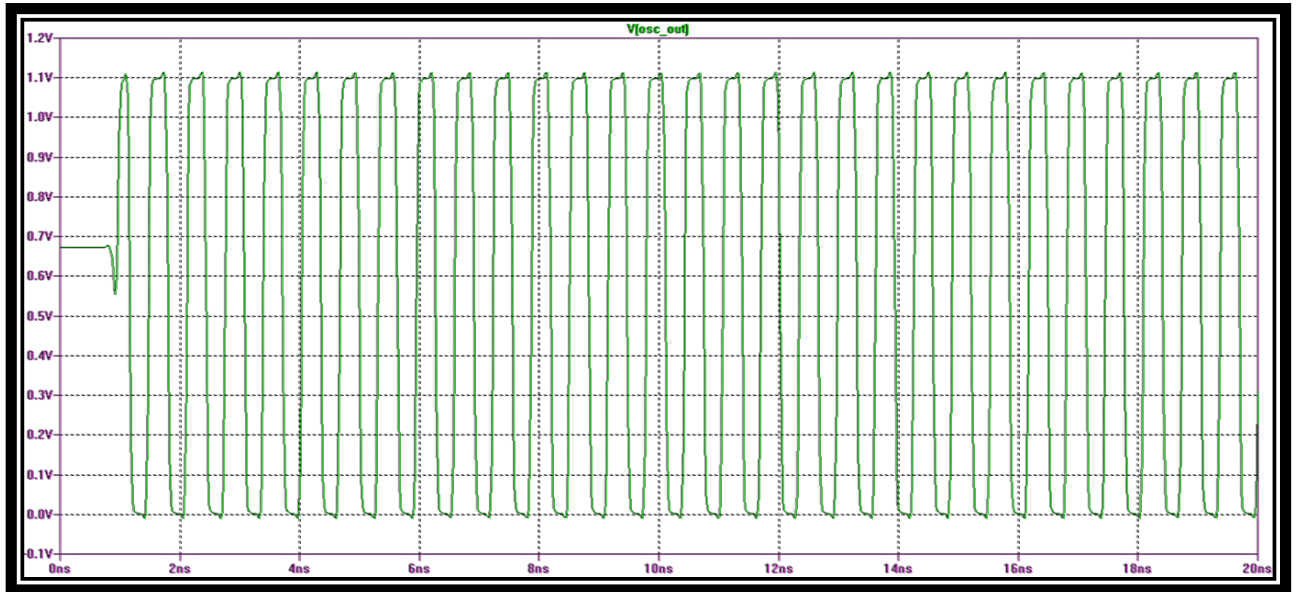
Figure 3.19: Observation of frequency at VDD (+10%)

As for 10% decrease we get-
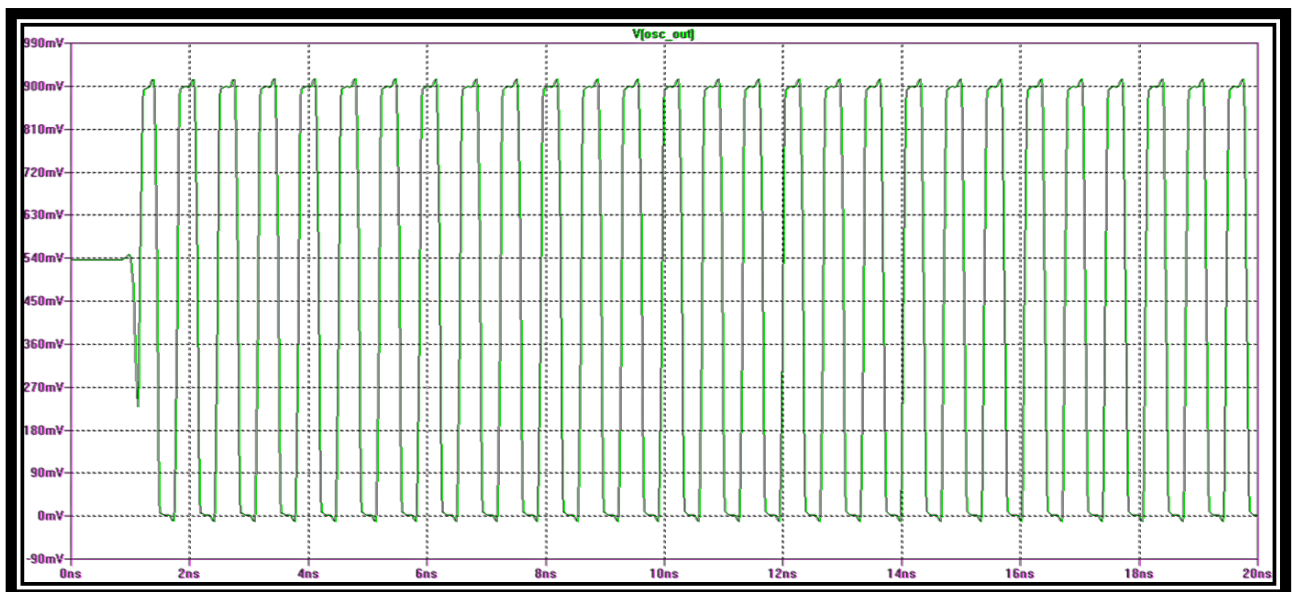
Figure 3.20: Observation of frequency at VDD (-10%)

Table 3.4: Data for VDD Variation (±10%)

Vin or Control Voltage (V)	Frequency at VDD=0.9V (GHz)	Frequency at VDD=1.1V (GHz)
0.573	1.37	1.43
0.6	1.48	1.59
0.7	1.69	1.92
0.8	1.80	2.08
1.0	1.86	2.25

Process Variation

Checking whether a change of process have any effect on the VCO component we get the following results-

Figure 3.21: Output waveform of CSVCO due to process scattering.

3.2.1 Power dissipation

Table 3.5: Total Power Dissipation

Voc (V)	Total Power Dissipation (μW)
0.401	136.0637
1.0	379.4973

3.3 Band Pass Filter Design

For design purpose we use,

FR4 substrate

Dielectric constant= 4.4

Thickness, h =1.6mm

Loss tangent, tanδ=0.002

Source Impedance = 50 Ohms

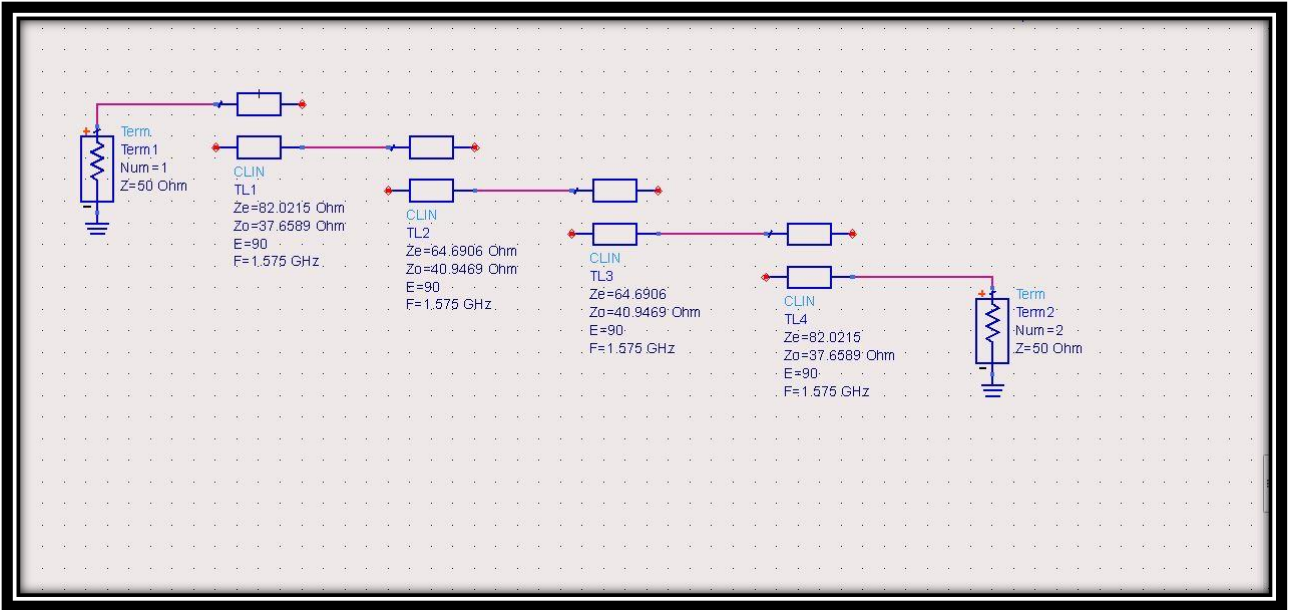A schematic diagram of band-pass filter is given below-

Figure 3.22: Schematic of microstrip coupled line bandpass filter

We simulate the performance of the designed filter-
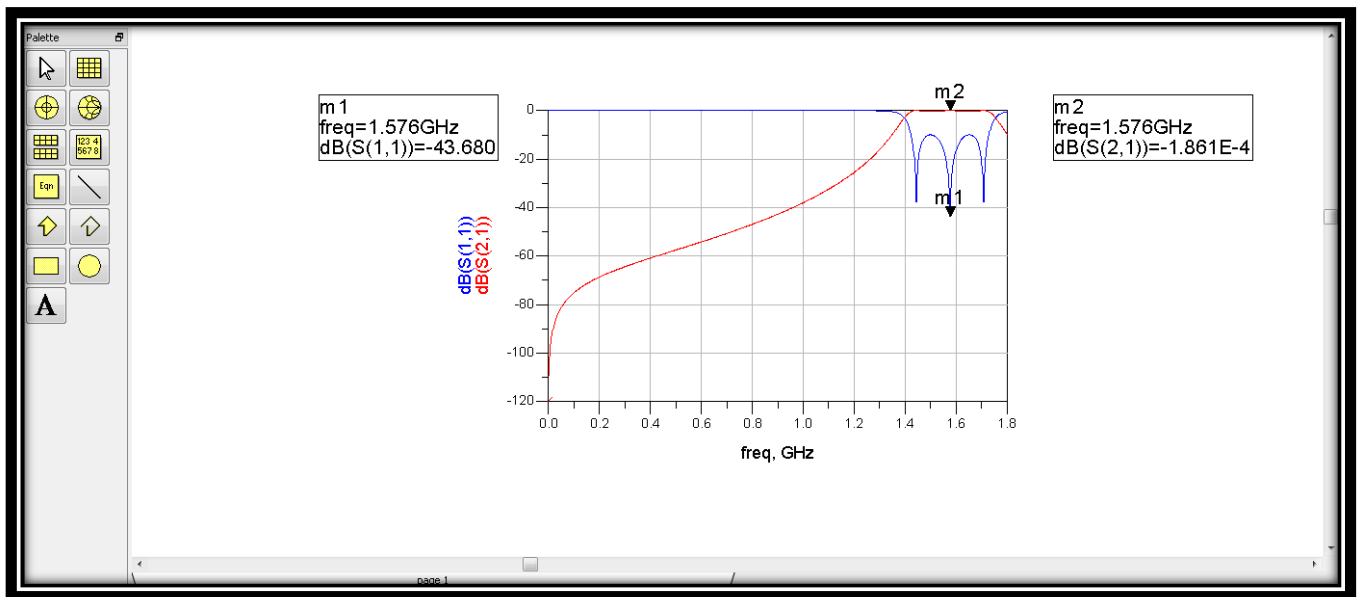
Figure 3.23: Simulated performance of microstrip parallel coupled bandpass filter

A 3D view representation of the filter-
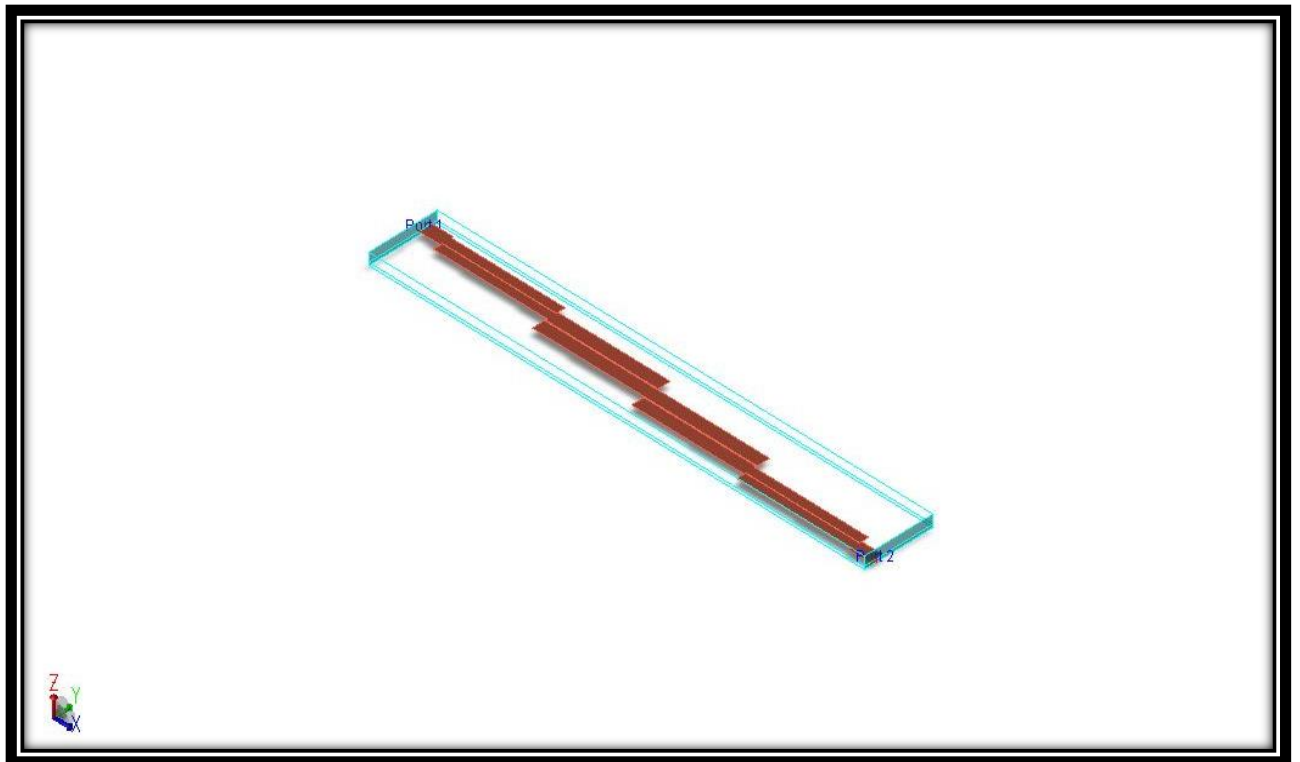
Figure 3.24: 3D structure design of microstrip parallel coupled bandpass filter in EDS

The 3D structure of band-pass filter is depicted in figure (3.24) and geometry show in table(3.5). A MATLAB code (Given in Appendix) is used to evaluate the Table (3.4) & Table (3.5).

Table 3.6: Calculated results of Even and Odd Impedance

J	$J_{J,J+1} / Y_0$	$(Z_{0e})_{J,J+1}$ (Ω)	$(Z_{0o})_{J,J+1}$ (Ω)
0	0.443626	82.0215	37.6589
1	0.237437	64.6906	40.9469
2	0.237437	64.6906	40.9469
3	0.443626	82.0215	37.6589

Table 3.7: Width and the Quarter Wavelength

J	W_J / h	S_J / h	ϵ_{re}	l (mm)
0	1.29731	0.0276846	3.23099	26.4917
1	1.7955	0.1169364	3.313299	26.1607
2	1.7955	0.1169364	3.313299	26.1607
3	1.29731	0.0276846	3.23099	26.4917

Chapter 4

Conclusion

4.1 Result and Discussion

From simulation, varying phase difference, and Fig. (3.7) we can conclude that phase difference generates average voltage at the output of PD which is linear in relation.

Design and simulation is done in LTSpice and HSpice. Fig. (3.8) depicts the schematic diagram of CSVCO and following fig.(3.9) and fig.(3.10) shows the output waveform at 0.401 V.. Both software shows approximately the same frequency at the same corresponding voltage. Table(3.2) shows the results.

Temperature variation is simulated at 0.6 V depicted in Fig(3.16). The green curve is for 50°C with frequency 1.51 GHz and the blue line stands for 75°C, corresponding frequency is 1.49 GHz.

For $V_{DD} \pm 10\%$ variation, we observe the frequency change which is given in the table.

When changing 50 nm to 55 nm, frequency drops. We also observe that for 0.6 V, the corresponding frequency is 1 GHz.

The simulated filter structure and response is shown in fig. (3.22) and fig. (3.23). In the response graph gain (dB) is plotted on the y axis and frequency (GHz) on the X axis. It is clear that the simulated mid-band (center) frequency is found to be 1.576 GHz. The values of insertion loss (S_{21}) and return loss (S_{11}) are (- 0.00018) dB and (- 43.680) dB at the center frequency. The Fabricated filter was measured using ADS and the simulated result shows that the band edges frequencies are 1.42 GHz and 1.72 GHz. From the simulation, we get approximately 19% bandwidth. Designed filter achieved a 3dB bandwidth of 23%.

4.2 Recommendation for Future Work

The following works can be carried out in future:

1. As the components are designed only, these discrete components will be integrated and simulated.

2. CSVCO performance parameters other than power and frequency, such as phase noise and linearity technique will be considered.

3. Self-correcting PD will be designed for increasing the performance, furthermore PFD (Phase frequency detector) will be designed and implemented for expanding the use of DPLL.

4. Layout design of CSVCO and PD will be performed.

5. We will make step for changing the bandwidth of Microstrip coupled line band-pass filter according to our future design.

6. For designing we have dealt with a pitfall and it is about lack of having professional licensed software.

7. We can come up with a conclusion that this individual components design will aid us to achieve a better scheme on DPLL in near future.

Appendix

Codes

Bandpass Code

clc, clear

%Microstrip coupled line bandpass filter calculation

er=4.4;

B=.2; %bandwidth

% A1=(Jo1/Yo);

% F=(J12/Yo);

% D=(J23/Yo);

% E=(j34/Yo);

T=sqrt(1.0967*1.5963)*2;

A1=sqrt(pi*B/(2*1.5963));

F=(pi*B)/T;

D=(pi*B)/T;

G=sqrt(pi*B/(2*1.5963));

%for the 1st line pair

Zoe01=50*(1+A1+A1*A1);

Zoo01=50*(1-A1+A1*A1);

%for the 2nd line pair

Zoe02=50*(1+F+F*F);

Zoo02=50*(1-F+F*F);

%for single edge microstrip line

%for 1st and 4th line pairs

Zose14=Zoe01/2

Zoso14=Zoo01/2

%for 2nd and 3rd line pairs

```matlab
Zose23=Zoe02/2

Zoso23=Zoo02/2



%for 1st and 4th line pairs


 B14 = 377*pi/(2*Zose14*sqrt(er));


Mse=2/pi*(B14-1-log(2*B14-1)+(er-1)/(2*er).*(log(B14-1)+0.39-0.61/er))   %Mse=(w/h)se



B14o = 377*pi/(2*Zoso14*sqrt(er));
Mso=2/pi*(B14o-1-log(2*B14o-1)+(er-1)/(2*er).*(log(B14o-1)+0.39-0.61/er))   %Mso=(w/h)so


%for 2nd & 3rd line pairs


 B23 = 377*pi/(2*Zose23*sqrt(er));


Nse=2/pi*(B23-1-log(2*B23-1)+(er-1)/(2*er).*(log(B23-1)+0.39-0.61/er))   %Nse=(w/h)se



B23o = 377*pi/(2*Zoso23*sqrt(er));
Nso=2/pi*(B23o-1-log(2*B23o-1)+(er-1)/(2*er).*(log(B23o-1)+0.39-0.61/er))   %Nso=(w/h)so


%it comes to a point where it reach the w/h and s/h for the desired coupled edge-strip line
%for 1st & 4th line pairs
y=cosh((pi/2)*2.62240);
p=cosh((pi/2)*7.4758);
sratioh14=acosh(62960.88708/62901.35723)*(2/pi)


%for 2nd& 3rd line pairs
```

```matlab
y1=cosh((pi/2)*3.7017);


p=cosh((pi/2)*6.7425);

s=y1+p-2;

d=p-y1;

sratioh23=acosh(s/d)*(2/pi)


%For find out value w/h
%for 1st and 4th line pair
a=(cosh((pi/2)*sratioh14)+1)*cosh((pi/2)*Mse);

b=(cosh((pi/2)*sratioh14)-1);

wratioh12=(acosh(.5*(a+b))-((pi/2)*sratioh14))/pi


%for 2nd and 3rd line pair
a1=(cosh((pi/2)*sratioh23)+1)*cosh((pi/2)*Nse);

b1=(cosh((pi/2)*.0277)-1);

wratioh23=(acosh(.5*(a1+b1))-((pi/2)*sratioh23))/pi


%required resonator
%for 1st & 4th line


yo=sqrt(1+(12/wratioh12));


po=(er-1)/2;

so=(1/yo)*po;

do=(er+1)/2;

Ere=so+do

lamda= 300/(1.575*sqrt(Ere))

L=lamda/4
```

y2=sqrt(1+(12/wratioh23));

p2=(er-1)/2;

s2=(1/y2)*p2;

d2=(er+1)/2;

Ere2=s2+d2

lamda2= 300/(1.575*sqrt(Ere2));

L2=lamda2/4

HSpice Code

*CSO.sp

.include cmosedu_models.txt

.option post=2 nomod

M1 N008 N002 N012 0 N_50n l=50n w=.5u

M2 N003 N002 N008 VDD P_50n l=50n w=1u

M3 VDD N001 N003 VDD P_50n l=50n w=1u

M4 N012 in 0 0 N_50n l=50n w=.5u

M5 N009 N008 N013 0 N_50n l=50n w=.5u

M6 N004 N008 N009 VDD P_50n l=50n w=1u

M7 VDD N001 N004 VDD P_50n l=50n w=1u

M8 N013 in 0 0 N_50n l=50n w=.5u

M9 N010 N009 N014 0 N_50n l=50n w=.5u

M10 N005 N009 N010 VDD P_50n l=50n w=1u

M11 VDD N001 N005 VDD P_50n l=50n w=1u

M12 N014 in 0 0 N_50n l=50n w=.5u

M13 N011 N010 N015 0 N_50n l=50n w=.5u

M14 N006 N010 N011 VDD P_50n l=50n w=1u

M15 VDD N001 N006 VDD P_50n l=50n w=1u

M16 N015 in 0 0 N_50n l=50n w=.5u

M17 N002 N011 N016 0 N_50n l=50n w=.5u

M18 N007 N011 N002 VDD P_50n l=50n w=1u

M19 VDD N001 N007 VDD P_50n l=50n w=1u

M20 N016 in 0 0 N_50n l=50n w=.5u

M21 N001 in 0 0 N_50n l=50n w=.5u

M22 VDD N001 N001 VDD P_50n l=50n w=1u

M23 osc_out N002 0 0 N_50n l=50n w=.5u

M24 VDD N002 osc_out VDD P_50n l=50n w=1u

Vin in 0 1

VDD VDD 0 DC 1

.op

.end

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