CHAPTER ONE

INTRODUCTION

We are living in the information age. Large amounts of information can be obtained via the Internet, for example, and can also be obtained quickly over long distance satellite communication systems. The development of the transistor and the integrated circuit has lead to these remarkable capabilities. The IC permeates almost every facet of our daily lives, including such things as the compact disc player, the fax machine, laser scanners at the grocery store, and the cellular telephone. One of the most dramatic examples of IC technology is the digital computer-a relatively small laptop computer today has more computing capability than the equipment used to send a man to the moon.

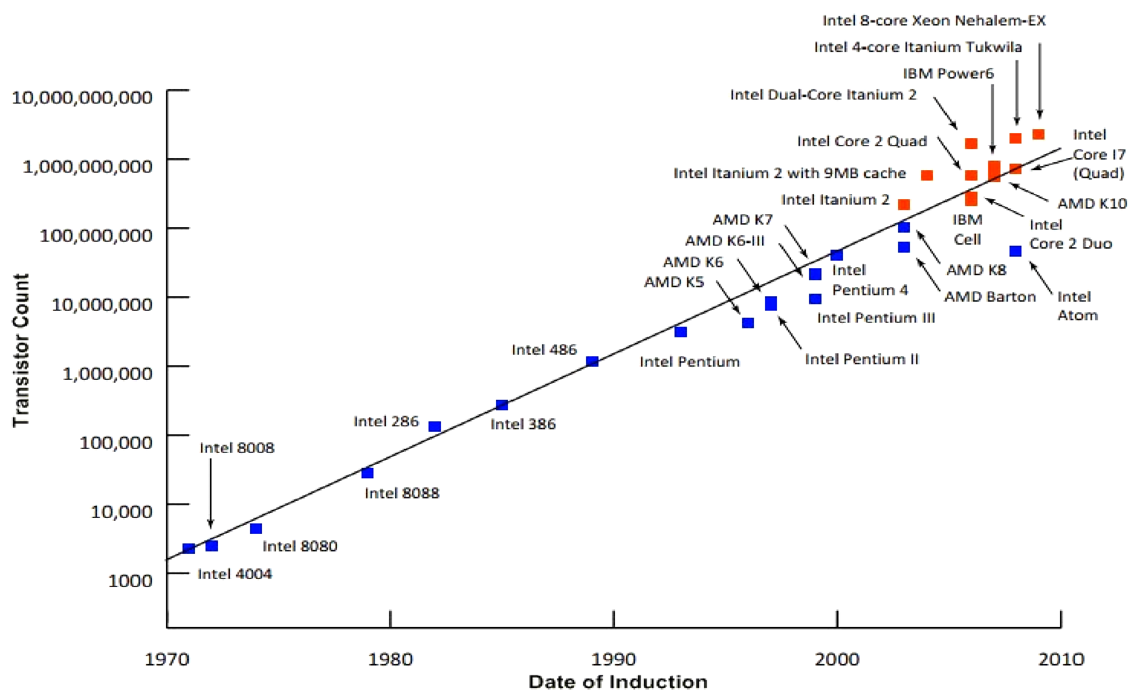


Figure 1.1: Plot of CPU transistor counts against dates of introduction; the line corresponds to exponential growth with transistor count doubling every two years [2].

A semiconductor electronics field continues to be a fast-changing one, with thousands of technical papers published each year, [1]. The fast changing semiconductor device technology follows the Moore's law, i.e.; device counts double every 18 months. The revolutionary nature of Moore's law is indicated by the way in which the number of transistors integrated in circuits on a single chip has grown, as indicated in figure 1.1.

1.1Basic structure of FETs

For more than four decades, transistors have been shrinking exponentially in size, and therefore the number of transistors in a single microelectronic chip has been increasing exponentially. Such an increase in packing density was made possible by continually shrinking the metal–oxide–semiconductor field-effect transistor (MOSFET).

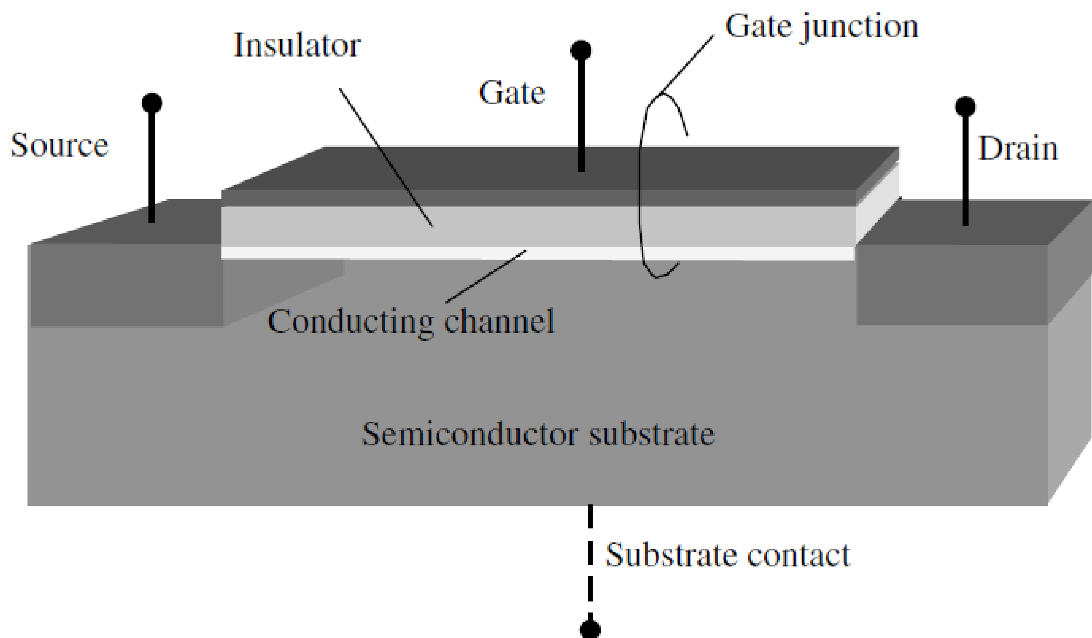


Figure 1.2: Schematic illustration of a generic field effect transistor. This device can be viewed as a combination of two orthogonal two-terminal devices [3].

1.2 Basic structure of MOSFETs

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a type of transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals,[4] the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

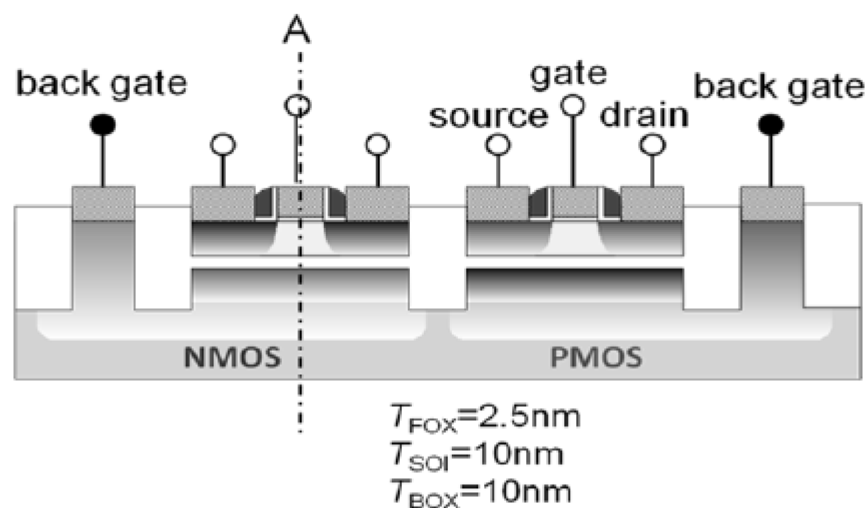


Figure 1.3: Schematic of silicon on ultrathin BOX MOSFET developed for Ultra low power applications with a conventional bulk-MOSFET technology [5]

A real MOS structure always contains so-called ‘‘oxide charges’’ located in the bulk of the oxide or at the oxide-silicon interface [6]. In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts via the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer. The channel can contain electrons (called an n MOSFET or nMOS), or

holes (called a pMOSFET or pMOS), opposite in type to the substrate, so nMOS is made with a p-type substrate, and pMOS with an n-type substrate (see article on semiconductor devices). In the less common depletion mode MOSFET, detailed later on, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and conductivity is decreased by application of a field that depletes carriers from this surface layer [7]. A metal–oxide–semiconductor field-effect transistor (MOSFET) is based on the modulation of charge concentration by a MOS capacitance between a body electrode and a gate electrode located above the body and insulated from all other device regions by a gate dielectric layer which in the case of a MOSFET is an oxide, such as silicon dioxide. If dielectrics other than an oxide such as silicon dioxide (often referred to as oxide) are employed the device may be referred to as a metal–insulator–semiconductor FET (MISFET). Compared to the MOS capacitor, the MOSFET includes two additional terminals (source and drain), each connected to individual highly doped regions that are separated by the body region. These regions can be either p or n type, but they must both be of the same type, and of opposite type to the body region. The source and drain (unlike the body) are highly doped as signified by a "+" sign after the type of doping [8]. If the MOSFET is an n-channel or nMOS FET, then the source and drain are "n+" regions and the body is a "p" region. If the MOSFET is a p-channel or pMOS FET, then the source and drain are "p+" regions and the body is an "n" region. The source is so named because it is the source of the charge carriers (electrons for n-channel, holes for p-channel) that flow through the channel; similarly, the drain is where the charge carriers leave the channel [9].Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. Robert Dennard's work on scaling theory was pivotal in recognizing that this ongoing reduction was possible. Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009. The semiconductor industry maintains a "roadmap", the ITRS, [10] which sets the pace for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication

process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (small MOSFETs exhibit higher leakage currents, and lower output resistance, discussed below).

1.3 Multigate MOSFETs

Conventional planar CMOS transistors on bulk silicon substrate have been a key component in ultra large scale integration (ULSI) technology for the past four decades. As planar CMOS transistors keep following a trend of downscaling, they are also approaching the fundamental physical limits imposed by the presence of several detrimental effects, such as gate oxide tunneling and short-channel effects (SCEs) [11], [12]. Until recently, many performance metrics (i.e. speed, total harmonic distortion, etc.) of the conventional MOSFET have generally improved with each scaling. But as channel lengths approach and fall below 100 nm, new characteristics are observed; many of them are undesirable. During the last few decades, an extraordinary effort has been made to improve semiconductor-device features while reducing their dimensions. In order to follow the predictions of the International Technology Roadmap for Semiconductors [13], new materials and architectures have been proposed.

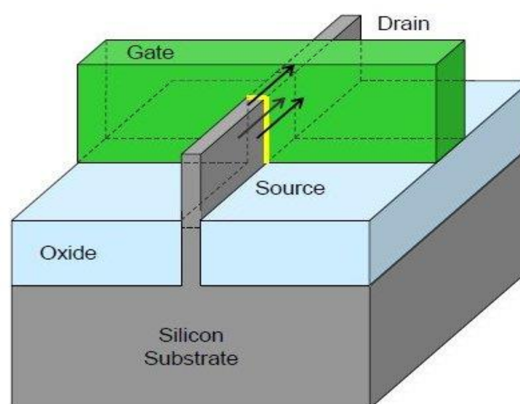


Figure 1.4: Multigate MOSFET [14]

In the current generation of transistors, the transistor dimensions have shrunk to such an extent that the electrical characteristics of the device can be

markedly degraded, making it unlikely that the exponential decrease in transistor size can continue. Recently, however, a new generation of MOSFETs, called multigate transistors, has emerged, and this multigate geometry will allow the continuing enhancement of computer performance into the next decade [15]. A multigate device or multiple gate field-effect transistor (MuGFET) refers to a MOSFET (metal–oxide–semiconductor field-effect transistor) which incorporates more than one gate into a single device. The multiple gates may be controlled by a single gate electrode, wherein the multiple gate surfaces act electrically as a single gate, or by independent gate electrodes. A multigate device employing independent gate electrodes is sometimes called a Multiple Independent Gate Field Effect Transistor (MIGFET).

1.3.1 SOI MOSFETs

Ultrathin-Film transistors are getting more attraction due to superior short-channel control and suppression of device variability originated by the dopant fluctuation [16], [17]. A big advantage of the planar thin-film transistor in comparison to advanced 3-D configuration is that the technology is rather compatible with existing CMOS technologies, and thus existing circuit designs are easier transferable.

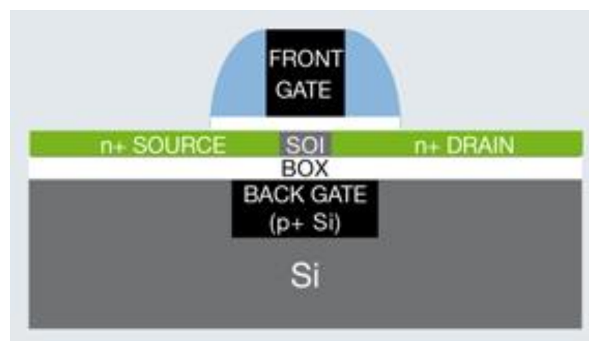


Figure 1.5: SOI MOSFET [22]

The silicon on insulator (SOI) MOSFET is one of such transistor structures developed for ultra low power applications [18]. Modeling of SOI-MOSFETs has been investigated for a long time, and most effort was given to describe the partially depleted condition [19], [20]. Conventional compact models are developed based on the threshold voltage V_{Th} description, and the floating potential value within the SOI layer at BOX is often analytically described [21].

1.3.2 Double gate SOI MOSFETs

As the scaling of conventional MOSFETs approaches its technological limit, the double-gate MOSFETs have emerged as an important candidate for the future device in the nanoscale era [23]. The device structure in which the channel is sandwiched between the two gates reforms the drain electric field ideally, and can effectively avoid the short channel effects (SCEs) which is caused by the distorted drain electric field in the small device [24]. SCE avoidance is not all that the double-gate device can provide. As a novel device with an additional terminal, the double-gate MOSFETs can lead us to a new research area for the novel circuit techniques [25]. The double-gate MOSFET (Fig) is a promising structure for CMOS scaling into the sub-30 nm regime [26]. This structure utilizes a very thin body to eliminate sub-surface leakage paths between the source and drain, and thereby provides excellent control of short-channel effects. The use of a lightly doped or undoped body is desirable for immunity against dopant fluctuation effects which give rise to threshold-voltage variation and also for reduced drain-to-body capacitance and higher carrier mobility which provide for improved circuit performance. The threshold voltage of a lightly doped DGMOSFET is adjusted by tuning the work function of the gate material [27]

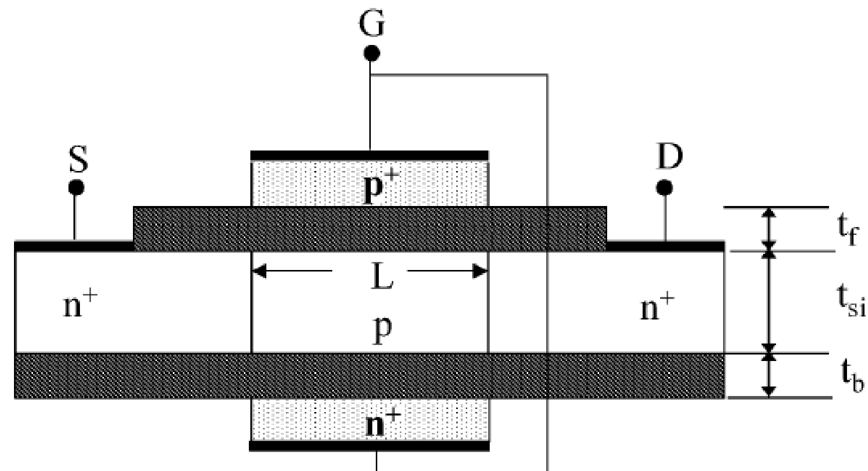


Figure 1.6: Double gate SOI MOSFET [28]

The double gate SOI MOSFETs is a natural extension from a slandered SOI device. The double gate devices rise to many performances enhancements such as increased Tran conductance and a lower threshold voltage. Double gate MOSFETs can be classified in two types (a) symmetrical devices, (b) asymmetrical devices: in symmetrical double gate setup, the back silicon oxide layer has the same thickness as the front silicon oxide layered and also identical gate materials (e.g. near mid –gap metals). This allows both gates to influence the operation of the device. Where for asymmetric devices, different strength can be obtained by different oxide thickness or material of different work function as (e.g. N+ poly & p+ poly) for the front &back gate. When voltage is applied to the gates of the device, the active silicon region is so thick that the control region of the silicon remains controlled by the majority carriers in the region. This causes not one but two channels to be formed. One channel form near the top boundary between silicon and the silicon insulator, the other one form likewise at the bottom interface. The total current through the device is equal to the sum of the currents through the separates channel [29][30][31].

1.3.3 Triple gate SOI MOSFETs (Fin-FETs)

The decreased feature size of metal-oxide-semiconductor (MOS) devices in ultra-large-scale-integrated circuits (ULSIs) requires the nano-scale complementary MOS (CMOS) fabrication technology. Standby power consumption in CMOS devices is now one of the most serious problem and becoming a limiting factor in MOSFET scaling [32]. Short channel effects (SCEs) such as threshold voltage (V_{Th}) roll off and sub-threshold slope degradation causes significant increased in power consumption. Fortunately, non-planar double-gate (DG) MOSFETs provide a potential solution for power consumption issues in ULSIs [33]. They have fundamental advantages of excellent short-channel effects (SCEs) immunity and high current drivability [33]. Among several types of DG MOSFETs, a fin-type DG MOSFET (FinFET) has widely been investigated thanks to its process compatibility with the conventional planar MOSFET [34]. In usual three-terminal (3T) FinFETs as shown in Figure1.7,the threshold voltage (V_{Th}) is changed from the conventional planar MOSFET and is too low for the NMOS(below0 V) when the gate is made of n+ polycrystalline-silicon (poly-Si) and the channel doping is low [35]. Therefore, an additional process is required to adjust a proper threshold voltage. Mostly, the threshold voltage of a MOSFET is defined at the surface condition of φ_{σ} =2φ_{f} where the strong inversion is reached. This definition is inadequate for the UTC DG MOSFET, where the current flows by a weak volume inversion mechanism [35]. To adjust the threshold voltage of DG MOSFETs properly, selection of a midgap gate material is one of the solutions. The other solution is using a poly-Si gate and to increase the threshold voltage with increasing channel doping concentration. However, introduction of a new gate-metal requires additional process optimization. Also, Coulomb scattering due to the dopant atoms causes severe degradation in the mobility of the carrier [36]. To overcome these difficulties, V_{Th} -controllable four-terminal (4T) FinFETs have been proposed and demonstrated by separating the gate electrode using a chemical-mechanical- polishing (CMP) process [37], [38]. Moreover, for the future ultralow power circuits design, the flexible control of the V_{Th} will inevitably be required. High drive current and excellent V_{Th} controllably have experimentally been confirmed in the fabricated 4T FinFETs.

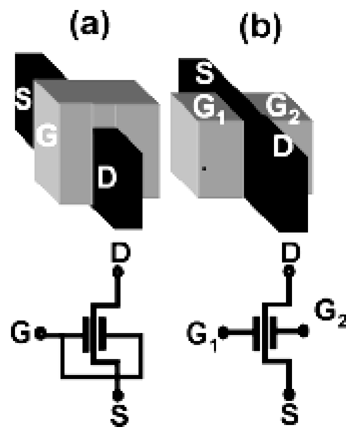


Figure 1.7: Schematic illustration of the 3T and 4T FinFETs fabricated using a SO substrate [37],[38].

Tri-gate(TG) field-effect transistors (FETs) such as fin-shaped FETs (FinFETs) have been proposed as the best candidates for sub-100 nm scaling of MOSFETs due to their excellent gate control for suppressing the short channel effects (SCEs) and proximity to standard bulk planar CMOS processing [39], [40]. Undoped or lightly doped silicon channels are preferred to reduce random dopant fluctuation and, therefore, to eliminate the threshold voltage and mobility variability [41]. Tri-gate or 3D transistor fabrication is used by Intel Corporation for the nonplanar transistor architecture used in Ivy Bridge and Haswell processors. These transistors employ a single gate stacked on top of two vertical gates allowing for essentially three times the surface area for electrons to travel. Intel reports that their tri-gate transistors reduce leakage and consume far less power than current transistors. This allows up to 37% higher speed, or a power consumption at under 50% of the previous type of transistors used by Intel[42][43].Intel explains, "The additional control enables as much transistor current flowing as possible when the transistor is in the 'on' state (for performance), and as close to zero as possible when it is in the 'off' state (to minimize power), and enables the transistor to switch very quickly between the two states (again, for performance)."[44] Intel

has stated that all products after Sandy Bridge will be based upon this design. Intel was the first company to announce this technology. In September 2002,[45]Intel announced their creation of 'Triple-Gate Transistors' to maximize 'transistor switching performance and decreases power-wasting leakage'. A year later in September 2003, AMD announced it was working on similar technology at the International Conference on Solid State Devices and Materials[46][47]. No further announcements of this technology were made until Intel's announcement in May 2011 although it was stated at IDF 2011, that they demonstrated a working SRAM chip based on this technology at IDF 2009.[48]

1.3.4 Double gate vs. tri gate MOSFETs

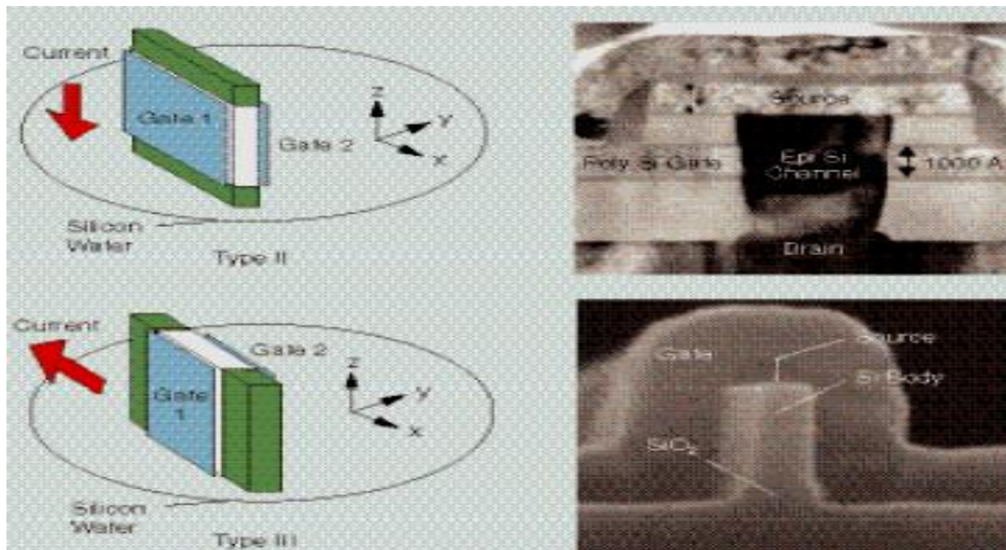


Figure 1.8: Three categories of DG-FET structures describe a large variety of schemes used over the last two decades in attempts to realize DGCMOS (inset SEMs reprinted with permission from [49]–[51]).

Numerous structures for DG-FETs have been proposed and demonstrated. These structures may be classified into one of three basic categories [52] illustrated in Figure 1.8, namely: Type II, the vertical DG, in which the silicon body has been rotated to a vertical orientation on the silicon wafer with the Source and drain on the top and bottom boundaries of the body, and the gates on either side. Type III, today most commonly referred to as a Fin- FET (with

the silicon resembling the dorsal fin of a fish), in which again the silicon body has been rotated on its edge into a vertical orientation so only the source and drain regions are placed horizontally about the body, as in a conventional planar FET.

1.4 FinFET technology –a brief review

Scaling of planar FET's has continued to provide performance, power, and circuit density improvements, up to the 22/20nm process node. Although active research on FinFET devices has been ongoing for more than a decade, their use by a production fab has only recently gained adoption[53]. The basic cross-section of a single FinFET is shown in Figure 1.9. The key dimensional parameters are the height and thickness of the fin. As with planar devices, the drawn gate length (not shown) separating the source and drain nodes is a "critical design dimension". As will be described in the next installment in this series, the h_{fin} and t_{fin} measures are defined by the fabrication process, and are not design parameters[54].

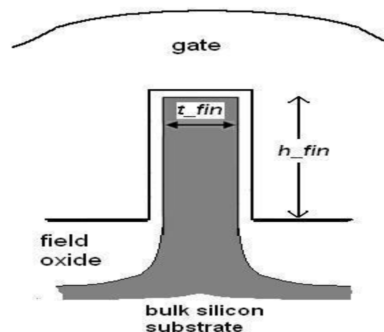


Figure 1.9: FinFET cross-section, with gate dielectric on fin sidewalls and top, and bulk silicon substrate [54]

The FinFET cross-section depicts the gate spanning both sides and the top of the fin. For simplicity, a single gate dielectric layer is shown, abstracting the complex multi-layer dielectrics used to realize an "effective" oxide thickness (EOT). Similarly, a simple gate layer is shown, abstracting the multiple materials comprising the (metal) gate. In the research literature, FinFETs have also been

fabricated with a thick dielectric layer on top, limiting the gate's electrostatic control on the fin silicon to just the sidewalls. Some researchers have even fabricated independent gate signals, one for each fin sidewall – in this case, one gate is the device input and the other provides the equivalent of FET “back bias” control. For the remainder of this series, the discussion will focus on the gate configuration shown, with a thin gate dielectric on three sides. (Intel denotes this as “Tri-Gate” in their recent IvyBridge product announcements. Due to the more complex fabrication steps (and costs) of “dual-gate” and “independent-gate” devices, the expectation is that these alternatives will not reach high volume production, despite some of their unique electrical characteristics. Another fabrication alternative is to provide an SOI substrate for the fin, rather than the bulk silicon substrate shown in the figure. In this series, the focus will be on bulk FinFETs, although differences between bulk and SOI substrate fabrication will be highlighted in several examples.

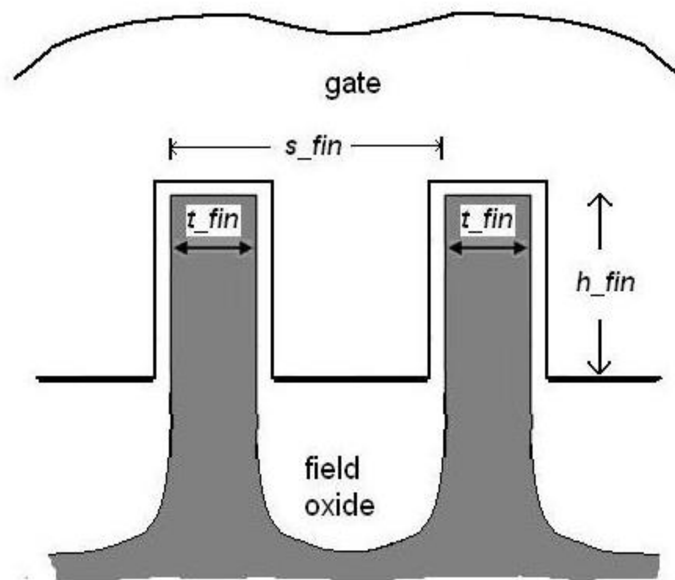


Figure 1.10: Multiple fins in parallel spaced s_fin apart, common gate input[54]

Figure 1.10 illustrates a cross-section of multiple fins connected in parallel, with a continuous gate material spanning the fins. The Source and Drain nodes of the parallel fins are not visible in this cross-section – subsequent figures will show the layout and cross-section view of parallel S/D connections. The use of parallel fins to provide higher drive current introduces a third parameter, the local fin spacing (S_{fin}). Simplistically, the effective device width of a single fin is:

$(2*h_{fin} + t_{fin})$, the total measure of the gate's electrostatic control over the silicon channel. The goal of the fabrication process would be to enable a small fin spacing, so that the FinFET exceeds the device width that a planar FET process would otherwise provide: $S_{fin} < (2*h_{fin} + t_{fin})$. Subsequent discussions in this series will review some of the unique characteristics of FinFETs, which result in behavior that differs from the simple (2*h + t) channel surface current width multiplier. The ideal topology of a “tall, narrow” fin for optimum circuit density is mitigated by the difficulties and variations associated with fabricating a high aspect ratio fin. In practice, an aspect ratio of (h_{fin}/t_{fin} ~2:1) is more realistic. One immediate consequence of FinFET circuit design is that the increments of device width are limited to (2h + t), by adding another fin in parallel. Actually, due to the unique means by which fins are patterned, a common device width increment will be (2*(2h+t)), as will be discussed in the next installment in this series. The quantization of device width in FinFET circuit design is definitely different than the continuous values available with planar technology. However, most logic cells already use limited device widths anyway, and custom circuit optimization algorithms typically support “snapping” to a fixed set of available width values. SRAM arrays and analog circuits are the most impacted by the quantized widths of FinFET's – especially SRAM bit cells, where high layout density and robust readability/write ability criteria both need to be satisfied. The underlying bulk silicon substrate from which the fin is fabricated is typically undoped (i.e., a very low impurity concentration per cm^3). The switching input threshold voltage of the FinFET device (V_{Th}) is set by the work function potential differences between the gate, dielectric, and (undoped) silicon materials. Although the silicon fin impurity concentration is effectively undoped, the process needs to introduce impurities under the fin as a channel stop, to block “punch through” current between source and drain nodes from carriers not controlled electrostatically by the gate input. The optimum means of introducing the punch through-stop impurity region below the fin, without substantially perturbing the (undoped) concentration in the fin volume itself, is an active area of process development. Modern chip designs expect to have multiple V_{Th} device offerings available – e.g., a “standard” V_{Th}, a “high” V_{Th}, and a “low” V_{Th} – to enable cell-swap optimizations that trade-off performance versus (leakage) power. For example, the delay of an SVT-based logic circuit

path could be improved by selectively introducing LVT-based cells, at the expense of higher power. In planar fabrication technologies, multiple V_{Th} device offerings are readily available, using a set of threshold-adjusting impurity implants into masked channel regions. In FinFET technologies, different device thresholds would be provided by alternative gate metallurgy, with different work function potentials. The availability of multiple (nFET and pFET) device thresholds is a good example of the tradeoffs between FinFET's and planar devices. In a planar technology, the cost of additional threshold offerings is relatively low, as the cost of an additional masking step and implant is straightforward. However, the manufacturing variation in planar device V_{Th}'s due to "channel random dopant fluctuation" (RDF) from the implants is high. For FinFET's, the cost of additional gate metallurgy processing for multiple V_{Th}'s is higher – yet, no impurity introduction into the channel is required, and thus, little RDF-based variation is measured. (Cost, performance, and statistical variation comparisons will come up on several occasions in this series of articles.) The low impurity concentration in the fin also results in less channel scattering when the device is active, improving the carrier mobility and device current [55][56][57].

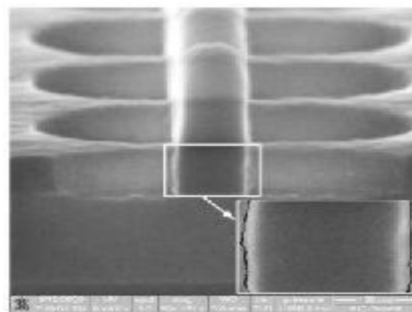


Figure 1.11: SEM cross-section of multiple fins. Gate edge roughness over the fin is highlighted in the expanded inset picture.[54]

Conversely, FinFET's introduce other sources of variation, not present with planar devices. The fin edge "roughness" will result in variation in device V_{Th} and drive current. (Chemical etch steps that are selective to the specific silicon crystal surface orientation of the fin sidewall are used to help reduce roughness. The characteristics of both planar and FinFET devices depend upon Gate Edge Roughness, as well. The fabrication of the gate traversing the topology over

and between fins will increase the GER variation for FinFET devices, as shown in Figure 1.11.

1.5 Literature Review

Several authors have carried out studies on Tri gate FinFET among which compact modeling of FinFET, leakage current, width quantization property have received considerable attention. Gu, et al. in their research paper "Statistical Leakage Estimation of Double Gate FinFET Devices Considering the Width Quantization Property" use research methodology to analyze a statistical leakage estimation method for FinFET devices considering the unique width quantization property. In this paper Monte Carlo simulations show that the conventional approach underestimates the average leakage current of FinFET devices by as much as 43% while the proposed approach gives a precise estimation with an error less than 5%[58]."Compact Modeling of Nanoscale Trapezoidal FinFETs" by Fasarakis, et al. contains an analytical compact model for the drain current of undoped or lightly doped nanoscale FinFETs with trapezoidal cross section[59]. The compact model of rectangular FinFETs is extended to trapezoidal FinFETs using equivalent nonplanar device parameters and corner effects. Rasouli, et al. in their paper "Design Optimization of FinFET Domino Logic Considering the Width Quantization Property" discerns that design optimization of FinFET domino logic is particularly challenging due to the unique width quantization property of FinFET devices [60]. Considering the width quantization property, this paper presents a statistical framework, which provides a reliable design window for keeper sizing to meet the noise margin constraint for the practical range of threshold voltage variation in sub-32-nm technology nodes. This paper also introduces a novel methodology for FinFET-based keeper design, which exploits the exclusive property of FinFET devices. Pablo, et al. Hu make an endeavour to propose a unified FinFET compact model for devices with complex fin cross-sections[61]. The proposed model accurately predicts the current-voltage characteristics of different FinFETs structures such as Double-Gate (DG), Trapezoidal Triple-Gate (T-TG), Cylindrical Gate-All-Around (Cy-GAA), or

Rectangular Gate-All-Around (Re-GAA) FinFETs. In the paper “Process Technology Variation” written by Kuhn, et al. the researchers attempt to quantify the key role of process variation in modern transistor technology[62]. To benchmark random V_{Th} variation this paper introduces an analytical expression for variation as a function of fundamental process parameters. This paper also shows off-state leakage variation with device width. Gaurav Saini and Ashwani K Rana make an attempt to analyze the scaling limits of Double Gate (DG) underlap and Triple Gate (TG) overlap FinFET structure using 2D and 3D computer simulations respectively in the paper “Physical Scaling Limits of FinFET Structure: A Simulation Study” [63]. To analyze the scaling limits of FinFET structure, in this paper simulations are performed using three variables: fin thickness, fin-height and gate-length. From 2D simulation of DG FinFET, it is found that the gate-length(L) and fin-thickness (Tfin) ratio plays a key role while deciding the performance of the device. Pablo, et al. to promote a universal core model for multiple-gate field-effect transistors (Mug-FETs)in the paper “A universal core model for multiple gate field-Effect transistors.Part I:Charge model” by assuming an arbitrary channel potential profile, which simplifies the mathematical formulation. The researchers perceives that the proposed model can be expressed as an explicit and continuous form for all operation regimes; therefore, it is well suited for compact modeling to support fast circuit simulations[64]. These researchers touches on the drain current model in the paper “A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part II: Drain Current Model”. Using this charge model in Part I, Pao–Sah’s integral is analytically carried out by approximating its integrand in this paper[65]. The model describes both the subthreshold inversion for undoped FETs and the effects of finite doping density in the channel. “Threshold-Voltage Modeling of Bulk Fin Field Transistors by Considering Surface Potential Lowering” by Byung-Kil CHOI and Jong-Ho LEE presents threshold voltage (V_{Th}) modeling of the double/triple-gate bulk fin field-effect transistors (FinFETs), performed by considering the potential lowering at the surface of fin body at V_{GS}=V_{Th} condition. The paper addresses V_{Th} behaviors of bulk FinFETs based on the surface potential lowering, three-dimensional (3-D) charge-sharing, narrow-width effect, and corner factor. The threshold voltages V_{Th} of the body-tied double/triple-gate MOSFETs (bulk FinFETs)

implemented on bulk silicon (Si) wafers were modeled systematically in the paper “Threshold-Voltage Modeling of Body-Tied FinFETs (Bulk FinFETs)” by Choi, et al[66]. The writers find out that the model predicts the V_{Th} behavior with fin body thickness, body doping concentration, gate height, gate length, and corner shape of the fin body. Shiying Xiong and Jeffrey Bokor investigate the manufacturability of 20-nm double-gate and FinFET devices in integrated circuits by projecting process tolerances in the paper “Sensitivity of Double-Gate and FinFET Devices to Process Variations”[67]. In this paper the sensitivity of threshold voltage to random dopant fluctuation was studied by Monte Carlo simulation. The authors make an endeavour to analyze the sensitivity of device electrical parameters to several important physical fluctuations such as the variations in gate length, body thickness, and gate dielectric thickness. “Impact of Device Parameters of Triple Gate SOI-Finfet on The Performance of Cmos Inverter At 22nm” by Prathima, et al. demonstrates a simulation based design evaluation for SOI FinFETs at 22nm gate length [68]. This paper reveals that for a given gate oxide thickness increasing the fin height and fin width degrades the SCEs, while improves the performance. It is found that reducing the fin thickness was beneficial in reducing the off state leakage current (I_{OFF}), while reducing the fin height was beneficial in reducing the gate leakage current (I_{GATE}). The paper “Dependability Analysis of Nano-scale FinFET circuits” by Wang, et al. provides the dependability analysis of FinFET circuits, studying the impact of process variation. This paper concluded that FinFET-based circuit design is more robust than the bulk CMOS based circuit design. “FinFETs for Nanoscale CMOS Digital Integrated Circuits” by Tsu-Jae King presents an overview of FinFET technology and describes how it can be used to improve the performance, standby power consumption, and variability in nanoscale-CMOS digital ICs. A comprehensive full-scale 3D simulation study of statistical variability and reliability of FinFet devices is examined in the paper “Statistical Variability and Reliability in Nanoscale FinFETs” by Wang, et al. Excellent electrostatic integrity and resulting tolerance to low channel doping are perceived as the main FinFET advantages, resulting in a dramatic reduction of statistical variability due to random discrete dopants (RDD). It is found that line edge roughness (LER), metal gate granularity (MGG) and interface trapped charges (ITC) dominate the parameter fluctuations with different distribution

features, while RDD may result in relatively rare but significant changes in the device characteristics. A complete FinFET structure analysis is given in the paper “FinFET Architecture Analysis and Fabrication Mechanism” by Hadia , et al. [69]. This paper mainly deals with detail description about the DG MOSFET structure and its particular type named as FinFET technology and its fabrication mechanism.

CHAPTER TWO

THEORITICAL OVERVIEW

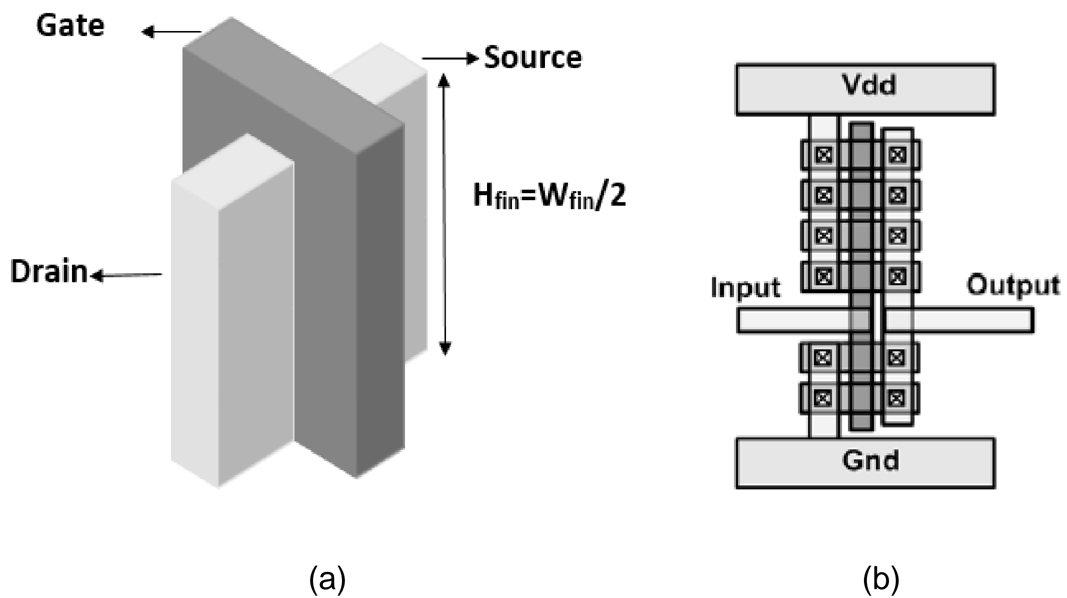
Triple-gate FinFET devices are considered as one of the most promising successors of conventional MOSFET devices because of the suppressed short channel effect, near-ideal subthreshold swing, and compatible process to existing SOI or bulk technologies. Due to the physical fin structure, the width of a FinFET device is quantized. This chapter developed a statistical leakage model for RDF induced threshold voltage variation. The atomistic RDF where the dopant's location also affects the overall V_{Th} is considered in the developed model. Compared with the conventional approach, the proposed model can estimate the width-dependent leakage distribution under atomistic RDF more accurately. In this work, we show that the impact of width quantization on statistical leakage estimation is significant for FinFET devices.A precise statistical leakage model is indispensable in modern VLSI design because the leakage variation not only leads to unpredictable power consumption but also poses serious threat to the circuit functionality. Statistically, leakage and V_{Th} of an individual device has a strong dependency on the device width due to atomistic RDF. In this work we developed a leakage estimation methodology which can accurately capture the statistical characteristics of leakage current under process variation. Monte Carlo simulation has been used to prove the accuracy of the proposed method. This chapter proposes a statistical leakage modeling approach which is capable of more accurately estimating the width-dependent leakage distribution under random dopant fluctuation than the conventional approach.

2.1 Introduction to FinFET Device

Conventional bulk CMOS scaling beyond 45nm is severely constrained by short channel effects and vertical gate insulator tunneling [70]. Double-gate FinFET technology [71][72][73][74] has been proposed as a very promising candidate to circumvent the conventional bulk CMOS scaling constraint, by changing the device structure in such a way that MOSFET gate length can be scaled further even with thicker oxide, so that we can continue scaling beyond the limit of conventional bulk CMOS. One of the grand challenges for nano-scale VLSI designers is guaranteeing dependability. Shrinking geometries, lower supply voltage, and higher frequencies, all have a negative impact on circuit dependability: the occurrences of soft errors increases due to these factors, and higher levels of device parameter variations change the design problem from deterministic to probabilistic. Consequently, reducing soft error rate and mitigating the impact of process variation are becoming increasingly critical. Both logic and SRAM FinFET technologies have been previously demonstrated [71][72]. the reliability and scalability analysis for FinFET circuits, showing that FinFET circuits have better soft error immunity, as well as less impact of process variation on the performance, comparing against the bulk CMOS counterparts.

Tripple-gate FinFET transistors are recognized as one of the most promising successors of traditional planar bulk devices in the sub-25nm regime due to the significantly reduced leakage current, excellent short channel behavior, and fabrication process which is compatible with existing SOI or bulk technology processes. The FinFET transistor shown in Fig. 2.1(a) is a quasi-planar Triple-gate device with a thin fin structure as the body. One can understand it as a planar triple gate device turned on its edge; i.e. the height of the device corresponds to the width of an equivalent planar device. Triple-gate FinFETs have a front and back inversion channel, so the effective transistor width of a single fin is twice the fin height; i.e.Wfin=2H. The body thickness T_{Si} is made extremely thin so that short channel effect is suppressed and the subthreshold leakage is reduced via the improved subthreshold swing. Leakage of a CMOS device is determined by the subthreshold swing defined as the change in gate voltage that yields 10X change in subthreshold current [75]. Smaller

subthreshold swing translates into less subthreshold leakage for the same V_{Th}. Bulk devices typically observe a subthreshold swing greater than 100mV/dec, while FinFET devices have a near-ideal subthreshold swing of around 80mV/dec at 110°C.This favorable property stems from the capacitive coupling between the surface potential and both front and back gates [76] .Figure. 2.1 shows a 3-dimensional FinFET structure and the cross section of the FinFETmodel. The FinFET model has symmetrical front and back metal gates which are tied together. Fig. 2.1(d) shows the I-V curve from the FinFETmodel at 110°C showing a subthreshold swing of 83mV/dec. Table 3.1 lists the device parameters of the designed FinFET model used throughout this work. Except the device characterization, all the simulation in this work was carried out by MATLAB using the device parameters found in our FinFET model.



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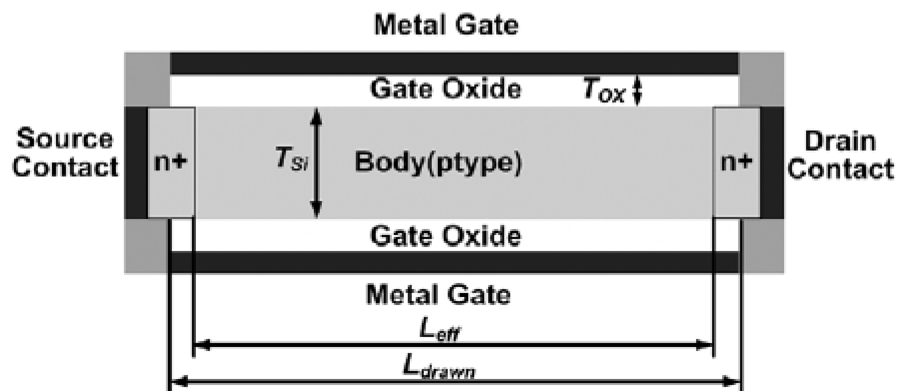

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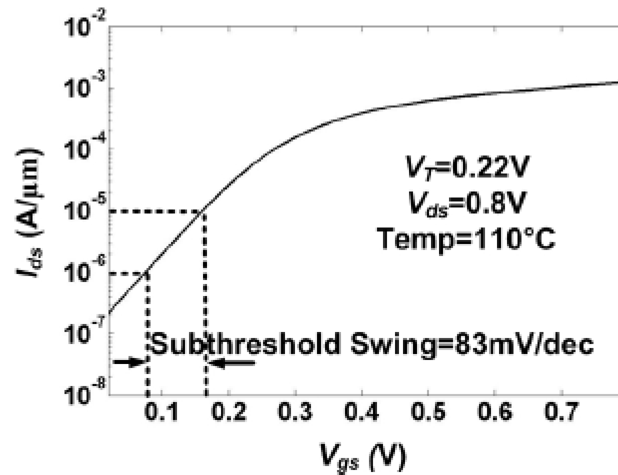


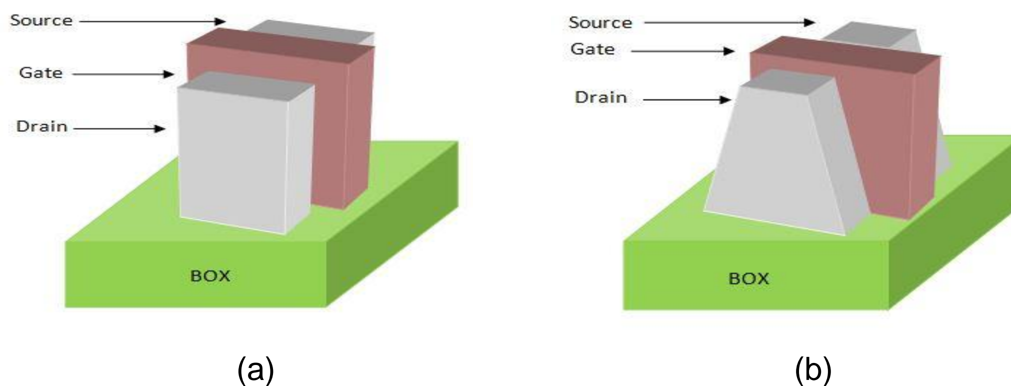
(d)

Figure 2.1: (a) 3D structure of a FinFET device (b) layout example of a width quantized FinFET inverter (c) cross section of a 21nm FinFET model (d) I-V characteristics of the FinFET model showing a near-ideal subthreshold swing of 83mV/dec at 110°C.[77]

Much of the previous work on FinFETs has been done at the device and process level, dealing with issues such as fabricating the FinFET structure, obtaining the desired threshold voltage, and aligning the gate, source, and drain region [78-80].Only few researchers have looked into FinFET design issues at the CAD and circuit level. T. Ludwig advocated DGCMOS-FinFET technology by showing practical circuit implementations for both digital and analog applications [81]. R. V.Joshi compared FinFET-based SRAM cells with planar PD-SOI cells showing reduced delay, less standby power, and small impact on read stability [82]. Z. Guofurther explored design tradeoffs in 6T and 4T FinFET SRAM design [73]. More recently, H. Ananthan proposed a compact physical model to obtain the threshold voltage and leakage distribution of FinFET devices due to gate length and body thickness variation [76,83]. However, the author did not discuss how to extend the single-fin leakage distribution into the distribution of larger multi-fin devices, which is necessary in designing any type of FinFET circuit.

2.1.1 Types of FinFET

Tri-Gate (TG) field-effect transistors (FETs) such as fin-shaped FETs (FinFETs) have been proposed as the best candidates for sub-100 nm scaling of MOSFETs due to their excellent gate control for suppressing the short channel effects (SCEs) and proximity to standard bulk planar CMOS processing [38][39]. Undoped or lightly doped silicon channels are preferred to reduce random dopant fluctuation and, therefore, to eliminate the threshold voltage and mobility variability [84]. Accurate and fast compact models for transistors are one of the main pillars in circuit simulators. Indeed, compact models represent an interface between circuit designers and device technology. The Compact Model Council (CMC) has chosen BSIM-CMG [85] [86] as the first and only industry-standard compact model for FinFETs. The core model used in BSIM-CMG is based on the solution of a rectangular shape TG- FinFET. Figure 2.2(a) shows the conventional rectangular shape FinFET with four fins.



(a) (b)

Figure 2.2: (a) Structure of rectangular shape Tri-gate FinFET
(b) Structure of rectangular shape Tri-gate FinFET

Recently, microscope cross sections of FinFETs from Intel have revealed that the TG transistors are in fact trapezoidal or almost triangular [87]. The trapezoidal cross section is markedly different to the idealized rectangular section investigated previously [88]-[92]. However, it is not clear whether the almost trapezoidal shape of the fin is what bulk FinFET technology can achieve in terms of the fin etching, or is deliberately engineered by Intel to have a critical impact on electron mobility or yield. The electrical properties of TG FinFETs with such nonvertical sidewalls have been investigated only by numerical

simulations [93] [94]. Thus, compact modeling of undoped or lightly doped nanoscale multigate MOSFETs extended from rectangular TG (Re-TG) [Fig. 2.2(a)] to trapezoidal TG (Tz-TG) [Figure. 2.2(b)] is urgently required. The downscaling of planar transistors has brought several detrimental effects such as increment of leakage currents and enhancement of Short-Channel-Effects [11][95]. In this context, FinFET devices (Figure. 2.1) have been recently adopted by the industry as a substitute of conventional bulk planar transistors [96][97]. The adoption of FinFETs solves several problems of planar transistors by improving the electrostatic control of the gate over the entire semiconductor channel, resulting in an increment of on-current and a reduction of Short-Channel-Effects.

Low leakage devices are a key enabler for long-life System-on-Chip applications with ultralow-power standby requirements. While bulk FinFETs show improved leakage performance over planar CMOS, leakage persists due to SCEs and gate-induced drain leakage (GIDL) [98] Leakage due to SCEs decreases as fin widths decreases [99]; however, etching thinner fins is a significant challenge [100]. GIDL, caused by band-to-band tunneling (BTBT), where the drain region extends under the gate, decreases with thinner fins [101]. However, GIDL is difficult to eliminate, because GIDL current increases as the gate WF(Work function) moves away from the band edges and due to the junction abruptness of the fin body doping. Reducing leakage requires sacrificing drive current; therefore, it is desirable to investigate tradeoffs between I_{ON} and I_{OFF}, and to provide chip designers control of the leakage/saturation current tradeoff via a multithreshold technology process. Because FinFET performance is determined in large part by the fin geometry, it is intuitive that fin cross section shape will have an impact on leakage. However, previous studies of fin shape were primarily focused on evaluating the impact on SCEs, and provided only preliminary investigations on leakage. Liu et al. [102]reported that leakage increased in silicon on insulator FinFETs as the fin cross-sectional shape changes from rectangular to triangular to trapezoidal. In their study, the width of the fin base changed from 13 (rectangular) to 92 (triangular) to 140 nm (trapezoidal). We believe that the increase in leakage is due to the increase in fin width, not the change in cross-sectional shape. Recently, Wu et al. [103] reported that fin shape has a

negligible impact on leakage performance. However, this result is neither conclusive nor generalizable as it is specific to a particular fin body doping. Prior multifin threshold FinFET research has focused on SOI (not bulk) FinFET technologies. Proposed multifin threshold techniques for SOI FinFETs include WF engineering, G–S/D overlap, and active fin doping. WF engineering is required to produce functional tri-gate FinFETs with undoped active fins and midgap gate metal WF [104].

Fin shape significantly impacts transistor leakage in bulk tri-gate nFinFETs with thin fins when the fin body doping profile is optimized to minimize leakage. A triangular fin reduces leakage current by 70% [105] over a rectangular fin with the same base fin width.

2.2 Modeling

2.2.1 Atomic RDF induced Threshold voltage variation in FinFET

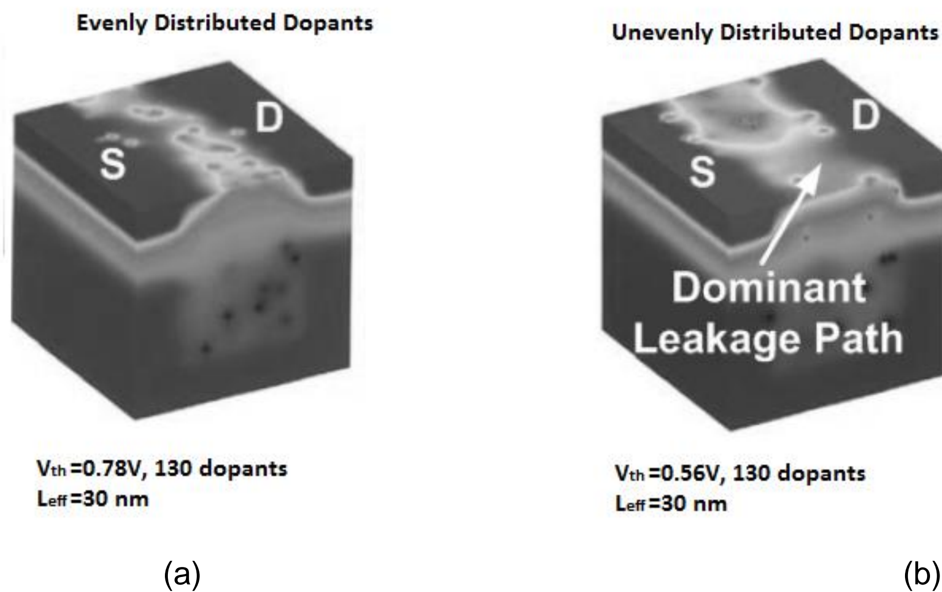
The variation of device leakage poses severe threat to circuit's functionality. The accurate modeling of device leakage consumption under process variation is very important for designer to design robust circuits in nanometer regime. A significant amount of work has been published on the prediction of leakage power under process variation using statistical methods. Based on the given probability density functions (PDFs) of random process parameters, the leakage PDF and cumulative density function (CDF) profile for a large circuit or whole chip has been derived. For example, S. Narendra provided a mathematical model to estimate the mean and standard deviation of full chip subthreshold leakage under intra-die variation based on the statistical leakage distribution of an individual device. The proposed model was verified with measurement results [106]. R. Rao used a similar approach for full-chip leakage prediction but extended the consideration to both intradie and inter-die variation [107]. S. Mukhopadhyay not only developed models for subthreshold leakage, but also considered the gate tunneling leakage and junction band-to-band tunneling (BTBT) leakage [108]. H. Chang further developed a more complete

model which also considers the spatial correlations among inter-die and intra-die process parameters [109].

All of the above work assumes a constant threshold voltage distribution from a single device. However, the threshold voltage distribution of a single device is highly width-dependent and more complicated than the conventional treatment because the random dopant fluctuation not only causes variation of the total doping concentration in a device but also causes an non-uniform placement of dopant atoms inside the device. An example of it is what was previously referred as “atomistic” random dopant fluctuation [110] [111]. Fig. 2.3(a) shows 3D simulation model for atomistic random dopant fluctuation (RDF) inside a device. The conventional description of RDF assumes a uniform distribution of dopant within the device even though the overall doping concentration may vary. In atomistic random dopant fluctuation, not only the overall doping concentration varies but also the placement of dopant atom changes leading to a decrease of threshold voltage, referred by previous publication as “random dopant induced threshold voltage lowering”. This effect is specially pronounced in nanometer regime because as device dimensions scale below 25nm, the number of dopant atoms per device has become very small (≤ 100), and thus V_{Th} can vary significantly due to the fluctuation in the number and placement of dopants. As shown in Figure. 2.3(a), an absence of dopant in a small region inside the channel may open a “tunnel” for the device creating a shift of overall threshold voltage. As enov studied this effect [110]. He simulated and plotted the threshold voltage with a 3D simulator which considered the discrete allocation of dopant atoms. Figure. 3.1(b) shows the results. Compared with the conventional approach assuming a uniform distribution of dopant, the situation with atomistic RDF causes a reduction of the overall threshold voltage of the device and a widening of the distribution curve, or an increase of the standard deviation. Fig. 3.1(b) also shows that the reduction of threshold voltage depends on the width of the devices. As will be shown in the next section, this width dependency of threshold voltage variation has not been modeled properly in conventional approach. H. Wong also observed a similar result [112]. He confirmed that when considering the atomistic RDF, the threshold voltage is shifted negatively. Especially, the threshold voltage shift in subthreshold region

is about 2~3X of that in linear region leading to significant change of leakage power compared with that predicted from uniform RDF. Note that the definition of threshold voltages used in [112] was different for subthreshold region and linear region. The subthreshold V_{Th} was defined as the gate voltage with I_{off} equal to 2nA/μm while the linear region V_T is obtained by extrapolating to zero source current in linear region. The authors uspected that the difference of V_{Th} shift in subthreshold region and linear region comes from the logarithmic dependency of current in subthreshold region. However, no analytical explanation was given for such an effect in any of the above references.

Although the atomistic RDF has been shown in device community for several years, it has not been considered by circuit designer due to the lack of proper model for such an effect. In this work, we will develop a statistical model for the atomistic RDF and shows that the developed model is more accurate than the conventional modeling of the RDF effect. We will also discuss the circuit-level application of the developed model considering the threshold voltage variation due to atomistic RDF.



(a) (b)

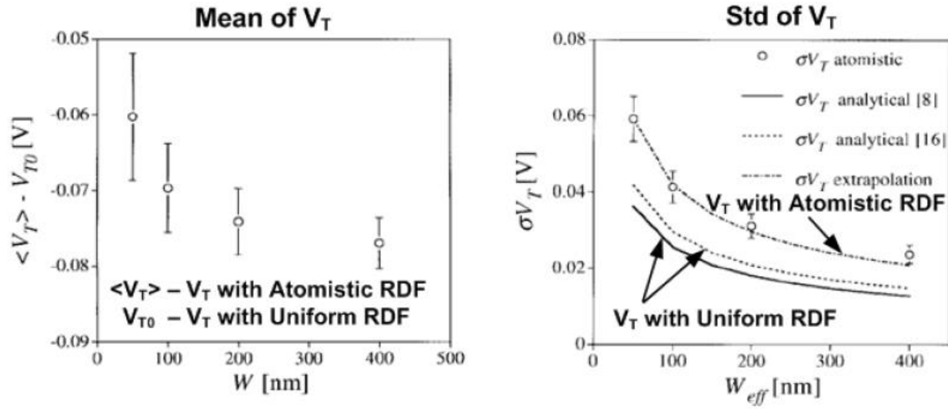


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Figure 2.3: Threshold voltage variation under atomistic random dopant fluctuation. (a) 3D model for CMOS channel region with uniform RDF(left) and atomistic RDF(right) [65]; (b) Simulation results on mean value (left) and standard deviation (right) of $V_{Th}$with uniform RDF and atomistic RDF [65].

Overall V_{Th} variation is a combination of systematic variation and random variation. Systematic variation includes V_{Th} variation due to systematic process variations across a wafer and betweendifferent wafers. They are quantified using V_{Th} measurements on transistors located in different parts of the wafer across multiple wafers. Examples include lithography-driven parameters suchas gate length, implant doping, and film thicknesses (gate oxide, gate poly or metal, spacer, etc.). Random V_{Th} variations, on the other hand, occur across a very short distance on one wafer.They are quantified using V_{Th} measurements on pairs of adjacent, matched transistors. Examples include random dopant fluctuation (RDF) in the transistor channel, poly or metal gate granularity, and transistor gate line edge roughness. The primary cause of random V_{Th} variations in deep submicron technologies is RDF, which describes the statistically random variation in the number of dopant atoms in the transistor channel. RDF is generally considered to cause over 70% of random V_{Th} variations at the 65nm technology node, and RDF becomes even more significant at smaller geometries as transistor channels — and the total number of dopant atoms in the channel — become smaller. Because overall V_{Th} variation has such a significant effect on performance and power consumption in deep submicron process technologies, it requires a statistical approach to product design to account for the variation of device characteristics.

Random threshold voltage variation *(σV_{Th})* is a key factor in determining the memory elements such as SRAMs and register file cells. To bench mark random V_{Th} variation, it is necessary to have an analyticalexpression for variation as a function of fundamental processparameters.

In the pioneering work of Mizuno et al. [113], the analytical expression for σV_{Th} in planar devices due to random dopant fluctuations was shown to be

$$\sigma V_{Th} = \frac{\sqrt[4]{4q^3 \varepsilon_{Si} \phi B}}{2} . \frac{T_{ox}}{\varepsilon_{Si}} . \frac{\sqrt[4]{N_{Si}}}{\sqrt{L_{eff}} We_{ff}} \quad (1)$$

where the key features are a linear dependence on the oxide thickness T_{ox}, an inverse square-root dependence on the effective length and width (L_{eff} and W_{eff}), and an inverse fourth-root dependency on N_{Si} (where N_{Si} is the total doping concentration per unit volume of the same type of species). An expression of a similar form was shown by Stolk et al. [114] with slightly different coefficients as

$$\sigma V_{Th} = \frac{\sqrt[4]{4q^3 \varepsilon_{Si} \phi_B}}{\sqrt{3}} . \left[\frac{k_b T}{q} . \frac{1}{\sqrt{4\varepsilon_{Si}} \phi_B N_{si}} + \frac{T_{ox}}{\varepsilon_{Si}} \right] . \frac{\sqrt[4]{N_{Si}}}{\sqrt{L_{eff}} We_{ff}} \quad (2)$$

In Eq. (2), the first term in the square brackets represents the surface potential fluctuations whereas the second term represents the fluctuations in the electric field. The decrease of the threshold voltage fluctuations with increasing the width of the gate is due to the averaging effects, in agreement with the experimental findings by Horstmann et al. [115]. The increase in the channel doping leads to larger threshold voltage standard deviation V_{th} . These results also imply that the fluctuations in the thresholdvoltage can be even larger in devices in which counter ion implantation is used forthreshold voltage adjustments. Similarly, the increase in the oxide thickness leadsto linear increase in the threshold voltage standard deviation. For FinFET equation 2 can be simplified as [62]

$$\sigma V_{Th} = q\left(\sqrt{\frac{W_{fin}}{2}}\right)\frac{t_{ox}}{\varepsilon_{ox}}\left(\frac{\sqrt{N_{si}}}{\sqrt{L_{eff}W_{eff}}}\right) \tag{3}$$

2.2.2 Statistical V_{Th} model for FinFET Device

This chapter propounds a statistical leakage modeling approach for estimating the leakage distribution of trapezoidal shaped FinFET under random dopant fluctuation by Monte Carlo simulation using MATLAB [116].Compact modeling of device has been preferred in this thesis work for better computational efficiency. The purpose of a statistical leakage estimation tool is to get a specific leakage distribution of a FinFET device based on process inputs such as the mean threshold voltage (V_{Th}) and standard deviation of V_{Th} due to process parameter variation.

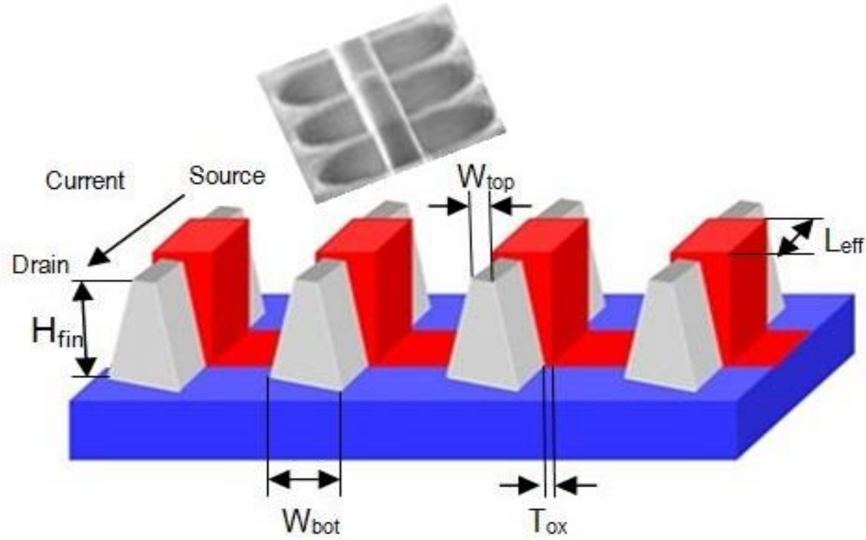


Figure 2.4: Structure of FinFET device having 4 Fins. Inset: SEM image of a FinFET [117]

Figure. 2.4 shows the structure of a 4-fin tri-gate trapezoidal shaped FinFET [118]. Tri-gate FinFET consists of two SOI gates connected together. In our proposed leakage current calculation we have considered this structure.

The expression for threshold voltage (V_{Th}) for trapezoidal FinFET can be obtained from [65]

$$V_{Th} = V_{FB} - \frac{Q_d}{C_g} + 2v_T \ln\frac{N_{si}}{n_i} - v_T \ln\left[\frac{C_{ch}}{C_g}(1 - e^{\frac{Q_d}{v_T C_{ch}}})\right], \tag{4}$$

where V_{FB}, v_T, N_{si}, n_i, C_g, C_{ch}, Q_d represents the flatband voltage, thermal voltage, doping concentration, intrinsic carrier concentration, gate oxide capacitance per unit length channel capacitance per unit length and depletion charge per unit length respectively. Depletion charge per unit length $Q_d$can be calculated as [64]

$$Q_d = -qN_{si}H_{fin}W_{fin}, \tag{5}$$

Where q is the electron charge, H_{fin} is the fin height and W_{fin} represents fin width. The analytical expression for C_g is obtained from [119]. The expression for C_{ch} is acquired by overlapping a TG FinFET along the fin width direction and a single-gate FET along the fin height direction [64].

$$C_g = \frac{1}{Weff}\left[\begin{array}{l}\dfrac{3.02\times 3\varepsilon_{ox}/2}{\ln(1+3t_{ox}/2H_{fin})} - \dfrac{5\varepsilon_{ox}/4}{\ln(1+5t_{ox}/4H_{fin})} \\ + \dfrac{5\varepsilon_{ox}/4}{\ln(1+5t_{ox}/4W_{fin})}\end{array}\right], \tag{6}$$

Where W_{eff} is the effective width of FinFET device, t_{ox} and ε_{ox} represents the oxide thickness and permittivity of the oxide, respectively, and

$$C_{ch} = \frac{1}{Weff}\left[W_{fin}\frac{\varepsilon_{si}}{H_{fin}} + 2H_{fin}\frac{\varepsilon_{si}}{W_{fin}}\right], \tag{7}$$

where ε_{si} is the permittivity of silicon.

For Tz-TG FinFETs, the equivalent fin thickness at the orthocenter of the trapezoidal structure is found to be $W_{eff} = 2H_{fin} + W_{fin}$

The fin width, W_{fin} is derived from the equation [64]

$$W_{fin} = W_{fin,eq} = W_{fin,top} + \frac{\lambda}{\lambda + 1}(W_{fin,bot} - W_{fin,top}) \tag{8}$$

where $$\lambda = \frac{2W_{fin,bot} + W_{fin,top}}{2W_{fin,top} + W_{fin,bot}} \tag{9}$$

For Re-TG FinFETs $\lambda = 1$, and for Tz-TG FinFETs $1 < \lambda < 2$. When $W_{fin,top} = 0$, then $\lambda = 2$ and (8) and (9) lead to the equivalent fin thickness in triangular TG FinFETs, corresponding to the silicon thickness at the orthocenter of the triangle

$$W_{fin} = W_{fin,eq} = \frac{2W_{fin,bot}}{3} \tag{10}$$

Random threshold voltage variation (σV_{th}) plays a key role in determining the leakage distribution of FinFET devices. The analytical expression for σV_{Th} in FinFET devices due to random dopant fluctuations is found to be [62]

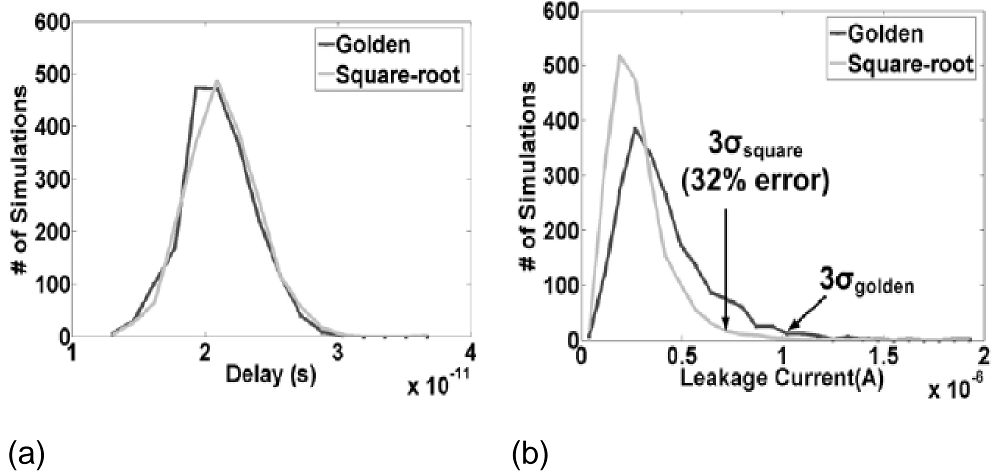
$$\sigma V_{Th} = q\left(\sqrt{\frac{W_{fin}}{2}}\right)\frac{t_{ox}}{\varepsilon_{ox}}\left(\frac{\sqrt{N_{si}}}{\sqrt{L_{eff} W_{eff}}}\right) \tag{11}$$

2.2.3. Conventional Statistical Leakage current Model and its Limitation

Equation 8 shows the conventional model for statistical V_{Th} estimation which will be referred to as the square-root method [68]. Here, the mean of V_{Th} is a constant and the standard deviation of V_{Th} is inversely proportional to the square-root of the gate area.

$$\mu(V_{Th}) = Cons\tan t$$
$$\sigma(V_{Th}) \propto \frac{1}{\sqrt{W.L}} \tag{12}$$

Although equation (9) has been widely used as a basis for delay estimation, it cannot properly model the device leakage under the impact of atomistic RDF. To motivate our work, we will first explain why the conventional square-root method fails to capture the actual (golden) case. Figure. 2.5(a) shows the simulation setup with progressively sized inverters for the delay and leakage experiments [77]. The golden results are obtained as described in Figure. 2.5 by assigning four independent random variables V_{Th} to each reference device to represent the atomistic RDF effect [77]. The conventional square-root method uses a single effective V_{Th} with the mean and sigma values calculated from equation (3.1). Leakage variation of the device can be expressed using this single effective V_{Th} as shown in Figure. 2.5. From Figure. 2.5(b), we can perceive that the delay distribution using (9) matches very closely with the golden results. The square-root method was originally developed to model the V_{Th} defined for the strong-inversion current which is a linear combination of the V_{Th}'s of sub-devices affected by the atomistic RDF [120]. The concept of sub-devices to account for the RDF inside a larger device is illustrated in Fig. 2.5 under the golden case. As a result, circuit parameters such as delay which are also approximately a linear function of V_{Th} can be correctly modeled using equation (9). This observation is consistent with the results shown in previous publications [121]. On the other hand, Figure. 2.5 shows a large discrepancy in leakage distributions between the two approaches. The conventional V_{Th} model in equation (8) fails to predict the golden leakage distribution, underestimating the 3σ leakage current by32%. This tells us that the effective V_{Th} following equation (9) does not work well for estimating the leakage distribution. This discrepancy comes from the fact that leakage current is an exponential function of V_{Th} and therefore the simple solution in equation (9) does not hold true for a sum of lognormal variables considering the atomistic RDF. In fact, equation (9) was originally derived based on the relationship between the active current and the V_{Th} of a device and thus is not accurate for modeling the leakage current [122]. The above simulation assumes no spatial correlation within a single device. As will be shown later, the conventional scheme shows a poor leakage estimation result when spatial correlation is included.



(a) (b)

Figure 2.5: Comparison between conventional square-root method and the actual (golden) case (a) Delay distribution; (b) Leakage distribution.[77]

Based on the above observations, this work will focus on developing an accurate leakage distribution model which captures the width-dependent characteristics of the leakage caused by atomistic RDF in a nanoscale CMOS device. One assumption used in this thesis is that a large device can be considered as a group of smaller devices by ignoring any fringing effect at the device boundary.

Golden	Square-root	Proposed
D G S; $W_y=nW_x$; W_x; V_{Txi}; V_{Txi+1} V_{Txi}: V_T of i-th sub-device	D G S; $W_y=nW_x$ V_{Ty}: effective V_T	D G S; $W_y=nW_x$ V_{Ty}: effective V_T
Given inputs for reference device: $W_x, \mu_{V_{Tx}}, \sigma_{V_{Tx}}$		W_x
$I_{leak} \propto \sum_{i=1}^{n} W_x e^{-qV_{Txi}/mkT}$ $\begin{cases}\mu(V_{Txi}) = \mu_{V_{Tx}} \\ \sigma(V_{Txi}) = \sigma_{V_{Tx}}\end{cases}$	$I_{leak} \propto W_y e^{-qV_{Ty}/mkT}$ $\begin{cases}\mu(V_{Ty}) = \mu_{V_{Tx}} \\ \sigma(V_{Ty}) = \sigma_{V_{Tx}} / \sqrt{\frac{W_y \cdot L_y}{W_x \cdot L_x}}\end{cases}$	$I_{leak} \propto W_y e^{-qV_{Ty}/mkT}$ $\begin{cases}\mu(V_{Ty}) = f_\mu(W_y, \mu_{V_{Tx}}, \sigma_{V_{Tx}}) \\ \sigma(V_{Ty}) = f_\sigma(W_y, \mu_{V_{Tx}}, \sigma_{V_{Tx}})\end{cases}$

Figure 2.6: Statistical leakage model comparison between the golden, square-root method, and proposed method.

2.2.4 Proposed Statistical Leakage Model

The goal of a statistical leakage estimation tool is to obtain an accurate leakage distribution of a device based on process inputs such as the V_{Th} mean and V_{Th} sigma of a reference device. Figure. 2.6 illustrates how the proposed approach is different from the conventional square-root method. Both the proposed and square-root methods introduce an effective V_{Th} to represent the device leakage variation using a single variable. However, unlike the square-root method, the mean and sigma of V_{Th} in the proposed method is expressed as a function of the device width W as well as the two other inputs (mean and sigma of reference device V_{Th}) to match the actual case. The following derivation will show how the actual leakage, which is a sum of lognormal distributions, can be precisely modeled using a single effective V_{Th} parameter with anew mean and sigma.

2.2.5 Impact of width quantization on FinFET Leakage estimation

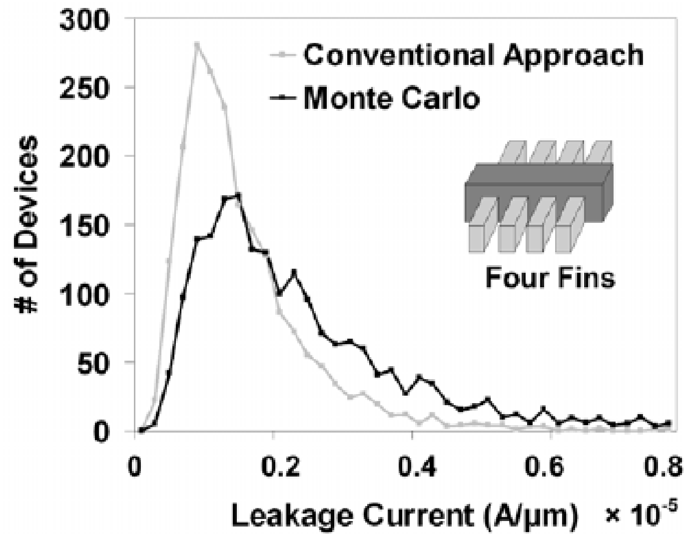
Width quantization is a unique property of FinFET devices; a large single device consists of multiple small unit fins. Width quantization is a byproduct of the fact that every fin must have an equal height (H) due to process restrictions [123]. Therefore, a FinFET device with a large width has to be discretized into multiple minimum unit fins. Fig. 2.1(b) shows a layout example of a FinFET inverter whose pull-up and pull-down are both quantized into smaller unit fins. The width of a single fin becomes the minimum step at which the transistor width can be incremented so the width of every transistor in a FinFET process is quantized. Circuit designers must take this into consideration while building FinFET circuits. In fact, a careful inspection indicates that the estimation results of the FinFET leakage distribution can be significantly affected by this phenomenon. Fig. 2.7(a) shows the difference between conventional leakage estimation method and the Monte Carlo simulation which serves as the golden result in this example[8].In our thesis we have considered trapezoidal shape FinFET with four fins Note the conventional approach here is the same as what was described in section 2.2.4 and equation (9). More specifically, given the mean μ and standard deviation σ of the single fin V_{Th}, conventional approaches

estimate the V_{Th} and leakage distribution of a multi-fin device assuming the same mean V_{Th} value and a σ which is inversely proportional to the square root of the device area (or the number of fins in FinFET) as:

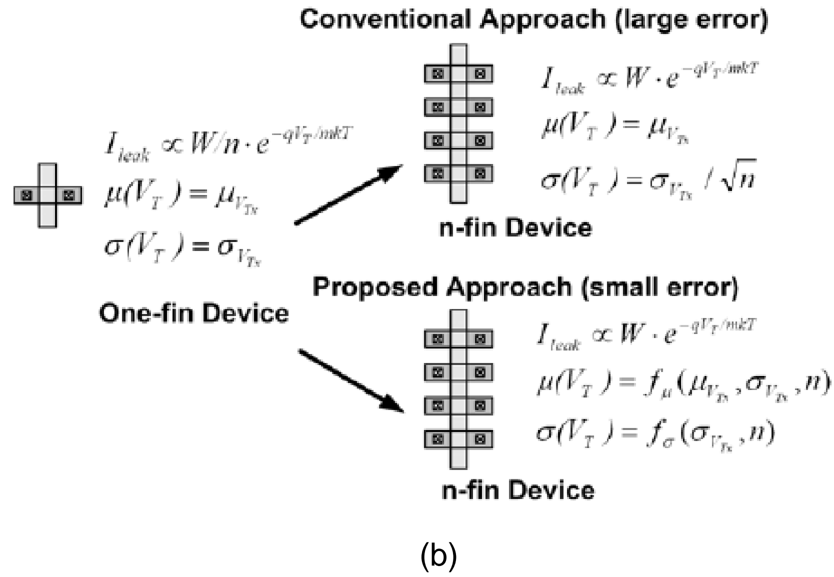
$$\sigma(V_{Th}) \propto \frac{1}{\sqrt{WL_{eff}}} = \frac{\sigma(V_{Tx})}{\sqrt{n}} \tag{13}$$

Here, $\sigma(V_{Tx})$ is the standard deviation of a single fin V_{Th}.

The conventional approach shows a large error in leakage estimation and more importantly it underestimates the leakage value leading to the potential failure of meeting design targets, such as power budget and noise margin requirements.[77]. The RDF introduces the threshold voltage variation among each individual fin. Due to the exponential relationship between leakage and V_{Th}, a leaky fin overweighs an unleaky fin in determining the overall device leakage current. As mentioned earlier, the conventional approach was derived based on a linear sum of the active current and V_{Th} and thus fails to capture the leakage characteristics of FinFET devices. Based on the above observation, this work utilizes a precise model for FinFET leakage estimation where both μ and σ of the "effective" V_{Th} are functions of the number of fins.



(a)



(b)

Figure 2.7:(a) Leakage distribution of a 4-fin device based on the conventional estimation approach and Monte Carlo simulation (golden) showing a large discrepancy. (b) Equations used in the conventional and proposed leakage estimation approaches for n-fin devices[8].

2.2.6 Statistical Leakage Estimation Under Width Quantization

In a width quantized FinFET device, the total leakage of an n-fin device is the sum of the leakage currents of each unit fin. Hence it can be expressed as the sum of lognormal terms as shown in {11},

$$I_{leak} = \sum_{i=1}^{n} C \frac{W}{n} e^{\frac{qV_{Th}}{mkT}} = \sum_{i=1}^{n} C \frac{W}{n} e^{-BV_{Th}} \qquad (14)$$

where W is the total width of the FinFET device, T is the temperature, m is the body effect coefficient, q is electron charge, k is Boltzmann's constant, and C is a technology parameter. q/mkT is referred as constant B for simplicity. The threshold voltage (V_{Th},) changes due to factors such as channel length variation and random dopant fluctuation (RDF). The threshold voltage of each fin can be modeled using correlated Gaussian random variables because: (1) RDF introduces uncorrelated V_{Th} variations because the device dopant concentration, which significantly influences the V_{Th} value, can be random even for devices within a small area. Xiong et.al, showed that as device dimensions scale below 25nm, the number of dopant atoms per device becomes less than

100, and thus V_{Th} can vary significantly due to the fluctuation in the number and placement of dopants [67]. Recently, Chiang shows that although undoped silicon is likely the material of choice for FinFET devices, even a single impurity atom randomly deposited in the channel region can lead to significant fluctuation in threshold voltage because of the ultra-thin body [124]. As a result, RDF will still remain as one of the major sources of variation in FinFETs. (2) Process parameters such as channel length and fin height show a strong spatial correlation. As shown in equation (11), the leakage of a large FinFET device can be expressed as a sum of lognormals. Although a closed form expression for a sum of lognormals does not exist, Wilkinson's method provides a simple approximation for modeling the sum of lognormals [125]. In Wilkinson's approach, a sum of lognormals $\sum_{i=1}^{n} \frac{W}{n} e^{x_i}$ can be approximated as another lognormal $\left(We^{y}\right)$ where y is a new Gaussian variable with a calculable mean and standard deviation. This approximation is completed by matching the first and second moment of both equations. Let $\left(m_{x_i}, \sigma_{x_i}\right)$ and $\left(m_{y_i}, \sigma_{y_i}\right)$ be the mean and standard deviation of the original Gaussian variables x_i and the new Gaussian variable y of the lognormal functions, respectively.

Let *rij* be the correlation coefficient of each random variable and n be the number of fins in a device. By equating the first two moments of the original lognormal equation and the new lognormal equation, we get:

$$u_1 = E(s) = \sum_{i=1}^{n} \frac{1}{n} e^{m_{x_i} + \sigma_{x_i}^2 / 2} = e^{m_y + \sigma_y^2 / 2}$$

$$u_2 = E\left(s^2\right) = \frac{1}{n^2}\left(\sum_{i=1}^{n} e^{2m_{x_i} + 2\sigma_{x_i}^2} + 2\sum_{i=1}^{n-1} \sum_{j=i+1}^{n} e^{m_{x_i} + m_{x_j}} e^{\left(\sigma_{x_i}^2 + \sigma_{x_{ji}}^2 + 2r_{ij}\sigma_{x_i}\sigma_{x_j}\right)/2} \right)$$

$$= e^{2m_y + 2\sigma_y^2} \tag{15}$$

In a FinFET device, it is fair to assume every fin has the same mean and variance of V_{Th}, and the same correlation between each other. Therefore, by solving equation (12), the mean and standard deviation of the new Gaussian variable in the lognormal equation is found as follows:

$$m_y = m_x + \frac{1}{2}\Delta$$

$$\sigma_y{}^2 = \sigma_x{}^2 - \Delta \tag{16}$$

$$\Delta = \sigma_x{}^2 - \ln\left(\frac{e^{\sigma_x{}^2} + (n-1)e^{r\sigma_x{}^2}}{n}\right) \tag{17}$$

where

Δ is a non-negative number. Finally, the average and standard deviation of the new equivalent V_{Th} can be derived from (14) by including the constant B defined in the subthreshold current equation (11).

$$\mu_{V_{Ty}} = \mu_{V_{Tx}} + \frac{1}{2}\Delta / B$$

$$\sigma_{V_{Ty}}{}^2 = \sigma_{V_{Tx}}{}^2 - \Delta / B^2, (\Delta \geq 0) \tag{18}$$

$$\Delta = B^2 \sigma_{V_{Tx}}{}^2 - \ln\left(\frac{e^{B^2\sigma_{V_{Tx}}{}^2} + (n-1)e^{rB^2\sigma_{V_{Tx}}{}^2}}{n}\right) \tag{19}$$

Here, V_{Ty} denotes the threshold voltage of an effective large single-fin device and V_{Tx} denotes the threshold voltage of the original single fin. This can be understood from the following relationship:

$$We^{-\frac{qV_{Ty}}{mkT}} = \sum_{i=1}^{n} \frac{W}{n} e^{-\frac{qV_{Tx_i}}{mkT}} \tag{20}$$

V_{Ty} is referred to as the “effective threshold voltage”. By introducing the effective threshold voltage concept, we can efficiently find the leakage distribution of a width quantized FinFET without having to run Monte Carlo simulations for n number of random variables. The expression for the effective V_{Th} in (15) reveals that the average of V_{Th} is reduced compared to that of a single fin. The amount of change in the average is determined by a single non-negative parameter Δ. The standard deviation σV_{Ty} also decreases with the larger number of fins due to the Δ parameter in equation (15).

2.2.7 Leakage Model for Discrete Width Multiplication (*$W_y = nW_x$*, n: integer)

Let V_{Ty} be the effective V_{Th} of a device with a width of W_y. $\mu_{V_{Tx}}$ and $\sigma_{V_{Tx}}$ are given parameters where V_{Tx} is the V_{Th} of a reference device with a width of W_x. The total device leakage can be expressed as:

$$\sum_{i=1}^{n} W_x e^{-BV_{Tx_i}} = W_y e^{-BV_{T_y}} \tag{21}$$

W_y is equal to nW_x and represents the V_{Th} of each reference sub-device considering the atomistic RDF. The mean and sigma of V_{Ty} in equation (18) can be expressed using the mean and sigma of V_{Tx} using Wilkinson's method which shows that a sum of lognormal variables can be approximated to another lognormal variable[126]. For simplicity, we define (μ_x, σ_x) as the mean and sigma of the reference device Gaussian variables ($-BV_{Tx_i}$) and (μ_y, σ_y) as those of the total device Gaussian variable ($-B \cdot V_{Ty}$) in equation (18). We also assume that a correlation coefficient r_x between two reference device Gaussian variables ($-BV_{Tx_i}$) is given to model the spatial correlation. Wilkinson's method allows us to equate the first moment and second moment of the two lognormal expressions in equation (18) as follows.

$$\begin{aligned}
u_1 &= E(s) = \sum_{i=1}^{n} e^{\mu_x + \sigma_x^2/2} = ne^{\mu_x + \sigma_x^{\ 2}/2} = e^{\mu_y + \sigma_y^2/2} \\
u_2 &= E(s^2) = \left(\sum_{i=1}^{n} e^{2\mu_x + 2\sigma_x^2} + 2\sum_{i=1}^{n-1} \sum_{j=i+1}^{n} e^{2\mu_x} e^{\left(2\sigma^2{}_x + 2r\sigma_x^2\right)/2} \right) \\
&= ne^{2\mu_x + \sigma^2{}_x} \left(e^{\sigma^2{}_x} + (n-1) e^{r_x \sigma^2{}_x} \right) \\
&= n^2 e^{2\mu_y + 2\sigma_y^2}
\end{aligned} \tag{22}$$

Solving equation (19), we find the following relationship:

$$\mu_y = \mu_x + \frac{1}{2}\Delta$$
$$\sigma_y{}^2 = \sigma_x{}^2 - \Delta \tag{23}$$

$$\Delta = \sigma_x{}^2 - \ln\left(\frac{e^{\sigma_x{}^2} + (n-1)e^{r_x\sigma_x{}^2}}{n}\right) \tag{24}$$

Where Δ is a non-negative number. By plugging in the constant B, we obtain the following relationship between the V_{Tx} and V_{Ty}:

$$\mu_{V_{Ty}} = \mu_{V_{Tx}} + \frac{1}{2}\Delta / B$$
$$\sigma_{V_{Ty}}{}^2 = \sigma_{V_{Tx}}{}^2 - \Delta / B^2, (\Delta \geq 0) \tag{25}$$

$$\Delta = B^2\sigma_{V_{Tx}}{}^2 - \ln\left(\frac{e^{B^2\sigma_{V_{Tx}}{}^2} + (n-1)e^{r_x B^2\sigma_{V_{Tx}}{}^2}}{n}\right) \tag{26}$$

Equation (23) shows that the mean value of the effective V_{Th} is reduced by $\frac{1}{2}\Delta / B$, which is consistent with our observation in Figure. 2.5(b) showing that the golden case has a higher average leakage compared to results from the conventional square-root method. The sigma value goes down according to equation(23) following a similar trend as the square-root method but giving a closer match with the golden case.

The correlation coefficient r_y between V_{Ty} of two devices al to the r_x value of the reference device because the device dimensions have changed. An expression for r_y is needed to extend the model for the continuous width multiplication case. Leakage currents of two new devices with equal sizes can be described as:

$$\sum_{i=1}^{n} W_x e^{-BV_{Tx1_i}} = W_y e^{-BV_{T_{y1}}}$$
$$\sum_{i=1}^{n} W_x e^{-BV_{Tx2_i}} = W_y e^{-BV_{T_{y2}}} \tag{27}$$

2.2.8 Leakage Model for Continuous Width Multiplication ($W_y=\alpha W_x$, α:positive rational number)

Wilkinson's method cannot be directly applied to solve for the continuous width case: i.e. given μV_{Tx} and σV_{Tx} of V_{Tx} for a device with width W_x, find the μV_{Ty} and σV_{Ty} of V_{Ty} for a device with width W_y, for a device with width W_y where $W_y=\alpha W_x$ and α is a positive rational number.

To solve this problem, we assume there exists a virtual reference device with width W_0 that satisfies both $W_x=mW_0$ and $W_y=nW_0$. α becomes n/m. and r_0 denote the mean, standard deviation, and correlation coefficient of V_{Th} forthe small virtual device. Now we can utilize the results from section 2.2.7 to carry outour derivation. From equation (23), we have:

$$\mu_{V_{Tx}} = \mu_{V_{T0}} + \frac{1}{2}\Delta_x / B$$
$$\sigma_{V_{Tx}}{}^2 = \sigma_{V_{T0}}{}^2 - \Delta_x / B^2, (\Delta \geq 0) \tag{28}$$

$$\Delta_x = B^2 \sigma_{V_{T0}}{}^2 - \ln\left(\frac{e^{B^2\sigma_{V_{T0}}{}^2} + (m-1)e^{r_0 B^2 \sigma^2{}_{V_{T0}}}}{m} \right) \tag{29}$$

And also

$$\mu_{V_{Ty}} = \mu_{V_{T0}} + \frac{1}{2}\Delta_y / B$$
$$\sigma_{V_{Ty}}{}^2 = \sigma_{V_{T0}}{}^2 - \Delta_y / B^2, (\Delta \geq 0) \tag{30}$$

$$\Delta_y = B^2 \sigma_{V_{T0}}{}^2 - \ln\left(\frac{e^{B^2\sigma_{V_{T0}}{}^2} + (n-1)e^{r_0 B^2 \sigma_{V_{T0}}{}^2}}{n} \right)$$

(31)

Solving equations (26) and (27) we finally find the relationship,

$$\mu_{V_{Ty}} = \mu_{V_{Tx}} + \frac{1}{2}\Delta / B$$
$$\sigma_{V_{Ty}}{}^2 = \sigma_{V_{Tx}}{}^2 - \Delta / B^2, (\Delta \geq 0) \tag{32}$$

$$\Delta = B^2 \sigma_{V_{Tx}}{}^2 - \ln\left(\frac{e^{B^2 \sigma_{V_{Tx}}{}^2} + (\alpha - 1) e^{r_x B^2 \sigma_{V_{Tx}}{}^2}}{\alpha} \right) \quad (33)$$

Equations (30) have the exact same format as equations (23) .This tells us that the same formulas can be applied to both discrete and continuous width cases. Although we started our derivation using a small reference device with a width of W_x, equations (29) and (30) can be used to relate the V_{Th} characteristics between any two devices with arbitrary widths, i.e. α can be either larger than 1 or smaller 1. In other words, the derived model can accurately estimate the leakage distribution of an arbitrary width device based on given process inputs for a reference device with any width value. Note that the above derivation is not specific to a certain type of variation. Therefore, the proposed model is general to any process variation sources although RDF is considered as the major cause of variation in this work.

2.3 Simulation Tool

Simulation is the imitation of the operation of a real-world process or system over time. The act of simulating something first requires that a model be developed. this model represents the key characteristics or behaviors/ functions of the selected physical or abstract system or process. The model represents the system itself, whereas the simulation represents the operation of the system over time. MATLAB (matrix laboratory) is one of the most commonly used simulation tools). It is a multi-paradigm numerical computing environment and fourth-generation programming language. Developed by *MathWorks*. MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation of user interfaces, and interfacing with programs written in other languages, including C, C++, Java, Fortran and Python. A MATLAB verson of R2012a is used for the process of simulation in our thesis.

2.3.1 Monte Carlo Simulation

Monte Carlo methods (or Monte Carlo experiments) are a broad class of computational algorithms that rely on repeated random sampling to obtain numerical results; typically one runs simulations many times over in order to obtain the distribution of an unknown probabilistic entity. They are often used in physical and mathematical problems and are most useful when it is difficult or impossible to obtain a closed-form expression, or unfeasible to apply a deterministic algorithm. Monte Carlo methods are mainly used in three distinct problem classes: optimization, numerical integration and generation of draws from a probability distribution.

Monte Carlo methods vary, but tend to follow a particular pattern:

1. Define a domain of possible inputs.
2. Generate inputs randomly from a probability distribution over the domain.
3. Perform a deterministic computation on the inputs.
4. Aggregate the results.

In general terms, the Monte Carlo method (or Monte Carlo simulation) can be used to describe any technique that approximates solutions to quantitative problems through statistical sampling. As used here, 'Monte Carlo simulation' is more specifically used to describe a method for propagating (translating) uncertainties in model inputs into uncertainties in model outputs {results). Hence, it is a type of simulation that explicitly and quantitatively represents uncertainties. Monte Carlo simulation relies on the process of explicitly representing uncertainties by specifying inputs as probability distributions. If the inputs describing a system are uncertain, the prediction of future performance is necessarily uncertain. That is, the result of any analysis based on inputs represented by probability distributions is itself a probability distribution.

Whereas the result of a single simulation of an uncertain system is a qualified statement, the result of a probabilistic (Monte Carlo) simulation is a quantified probability. Such a result is typically much more useful to decision-makers who utilize the simulation results.

In order to compute the probability distribution of predicted performance, it is necessary to propagate (translate) the input uncertainties into uncertainties in the results. A variety of methods exist for propagating uncertainty. Monte Carlo simulation is perhaps the most common technique for propagating the uncertainty in the various aspects of a system to the predicted performance.

By using probability distributions, variables can have different probabilities of different outcomes occurring. Probability distributions are a much more realistic way of describing uncertainty in variables of a risk analysis. Common probability distributions include:

Normal – Or "bell curve." The user simply defines the mean or expected value and a standard deviation to describe the variation about the mean. Values in the middle near the mean are most likely to occur. It is symmetric and describes many natural phenomena such as people's heights. Examples of variables described by normal distributions include inflation rates and energy prices.

Lognormal – Values are positively skewed, not symmetric like a normal distribution. It is used to represent values that don't go below zero but have unlimited positive potential. Examples of variables described by lognormal distributions include real estate property values, stock prices, and oil reserves.

Uniform – All values have an equal chance of occurring, and the user simply defines the minimum and maximum. Examples of variables that could be uniformly distributed include manufacturing costs or future sales revenues for a new product.

Triangular – The user defines the minimum, most likely, and maximum values. Values around the most likely are more likely to occur. Variables that could be described by a triangular distribution include past sales history per unit of time and inventory levels.

PERT- The user defines the minimum, most likely, and maximum values, just like the triangular distribution. Values around the most likely are more likely to occur. However values between the most likely and extremes are more likely to occur than the triangular; that is, the extremes are not as emphasized. An example of the use of a PERT distribution is to describe the duration of a task in a project management model.

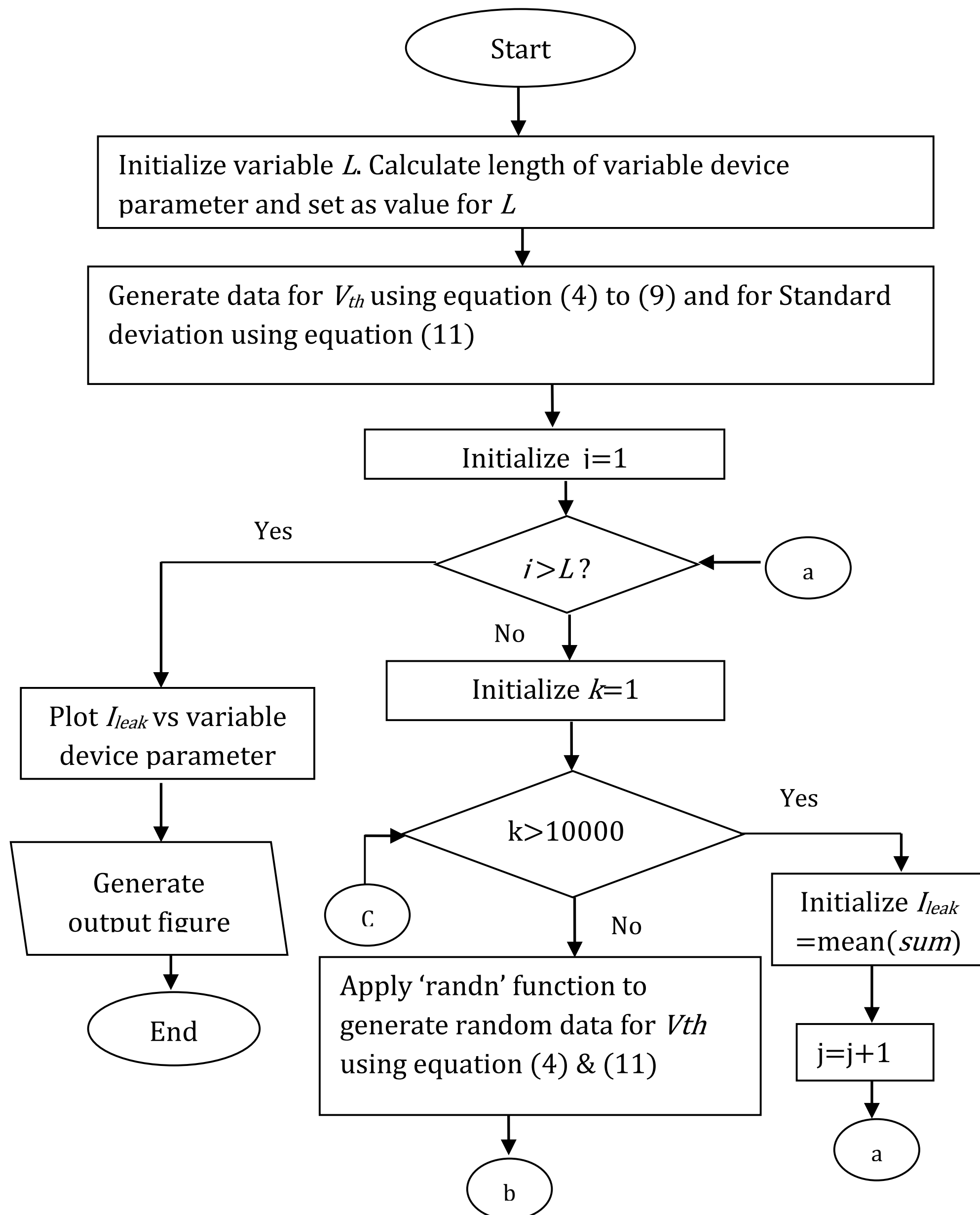
Discrete – The user defines specific values that may occur and the likelihood of each. An example might be the results of a lawsuit: 20% chance of positive

verdict, 30% change of negative verdict, 40% chance of settlement, and 10% chance of mistrial.

In our proposed Monte Carlo Simulation a normal probability distribution is considered. Initially the mean or expected value and a standard deviation is described to determine the the variation about the mean. The threshold voltage of the FinFET is considered as input .During a Monte Carlo simulation, values are sampled at random from the input probability distributions. Each set of samples is called an iteration, and the resulting outcome from that sample is recorded. As there are four number of fins we obtain four random threshold voltage output. This four random threshold voltage results in four leakage current. In Monte Carlo simulation, the entire device is simulated a large number (e.g., 10000) of times and finally results are summed up to obtain the total leakage current of the system. This results in a large number of separate and independent results, each representing a possible future for the system. The results of the independent system realizations are assembled into probability distributions of possible outcomes. As a result, the outputs are not single values, but probability distributions.
This chapter developed a statistical leakage model for RDF induced threshold voltage variation. The atomistic RDF where the dopant’s location also affects the overall V_{Th} is considered in the developed model. Compared with the conventional approach, the proposed model can estimate the width-dependent leakage distribution under atomistic RDF more accurately. Utilizing the model, the leakage distribution for width-quantized FinFET device is also modeled correctly.

2.3.2 Coding Process

Our simulation process of computing leakage current variation with process parameter contains certain steps. A detailed algorithm of entire coding process of the mentioned purpose is mentioned here in a compact or general form for all process parameters.



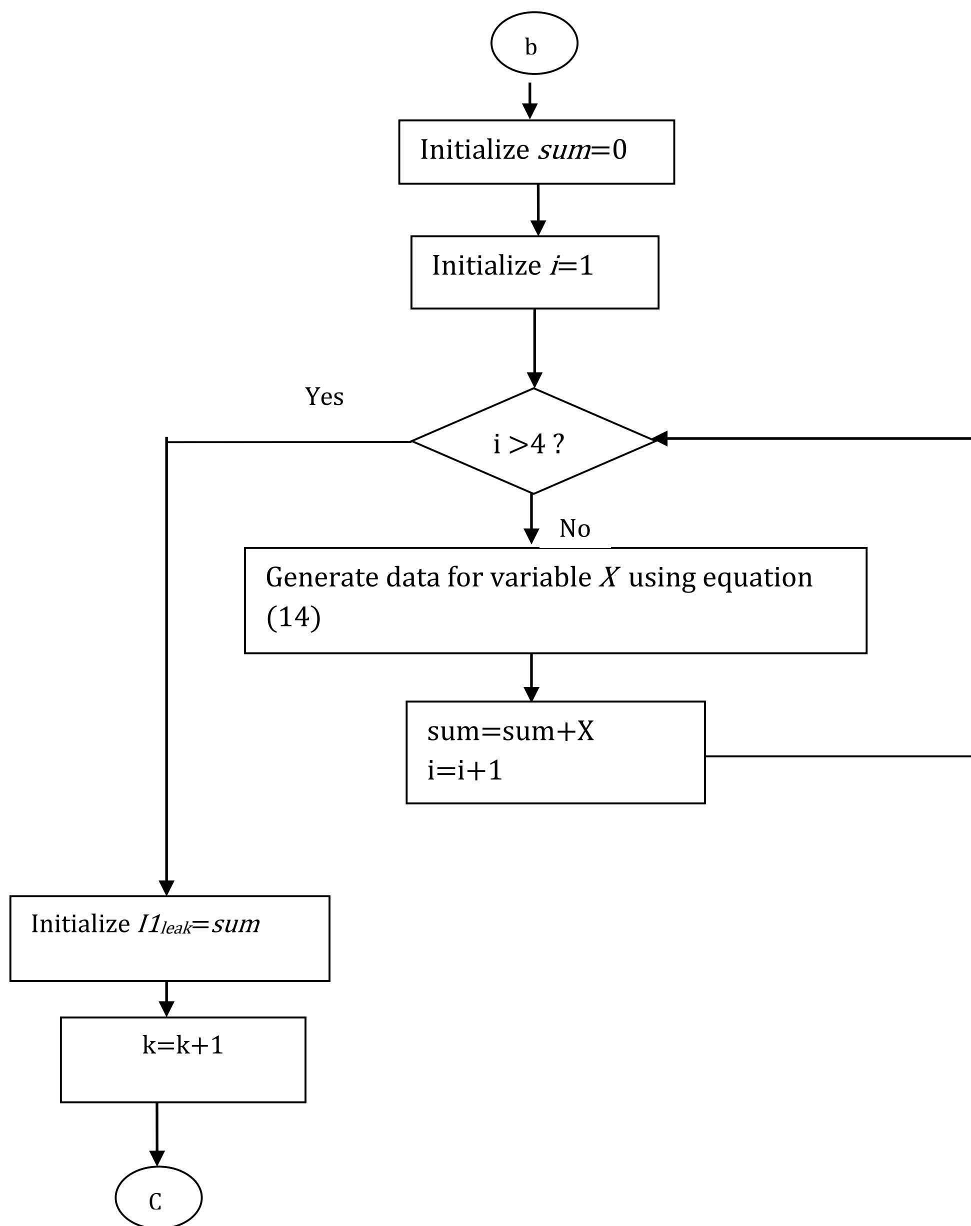


Figure 2.8: Algorithm of Coding Process

CHAPTER THREE

RESULT AND DISCUSSIONS

Numerical simulation is an extremely efficient tool for detailed investigation of physical phenomena, which determine electrical characteristics of semiconductor devices. Simulation results we present in this study had been obtained using MATLAB Software. A computer program has been developed in order to simulate the expressions for the described model found in the previous chapter using MATLAB. Numerical data generated by the program are plotted in this chapter to study the variation of threshold voltage and leakage of TG FinFET on various device parameters. Leakage current is strongly influenced by variations in the device threshold voltage V_{Th} because transistor leakage current increases exponentially as V_{Th} decreases. Process variations affect the device characteristics since these variations results in V_{Th}variation leading to a leakage current distribution instead of a constant leakage current. Process or physical parameter variations in TG FinFET can be induced by factors including RDF, body thickness variation, T_{ox} variation and gate height variation. The leakage current distribution due to different physical parameters variation incorporating random process parameter variation with Monte Carlo Simulation is presented in this chapter. Relative threshold voltage and leakage current characteristics are analyzed changing the fin numbers. Finally a comparative study between TZ shaped and Rect shaped TG FinFET by leakage current distribution is presented.

3.1 Threshold Voltage and Leakage Current Analysis of Tz FinFET

In this part we take a reference value of different device parameter. We consider the Tz shaped TG FinFET having four fins for our analysis. The corresponding reference data of device parameters are listed in table 3.1.

Table 3.1: Reference values of Device parameters used in simulation

Name of the Device parameters	**Reference value**
Bottom Fin Width, W_{bot} (nm)	15
Top Fin Width, W_{top}(nm)	13
Fin Height, H_{fin} (nm)	30
Thickness of Oxide layer, T_{ox} (nm)	1
Doping concentration, N_{si} (m-3)	5×10^{24}
Relative permittivity of Oxide layer,ϵ_{ox} (Nm^2C^{-2})	3.5
Relative permittivity of Insulator,ϵ_{si} (Nm^2C^{-2})	11.6
Thermal Voltage, V_T (V)	.026
Effective length, L_{eff} (nm)	25
Intrinsic carrier concentration, n_i (m-3)	1.5×10^{16}
Flatband Voltage, V_{fb} (V)	0
Sub-threshold voltage swing, m (mV/decade)	83

3.1.1 Variation of Threshold Voltage with Fin Height

By writing appropriate programming code for equation (4) changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of V_{Th} with H_{fin} is found which is shown in figure 3.1.1.

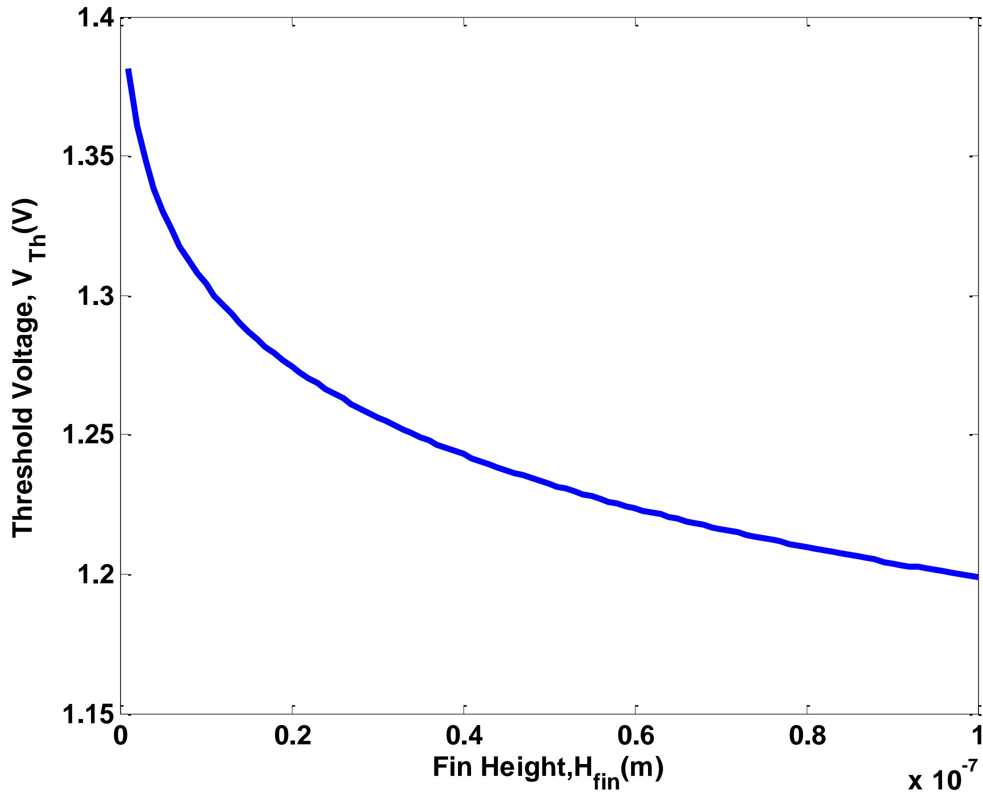


Figure 3.1.1: Variation of Threshold Voltage V_{Th} with changing Fin height H_{fin} keeping W_{bot}= 15 nm, W_{top}= 13 nm, T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

The relation between V_{Th} and H_{fin} is observed in Figure 3.1.1. From equations (5) to (7), it is clearly found that threshold voltage V_{Th} exponentially decreases with the increase in fin height H_{fin}.

3.1.2 Leakage Current variation with changing Fin Height

Writing appropriate programming code for equation (14) changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with H_{fin} is found by monte carlo simulation which is shown in figure 3.1.2.

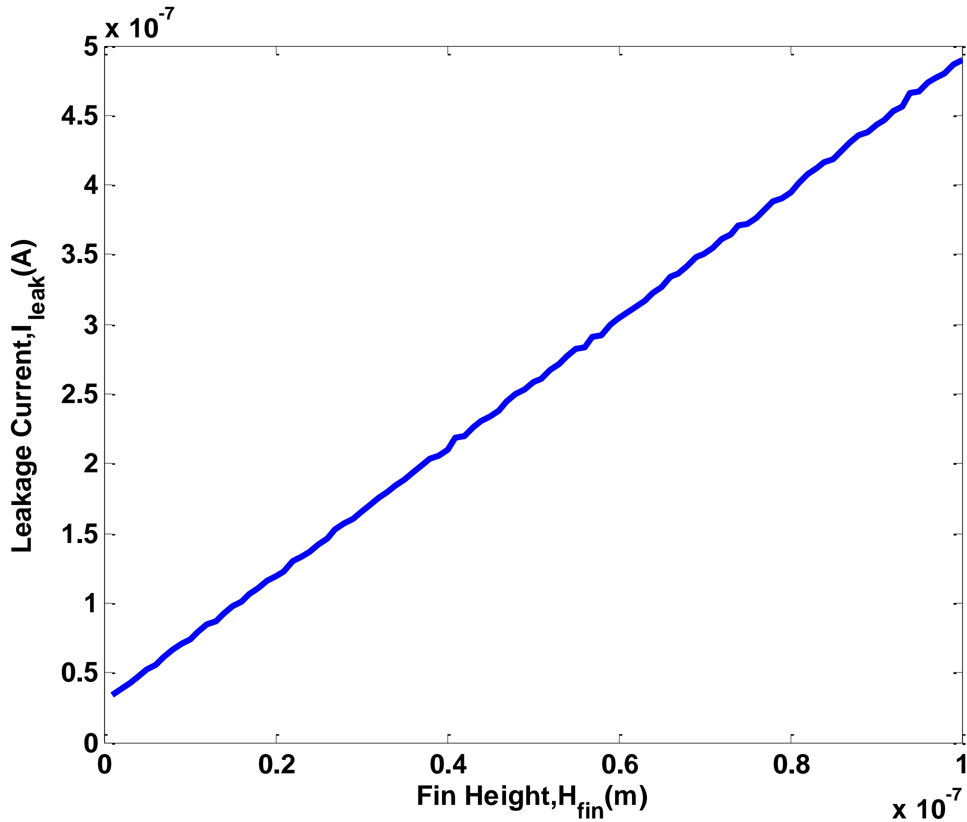


Figure 3.1.2: Lekage Current Variation I_{leak} with changing Fin height H_{fin} keeping $W_{fin,bot}$= 15 nm, W_{top}= 13 nm, t_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

Accordingly From Figure 3.1.2, we observe that the variation of H_{fin} leads to increase in leakage current. The exponential nature of threshold voltage variation with changing H_{fin} found in figure 3.1.1 is linear in figure 3.1.2 due the term $exp(-V_{Th})$ in equation (14).

3.1.3 Variation of Threshold Voltage with Fin Width

By writing appropriate programming code for equation (4) changing only Fin width from 1 m to 1×10^{-8} m and keeping other parameter constant same as mentioned in table 3.1, the variation of V_{Th} with W_{fin} is found which is shown in figure 3.1.3.

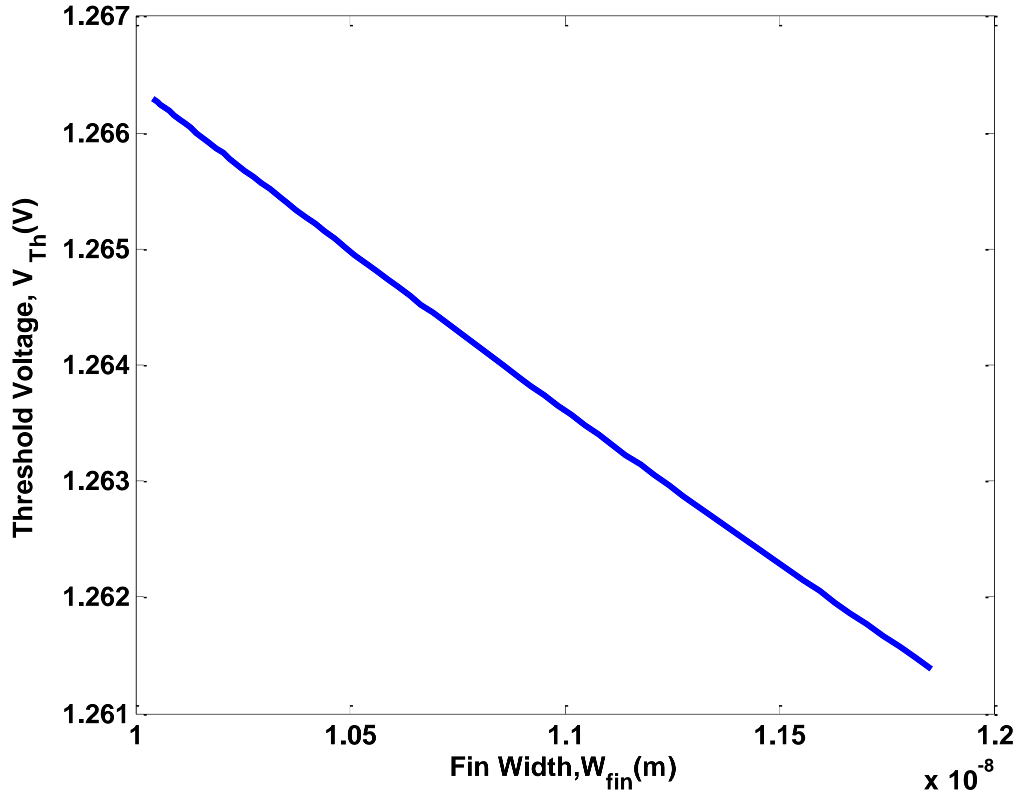


Figure 3.1.3: Variation of Threshold Voltage V_{Th} with changing Fin width W_{fin} keeping H_{fin}=30 nm, T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

It is found from figure 3.1.3 that the threshold voltage V_{Th} decreases linear with the increase in fin width W_{fin}. As seen from equation (6) and (7) , the gate capacitance and channel capacitance is inversely proportional to W_{eff} and linear, leakage current variation curve taking the peak point of random variation is exponential in nature.

3.1.4 Leakage Current variation with changing Fin Width

Writing appropriate programming code for equation (14) changing only Fin width from 1 to 1×10^{-8} m and keeping other parameter constant the variation of leakage current with W_{fin} is found by monte carlo simulation which is shown in figure 3.1.4.

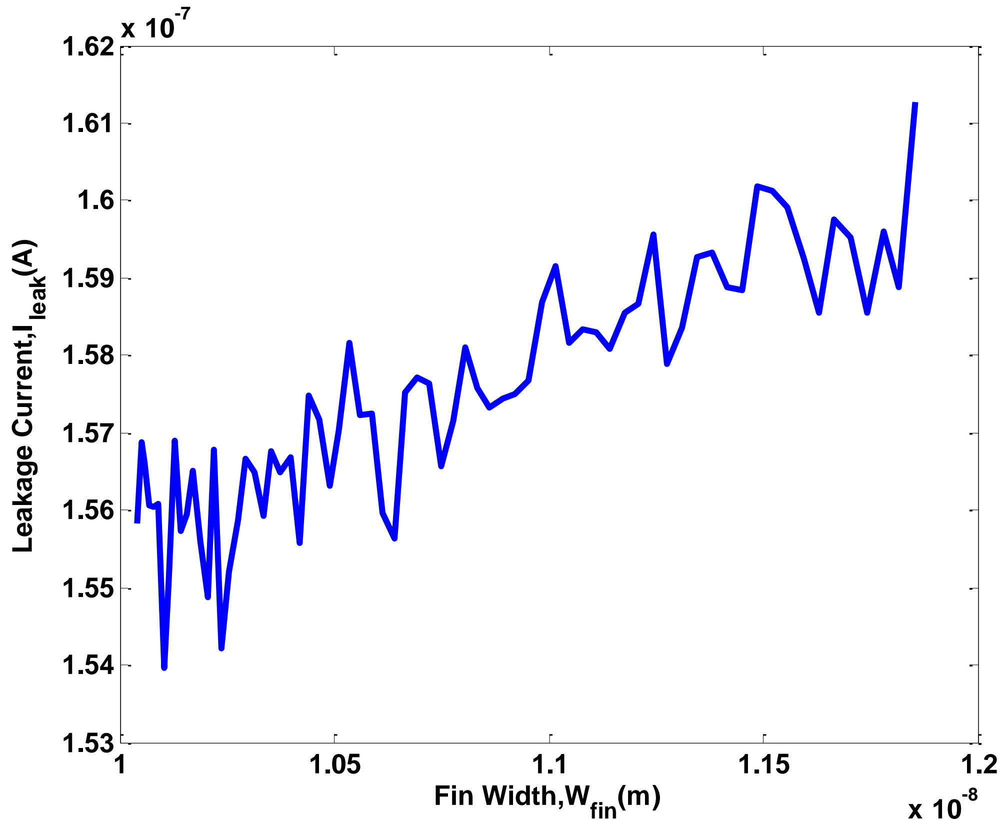


Figure 3.1.4: Leakage current variation of Threshold Voltage I_{leak} with changing Fin width W_{fin} keeping H_{fin}=30 nm, T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

From Figure 3.1.4, we notice that the variation of V_{Th} directs to leakage current variation increasing in random manner. The randomness is the effect of RDF as mentioned earlier. As threshold voltage variation with respect to fin width is linear.

3.1.5 Variation of Threshold Voltage with Oxide Thickness

By writing appropriate programming code for equation (4) changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table ,the variation of V_{Th} with T_{ox} is found which is shown in figure 3.1.5.

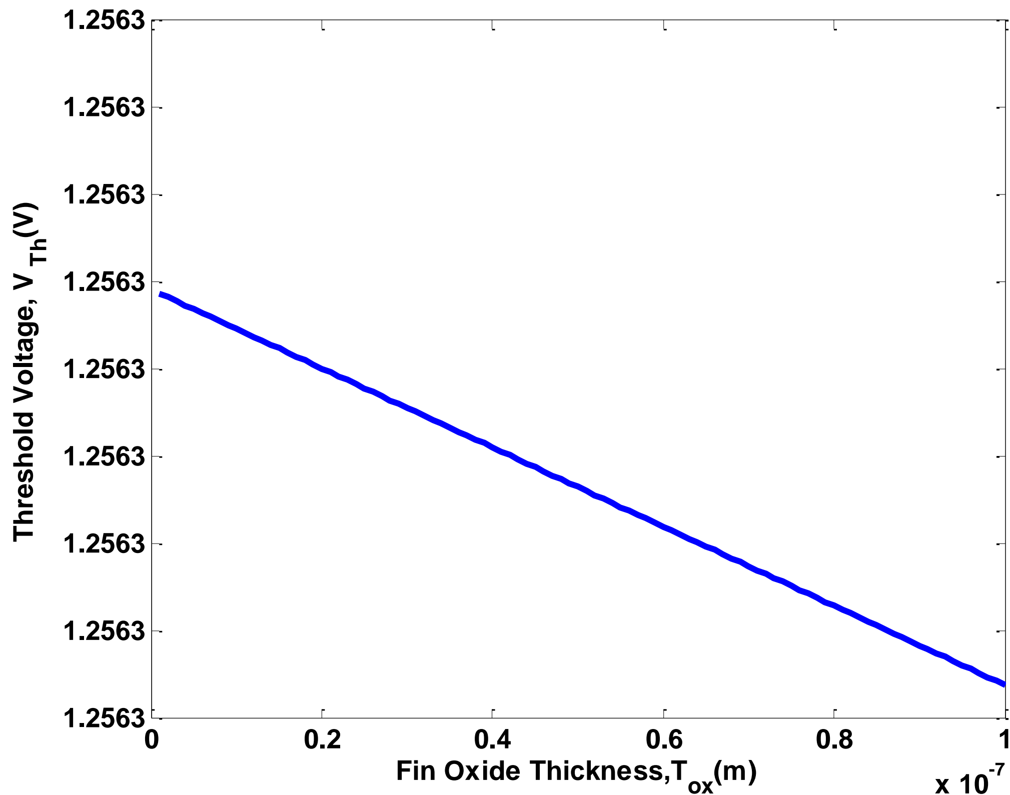


Figure 3.1.5: Variation of Threshold Voltage V_{Th} with changing Fin Oxide Thickness T_{ox} keeping W_{bot}= 15nm, W_{top}= 13 nm, H_{fin}= 30nm and N_{si}= 5×10^{18} cm^{-3}

Figure 3.1.5 illustrates that V_{Th} decreases with increasing oxide thickness as expected. The increase in oxide thickness increases gate capacitance according to equation (6) which again decreases threshold voltage linearly.

3.1.6 Leakage Current Distribution with changing Fin Oxide Thickness

Writing appropriate programming code for equation (14) changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with T_{ox} is found by monte carlo simulation which is shown in figure 3.1.6.

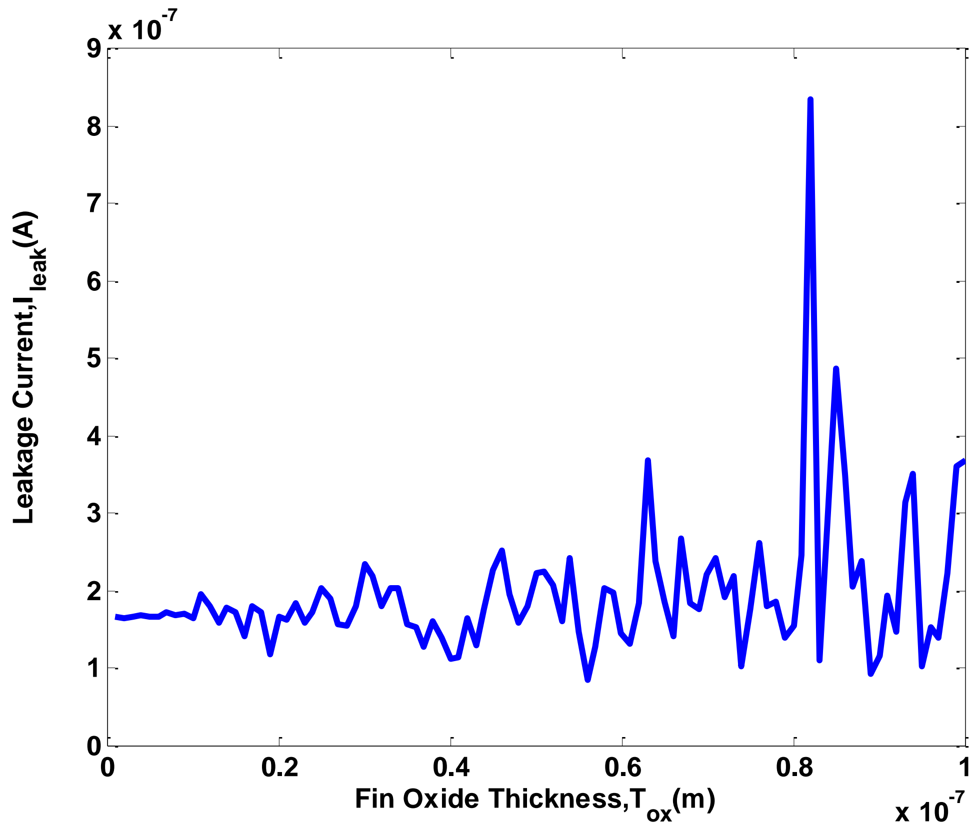


Figure 3.1.6: Leakage Current variation I_{leak} with changing Fin Oxide Thickness T_{ox} keeping W_{bot}= 15 nm, W_{top}= 13 nm, H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

From Figure 3.1.6, it is noticed that the variation of V_{Th} directs to leakage current variation increasing in random manner due to the effect of RDF. As threshold voltage variation with respect to oxide thickness is linear, leakage current variation curve taking the peak point of random variation is exponential in nature.

3.1.7 Variation of Threshold Voltage with Doping Concentration

By writing appropriate programming code for equation (4) changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} and keeping other parameter constant same as mentioned in table 3.1, the variation of V_{Th} with N_{si} is found which is shown in figure 3.1.7.

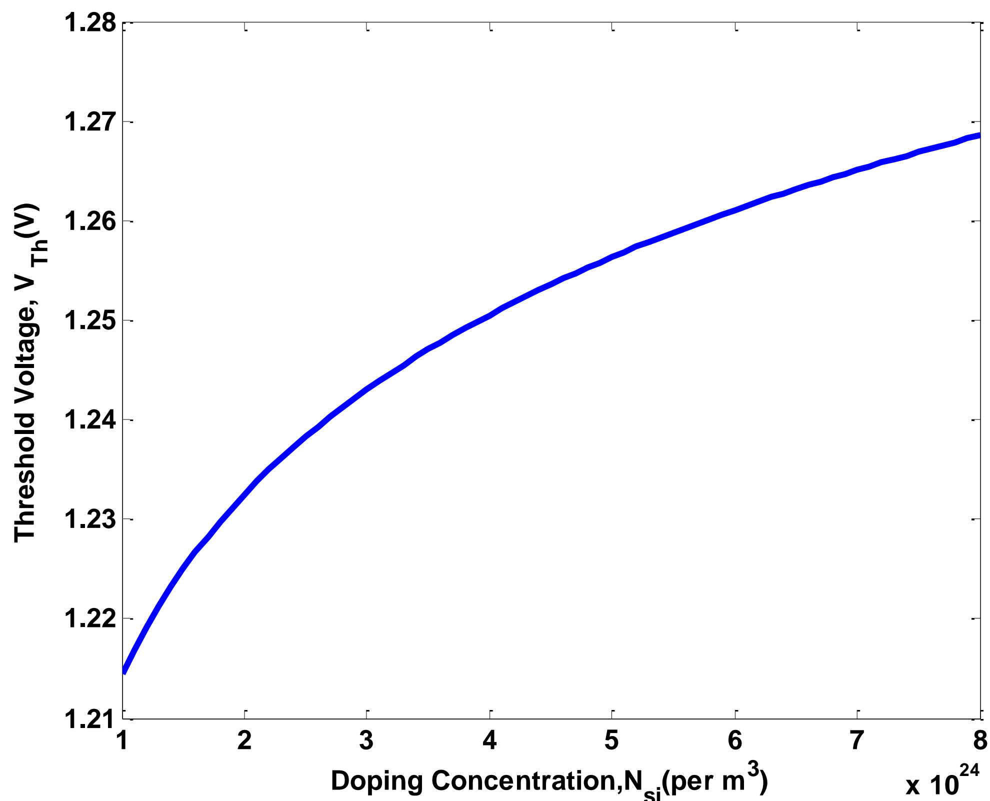


Figure 3.1.7: Variation of Threshold Voltage V_{Th} with changing Doping Concentration N_{si} keeping W_{bot}= 15 nm, W_{top}= 13 nm, T_{ox}= 1 nm and H_{fin} = 30 nm

Figure 3.1.7 demonstrates that V_{Th} is increasing with the increase in channel doping concentration N_{Si} in accordance with equation (4) to equation (5). The resulting curve is logarithmic.

3.1.8 Leakage Current variation with Doping Concentration

Writing appropriate programming code for equation (14) changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with N_{si} is found by monte carlo simulation which is shown in figure 3.1.8.

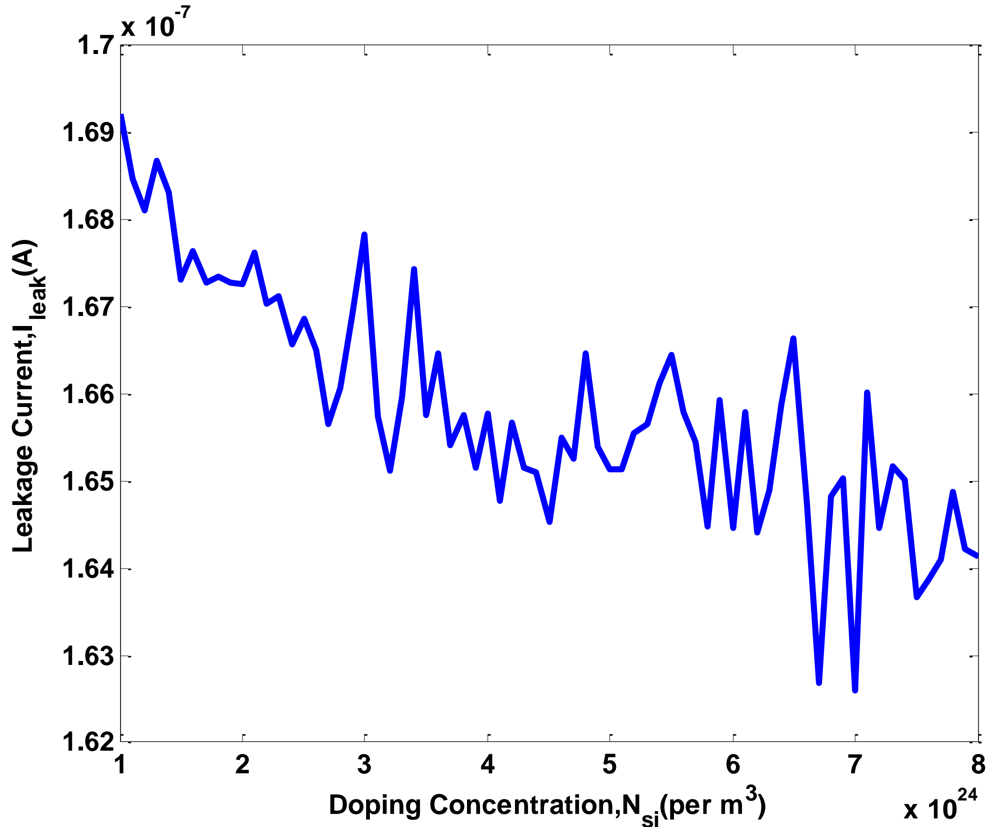


Figure 3.1.8: Leakage Current variation I_{leak} with changing Doping Concentration N_{si} keeping W_{bot}= 15 nm, W_{top}= 13 nm, t_{ox}= 1 nm and H_{fin} = 30 nm

RDF introducing statistically random variation in the number of dopant atoms causes over 70% of random V_{Th} variations [127].The increase in channel doping concentration decreases standard deviation of threshold voltage, σV_{Th} that results in lowering the current as shown in figure 3.1.8.

3.1.9 Leakage Current variation with Fin Height relative to Fin number

In this section simulation is done for three different Fin number as four Fin, six Fin and eight Fin model. Writing appropriate programming code for equation (14) changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with H_{fin} is found by monte carlo simulation which is shown in figure 3.1.9.

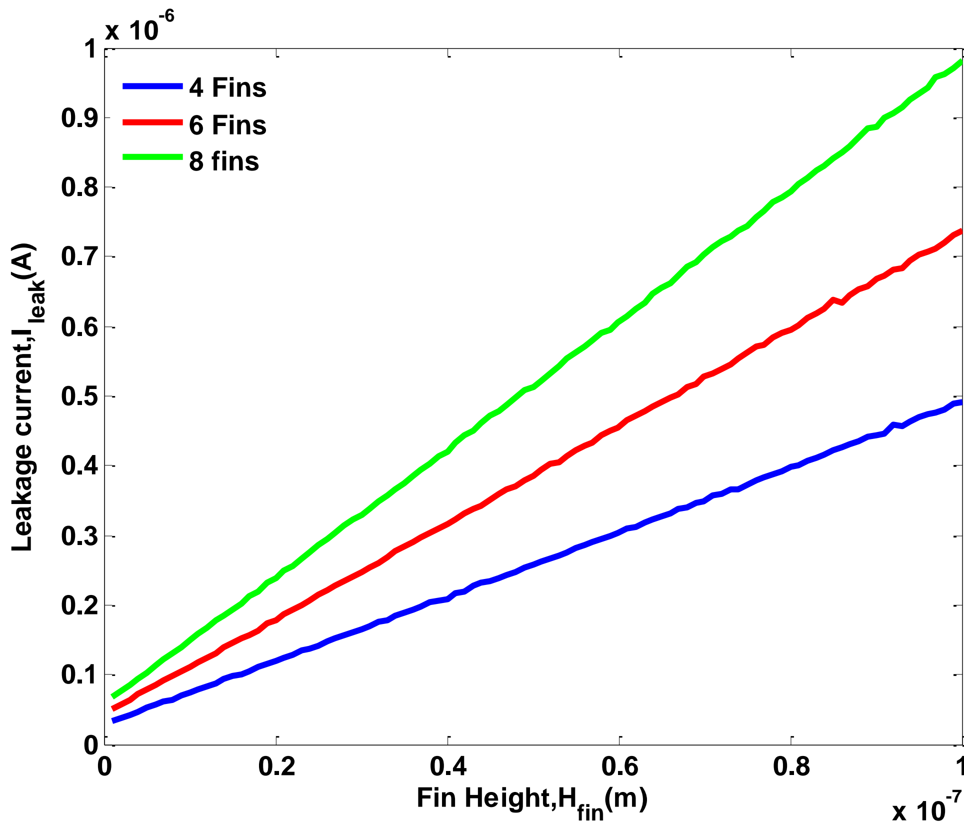


Figure 3.1.9: Lekage current variation I_{leak} with changing Fin height H_{fin} keeping W_{bot}= 15 nm, W_{top}= 13 nm, T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3} for different Fin number

Increasing the number of fins give rise to leakage current. Leakage current variation rate is minimum for four fin device model of TZ shaped TG FinFET which is noticed from figure 3.1.9.

3.1.10 Leakage Current variation with Fin Width relative to Fin number

In this section simulation is done for three different Fin number as four Fin, six Fin and eight Fin model. Writing appropriate programming code for equation (14) changing only Fin width from 1 to 1×10^{-8} m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with W_{fin} is found by monte carlo simulation which is shown in figure 3.1.10.

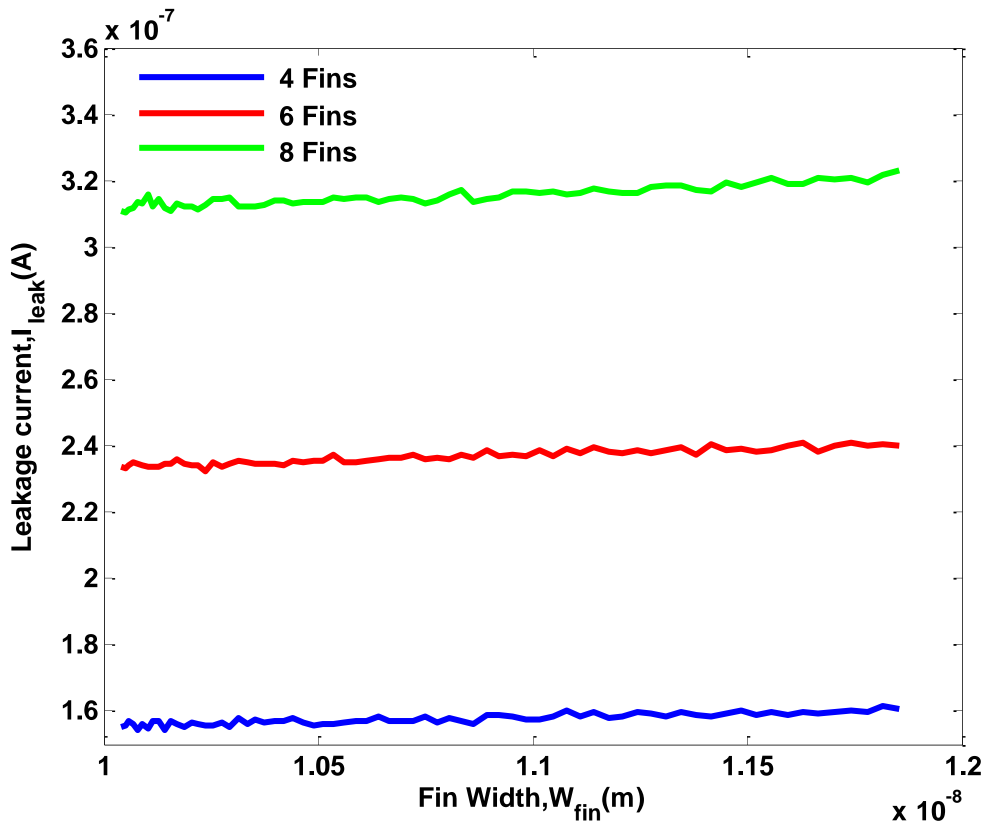


Figure 3.1.10: Leakage current variation of Threshold Voltage I_{leak} with changing Fin width W_{fin} keeping H_{fin}=30 nm, T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3} for different Fin number

It is noticed from figure 3.1.10 that increasing the number of fins give rise to leakage current. Leakage current variation rate is minimum for four fin device model of Tz shaped TG FinFET.

3.1.11 Leakage Current variation with Fin Oxide Thickness relative to Fin number

In this section simulation is done for three different Fin number as four Fin, six Fin and eight Fin model. Writing appropriate programming code for equation (14) changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with T_{ox} is found by monte carlo simulation which is shown in figure 3.1.11.

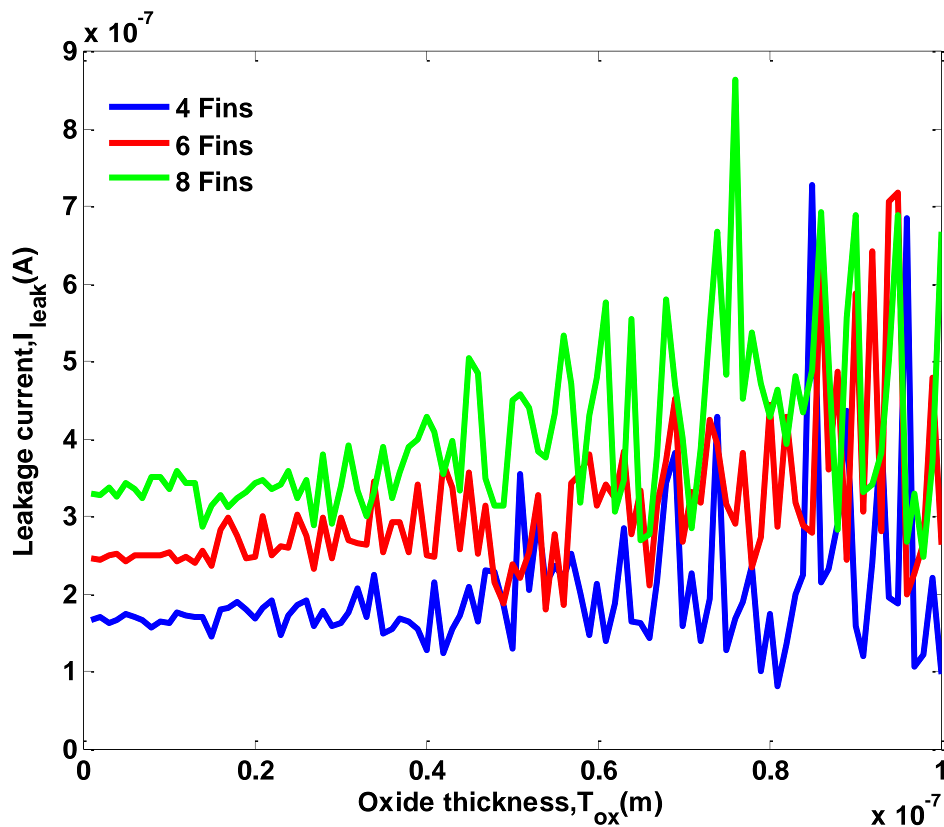


Figure 3.1.11: Leakage Current variation I_{leak} with changing Fin Oxide Thickness T_{ox} keeping W_{bot}= 15 nm, W_{top}= 13 nm, H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3} for different Fin number

From figure 3.1.11 we observe that increasing the number of fins give rise to leakage current. Leakage current variation rate is minimum for four fin device model of TZ shaped TG FinFET.

3.1.12 Leakage Current variation with Doping Concentration relative to Fin number

In this section simulation is done for three different Fin number as four Fin, six Fin and eight Fin model. By appropriate programming code for equation (14) changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} and keeping other parameter constant the variation of leakage current with N_{si} is found by monte carlo simulation which is shown in figure 3.1.12.

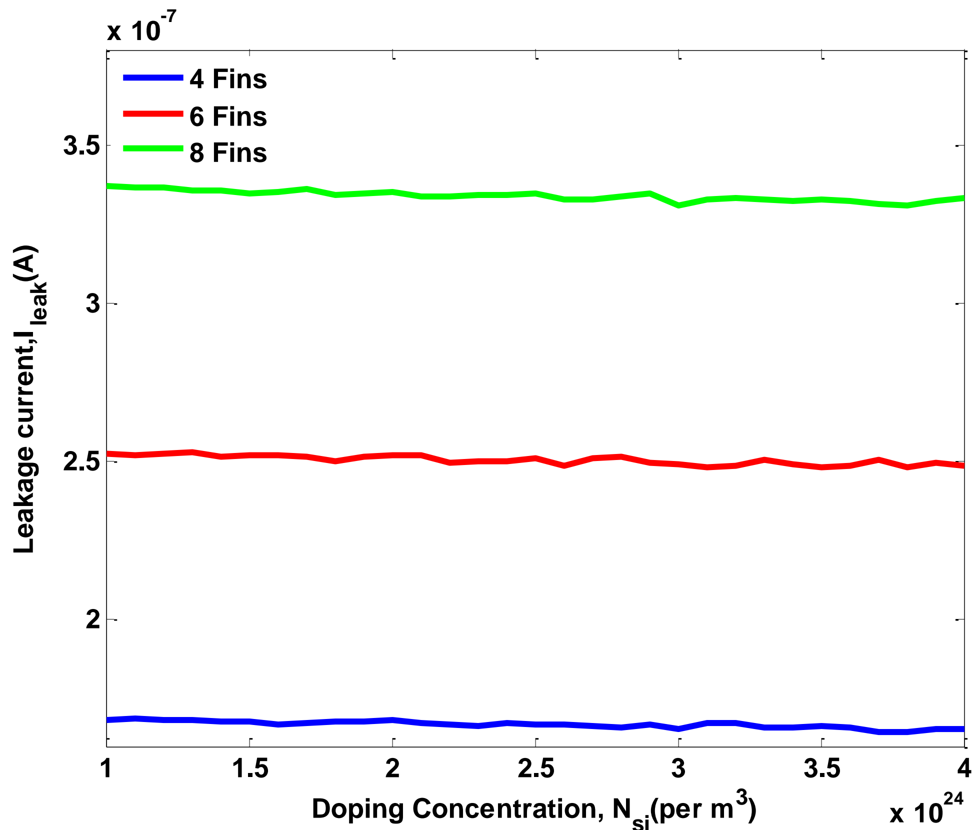


Figure 3.1.12: Leakage Current variation I_{tleak} with changing Doping Concentration N_{si} keeping W_{bot}= 15 nm, W_{top}= 13 nm, t_{ox}= 1 nm and H_{fin} = 30 nm for different Fin number

Figure 3.1.12 shows that increasing the number of fins give rise to leakage current. Leakage current variation rate is minimum for four fin device model of Tz shaped TG FinFET.

3.1.13 Leakage Current Distribution for Tz FinFET

Incorporating the standard threshold voltage deviation from equation (3) in leakage current equation (14), distribution of leakage current variation is simulated which is shown in figure 3.1.13. Values of device parameters are taken from table 3.1.

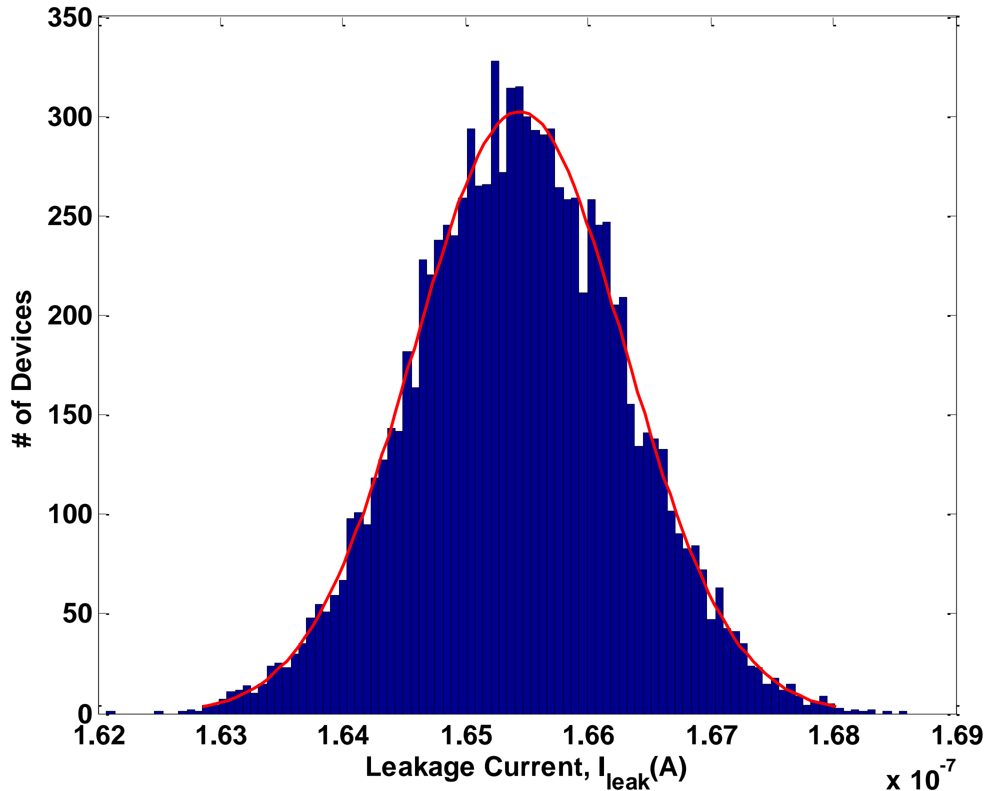


Figure 3.1.13: Leakage current distribution of Tz FinFET keeping W_{bot}= 15 nm, W_{top}= 13 nm, T_{ox}= 1 nm, $H_{fin=}$30 nm and N_{si}= 5×10^{18} cm^{-3}

The leakage current distribution found from figure 3.1.13 is symmetrical Gaussian distribution of 10000 transistors each having 4 fins using MATLAB function *"hist".* The leakage current distribution is spread for .05 $\times10^{-7}$ A wide. The highest Distribution rate is found in between 1.65×10^{-7} A to 1.66×10^{-7} A. Leakage current distribution is very influencing on power consumption of device.

3.2 Comparison of Trapezoidal and Rectangular shape FinFETs

In Rect shaped FinFETs the corner effect due to high doping concentration is effective. This effect is disadvantageous for device performance. An approach to change in Fin shape showed satisfactory improvement in device performance. As mentioned earlier the new shape of Fin is trapezoidal. In this section a comparative study between rectangular and trapezoidal shaped FinFET is done to give a clear view of device characteristics of both FinFET models.

The distinguishing process parameter between Tz and Rect shape TG FinFET is the Fin width which influences effective width W_{eff} as described in chapter 2.2.2 ($W_{eff} = 2H_{fin} + W_{fin}$). This effective width is incorporated in calculation of gate and channel capacitance shown in equation (6) and (7). Later on these capacitances are included in threshold voltage V_{Th} equation, thereby in leakage current equation. Considering this factor we simulate leakage current variation for Rect shaped as well as Tz shaped TG FinFET thus showing characteristic comparison between them. For simulation, we take the Fin width of Rect shape FinFET same as the bottom Fin width of Tz shape FinFET. Top Fin width of Tz shape is taken 2~3 nm less than the bottom one. Other parameter values are taken from table 3.1 for programming purpose. Comparison between the two device models are done based on variation of threshold voltage and leakage current variation. Further a comparison based on current distribution is done to understand the speed of operation.

3.2.1 Comparison based on Threshold Voltage variation with Fin Height

For both the model of FinFETs equation (4) is programmed changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of V_{Th} with H_{fin} is found which is shown in figure 3.2.1.

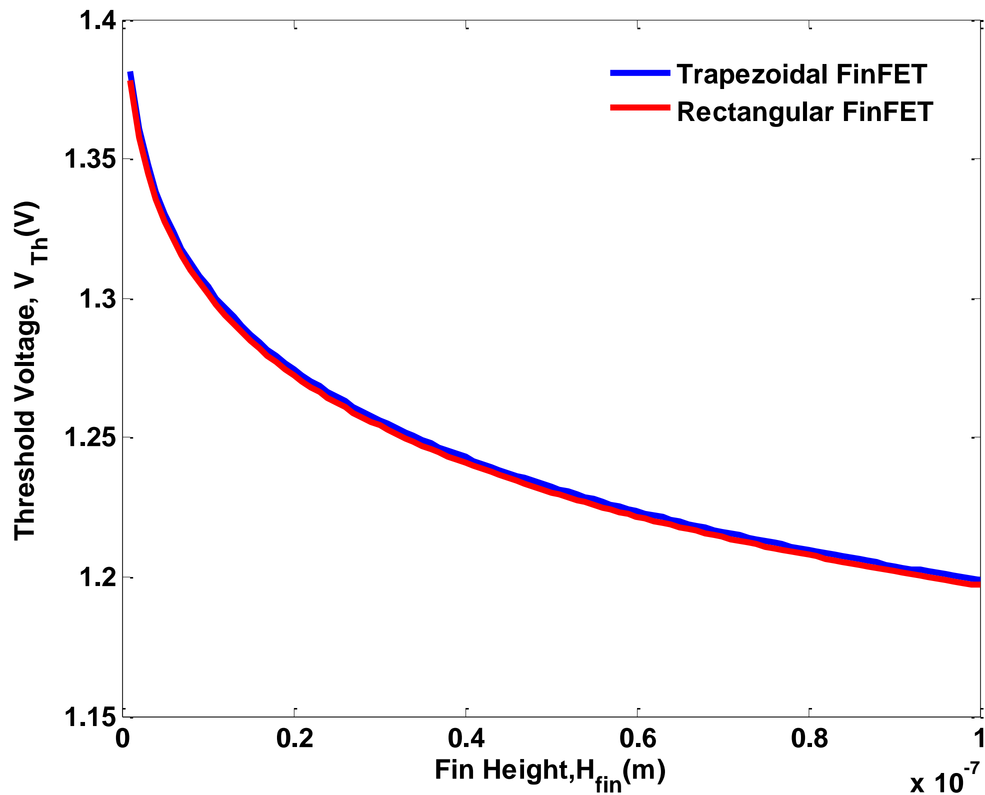


Figure 3.2.1: Variation of Threshold Voltage V_{Th} with Fin height H_{fin} forTz and Rect shaped TG FinFETs keeping T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

From figure 3.2.1 it's clearly seen that threshold voltage variation with Fin height H_{fin} of Tz and Rect shaped TG FinFET is very closely matched. So Threshold voltage deviation from Rect to Tz shaped FinFET device can be neglected while varying the Fin Height.

3.2.2 Comparison based on Leakage Current variation with Fin Height

Equation (14) is proggrammed corresponding to Tz shaped and Rect shaped FinFETs changing only Fin height from 0 to 1×10^{-7}m and keeping other parameter constant same as mentioned in table 3.1, the variation of leakage current with H_{fin} is found by monte carlo simulation which is shown in figure 3.2.2.

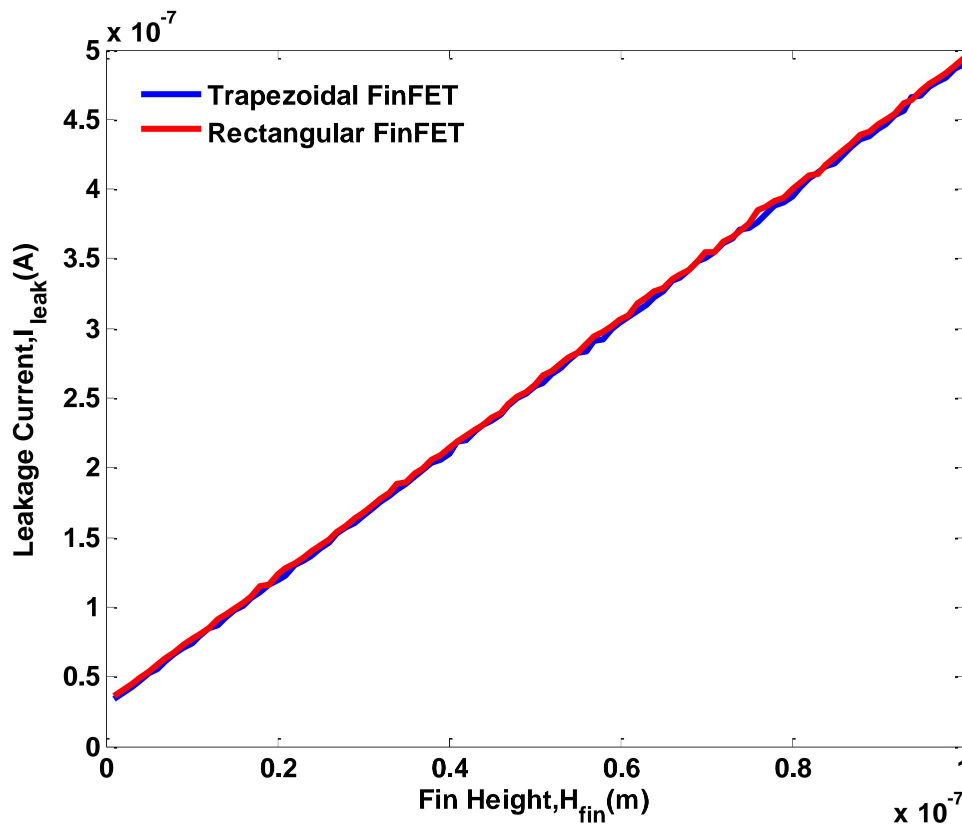


Figure 3.2.2: Lekage current variation I_{leak} with changing Fin height H_{fin} for Tz and Rect shaped TG FinFETs keeping T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

From figure 3.2.1, leakage current variation of Rect shaped FinFET with changing $H_{fin}$is slightly larger than that of TZ shaped FinFET. This small decrement in leakage current variation is an impact to use Tz shaped rather than Rect shape TG finFET in nano devices.

3.2.3 Comparison based on Threshold Voltage variation with Oxide Thickness

For both the model of FinFETs equation (4) is programmed changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table ,the variation of V_{Th} with T_{ox} is found which is shown in figure 3.2.3.

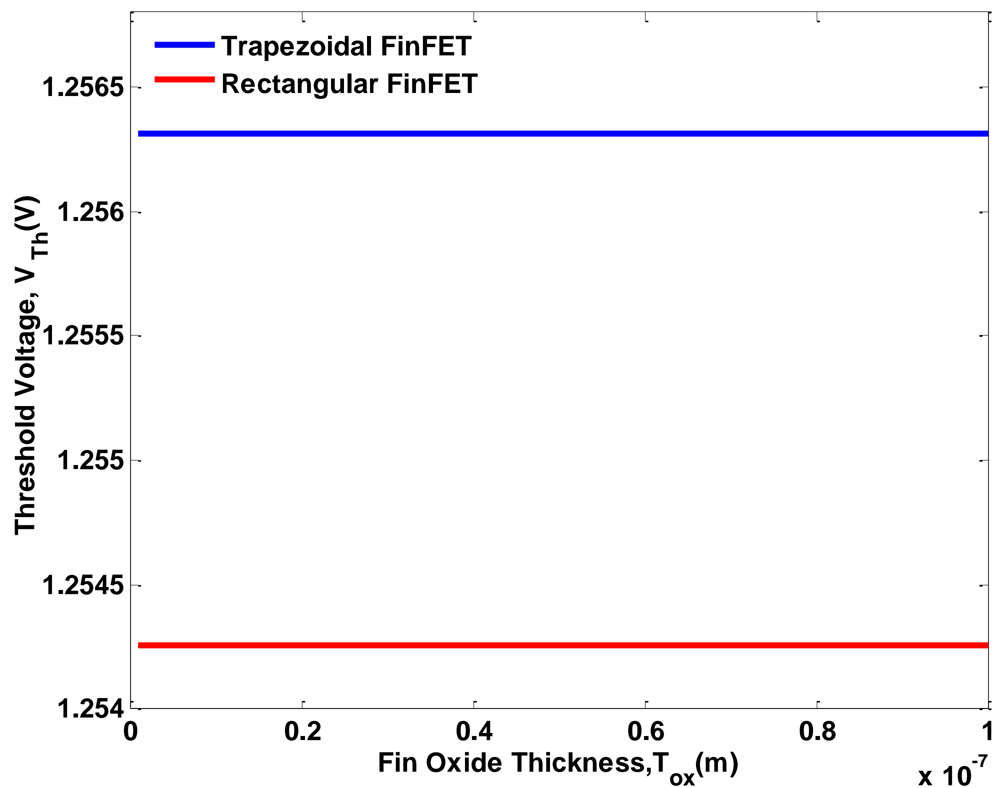


Figure 3.2.3: Variation of Threshold Voltage V_{Th} with Fin Oxide Thickness T_{ox} for Tz and Rect shaped TG FinFETs keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

Threshold voltage variation with Oxide Thickness is in similar pattern for Rect and Tz shaped TG FinFETs, there is no deviation in threshold voltage variation from Rect to Tz shape model. But the higher range of threshold voltage value found in Tz shape than Rect shape FinFET cause varity in their application.

3.2.4 Comparison based on Leakage Current variation with Oxide Thickness

Writing appropriate programming code for equation (14) corresponding to Tz and for Rect shaped FinFETs changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant the variation of leakage current with T_{ox} is found by monte carlo simulation which is shown in figure 3.2.4.

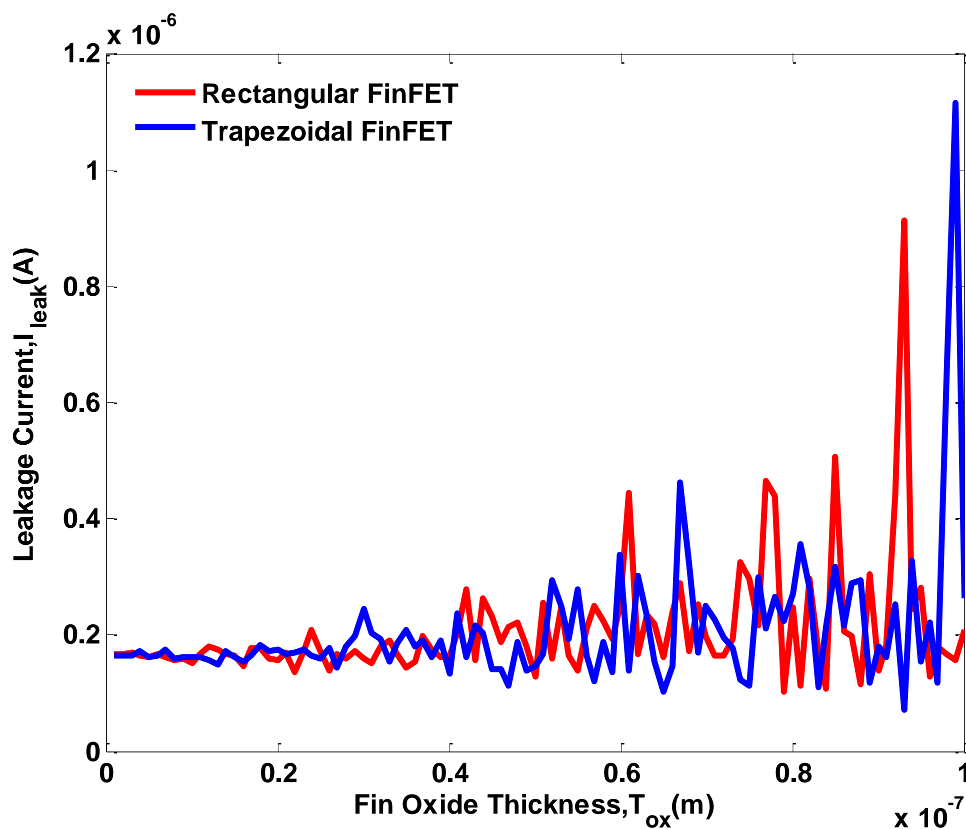


Figure 3.2.4: Leakage Current variation I_{leak} with changing Fin Oxide Thickness T_{ox} for Tz and Rect shaped TG FinFETs keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

Figure 3.2.4 shows that leakage current variation of Rect shaped FinFET with changing H_{fin} is closely matched to that of Tz shaped FinFET. At some point leakage current variation of Tz shaped FinFET shows larger spike than Rect shaped FinFET due to randomness.

3.2.5 Comparison of Threshold Voltage variation with Doping Concentration

For both the model of FinFETs equation (4) is programmed changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} the variation of V_{Th} with N_{si} is found which is shown in figure 3.2.5.

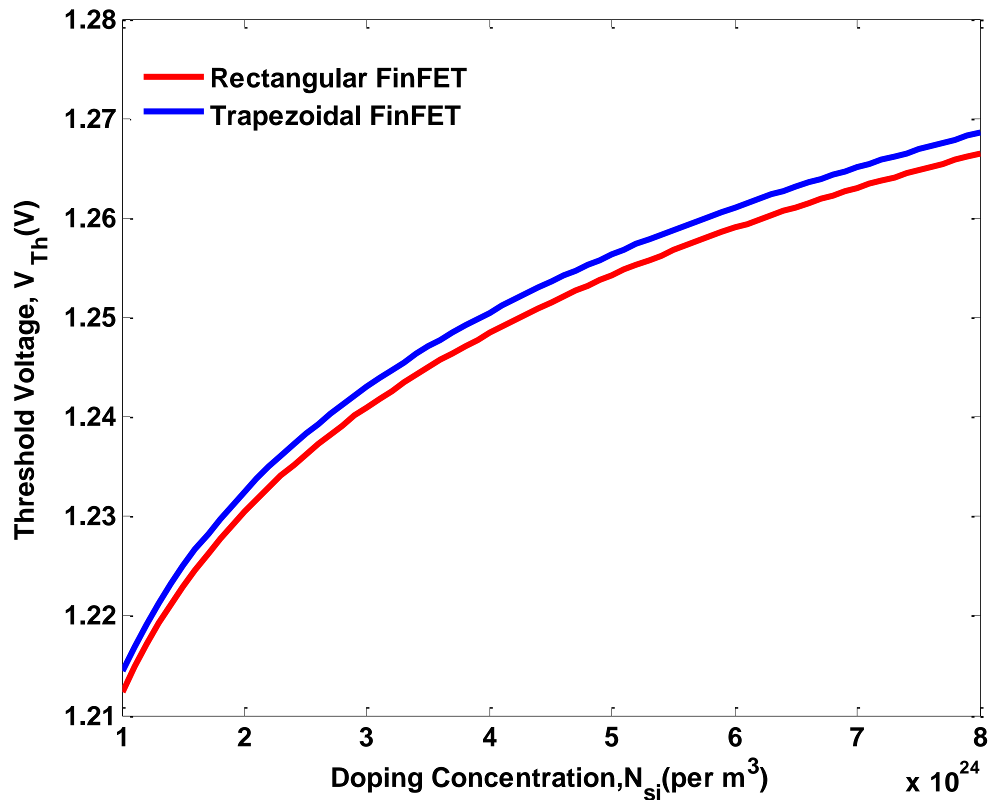


Figure 3.2.5: Variation of Threshold Voltage V_{Th} with changing Doping Concentration N_{si} for Tz and Rect shaped TG FinFETs keeping T_{ox}= 1 nm and H_{fin} = 30 nm

Threshold voltage variation with Doping Concentration is in similar pattern for Rect and Tz shaped TG FinFETs, deviation in threshold voltage variation from Rect to Tz shape model is not influencing factor. But the Tz shape shows higher range of threshold voltage value than Rect shape FinFET which may fill some criteria of application.

3.2.6 Comparison based on Leakage Current variation with Doping Concentration

Writing appropriate programming code for equation (14) corresponding to Tz shaped and Rect shaped FinFETs changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} and keeping other parameter constant the variation of leakage current with N_{si} is found by monte carlo simulation which is shown in figure 3.2.6.

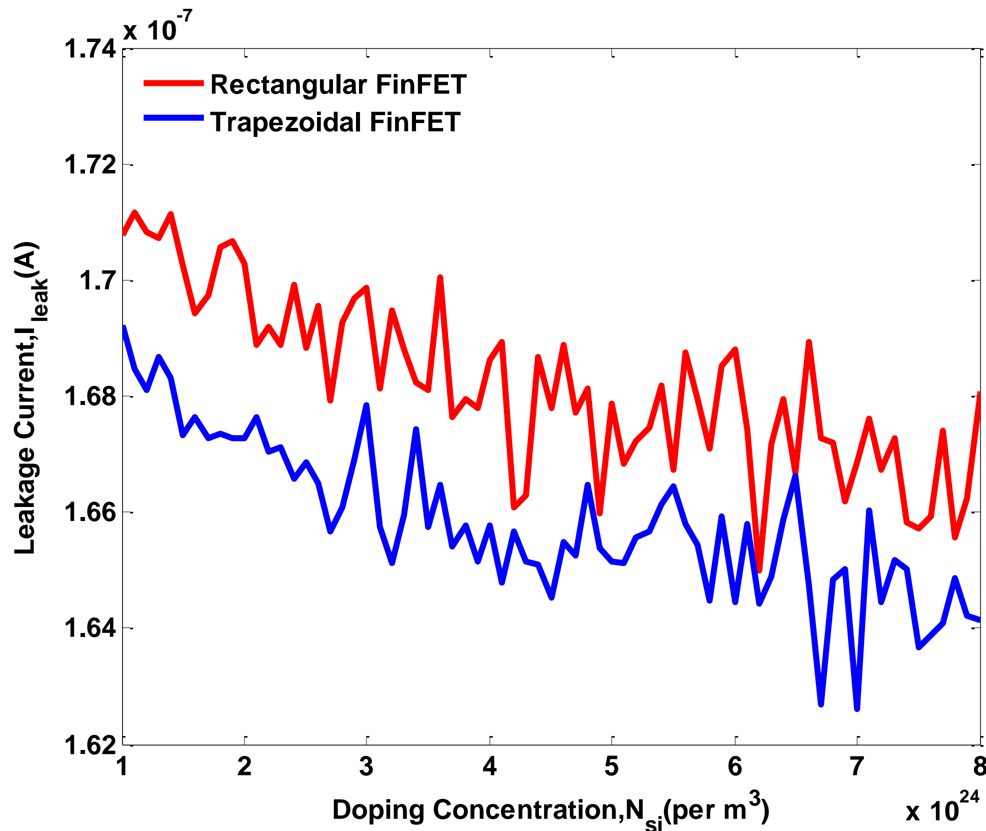


Figure 3.2.6: Leakage Current variation of I_{leak} with changing Doping Concentration N_{si} for Tz and Rect shape TG FinFETs keeping T_{ox}= 1 nm and H_{fin} = 30 nm

From figure 3.2.4, leakage current variation of Rect shaped FinFET with changing H_{fin} is larger than that of Tz shaped FinFET. For doping variation due to fabrication Rect shape FinFET is more vulnerable to produce affective leakage current than Tz shape FinFET.

3.2.7 Comparison based on Leakage Current Distribution

Equation (14) is programmed showing leakage current as sum of lognormals [116]. The simulated leakage current distribution of Tz-FinFET and Re-FinFET using statistical leakage current modeling method is shown in figure 3.2.7.

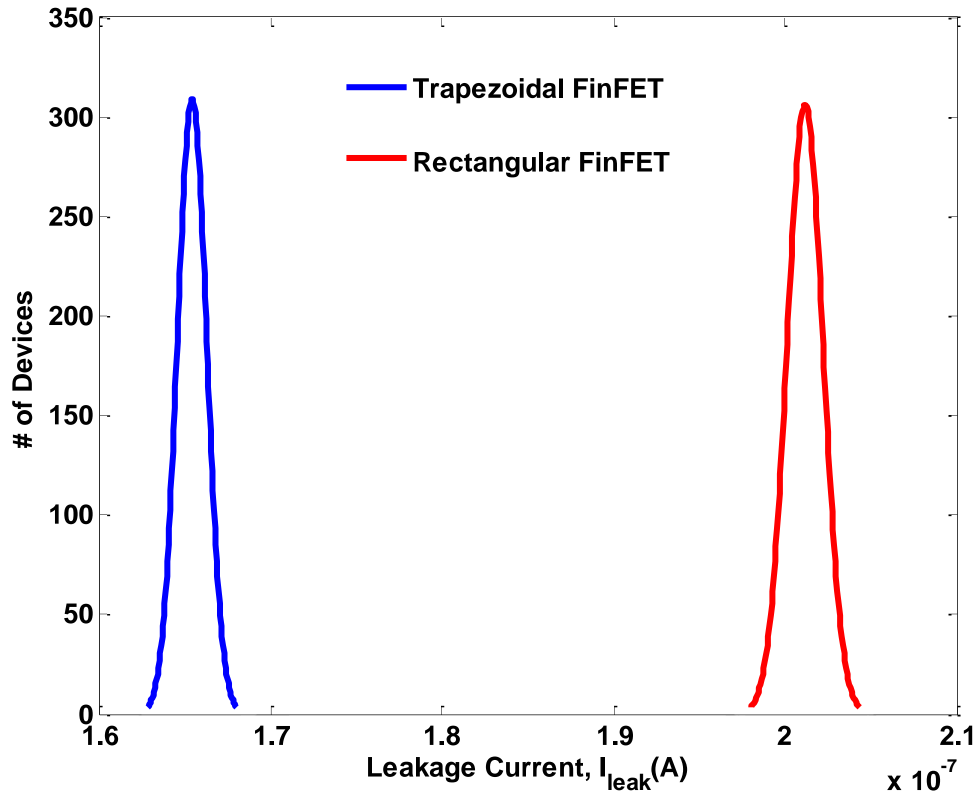


Figure 3.2.7: Leakage Current Distribution of Rect and Tz shaped FinFETs keeping T_{ox}= 1 nm, H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}. For Tz shape W_{bot}=15 nm, W_{top}=13 nm. For Rect W_{fin}=15 nm

It is notable from figure 3.2.7 that for rectangular FinFET the distribution of leakage current moves to the right. Therefore, Tz shaped FinFETs give less leakage current than the Rect shaped FinFET. As we know that the less the leakage current, the better will be the performance of a transistor.This property of Tz shaped FinFETs makes the operation of such devices faster compared to Rect shaped FinFETs.

3.3 Comparison of Trapezoidal and Triangular shape FinFETs

Corner effect due to high doping concentration found in Rect shape is overcome in trapezoidal shape FinFET. This approach of changing Fin shape from rectangular to trapezoidal shaped TG FinFET actually interprets to decrease top Fin width. So least top Fin Width is supposed to show more satisfactory improvement in device performance. Least top Fin width corresponds to triangular shaped TG FinFET. In this section a comparative study between triangular and trapezoidal shaped FinFET is done to give a clear view of device characteristics of both FinFET model.

The distinguishing process parameter between Tz and Tr shaped TG FinFET is the Fin width which influences effective width W_{eff} as described in chapter 2.2.2 ($W_{eff} = 2H_{fin} + W_{fin}$). This effective width is incorporated in calculation of gate and channel capacitance shown in equation (6) and (7). Later on these capacitances are included in threshold voltage V_{Th} equation, thereby in leakage current equation. Considering this factor we simulate leakage current variation for Tr shaped as well as Tz shaped TG FinFET thus showing characteristic comparison between them. For simulation, we take the Fin width of Tr shape FinFET same as the bottom Fin width of Tz shape FinFET. Top Fin width of Tz shape is taken 2~3 nm less than the bottom one. Other parameter values are taken from table 3.1 for programming purpose. Comparison between the two device models are done based on variation of threshold voltage and leakage current variation. Further a comparison based on current distribution is done to understand the speed of operation.

3.3.1 Comparison based on Threshold Voltage variation with Fin Height

For both the model of FinFETs equation (4) is programmed changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table 3.1, the variation of V_{Th} with H_{fin} is found which is shown in figure 3.3.1.

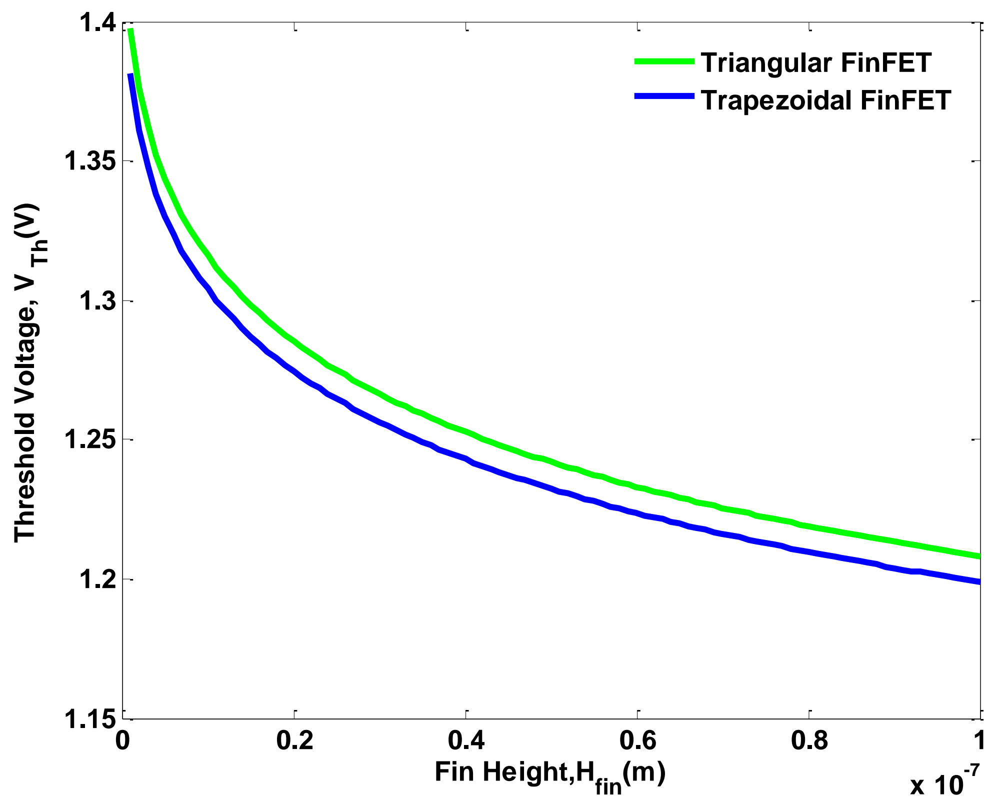


Figure 3.3.1: Variation of Threshold Voltage $V_{th}$with Fin height H_{fin} forTz and Tr shape TG FinFETs keepingT_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

From figure 3.2.1 it's clearly seen that threshold voltage variation with Fin height H_{fin} of Tz and Rect shaped TG FinFET is very closely matched in pattern. But the range of variation is higher in Tr shape than Tz shaped TG FinFET.

3.3.2 Comparison based on Leakage Current variation with Fin Height

Writing appropriate programming code for equation (14) corresponding to Tz shape and Tr shape FinFETs changing only Fin height from 0 to 1×10^{-7} m and keeping other parameter constant the variation of leakage current with H_{fin} is found by monte carlo simulation which is shown in figure 3.3.2.

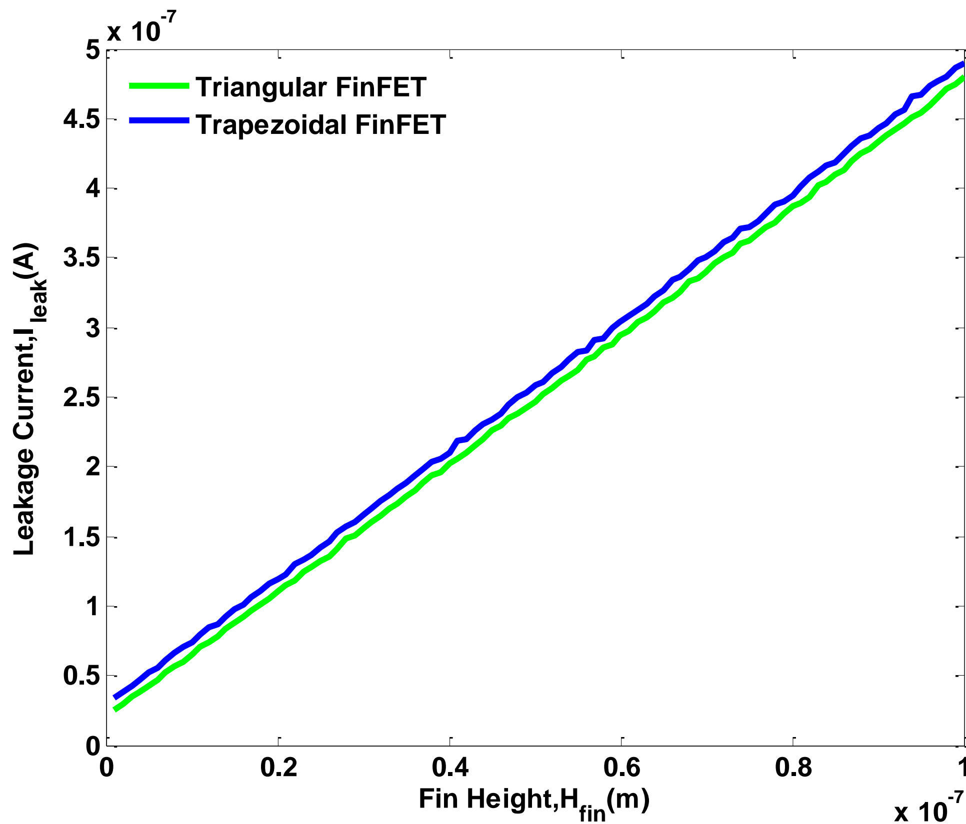


Figure 3.3.2: Leakage Current variation of Threshold Voltage V_{Th} with Fin height H_{fin} forTz and Tr shaped TG FinFETs keeping T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

From figure 3.3.2, leakage current variation of Tr shape FinFET with changing H_{fin} is less than that of Tz shape FinFET. But the similar pattern of resulting graph depicts negligible deviation of leakge current variation from Tz to Tr shaped TG FinFETs.

3.3.3 Comparison based on Threshold Voltage variation with Oxide Thickness

For both the model of FinFETs equation (4) is programmed changing only oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant same as mentioned in table ,the variation of V_{Th} with T_{ox} is found which is shown in figure 3.3.3.

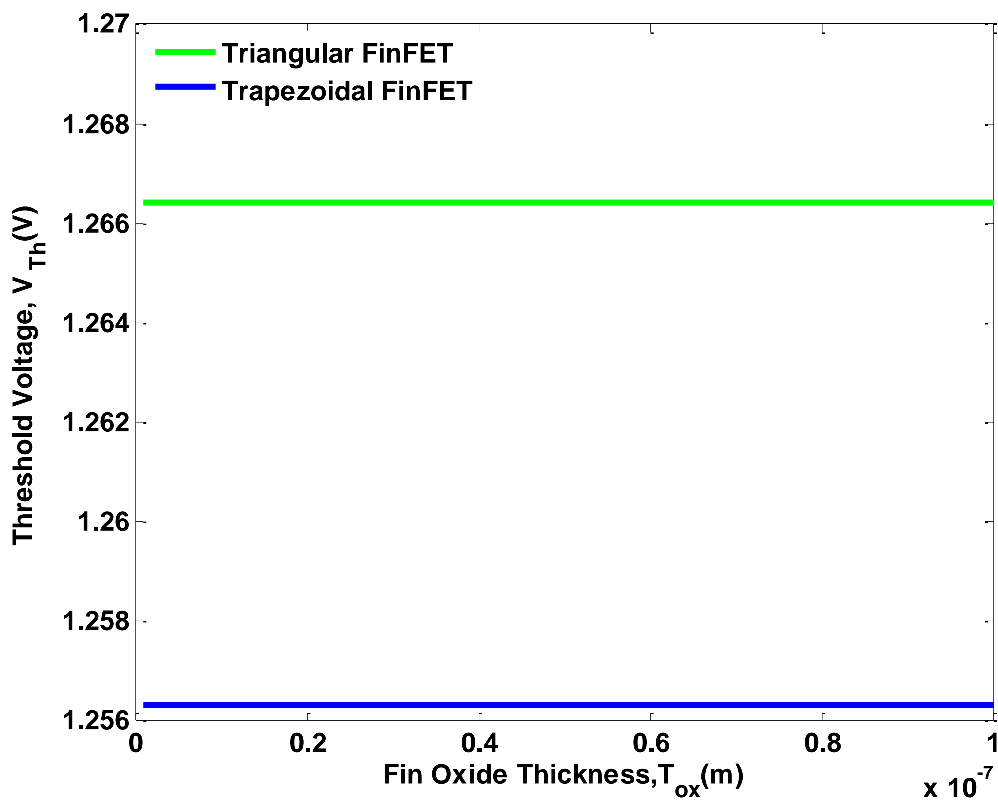


Figure 3.3.3: Variation of Threshold Voltage V_{Th} with Fin Oxide Thickness T_{ox} for Tz and Tr shaped TG FinFETs keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

Threshold voltage variation with Oxide Thickness is in similar pattern for Tr and Tz shaped TG FinFETs, there is no deviation in threshold voltage variation from Tr to Tz shape model. But the higher range of threshold voltage value found in Tr shape than Tz shape FinFET cause varity in their application.

3.3.4 Comparison based on Leakage Current variation with Oxide Thickness

Writing appropriate programming code for equation (14) corresponding to Tz shape and Tr shape FinFETs changing only Oxide thickness from 0 to 1×10^{-7} m and keeping other parameter constant the variation of leakage current with T_{ox} is found by monte carlo simulation which is shown in figure 3.3.4.

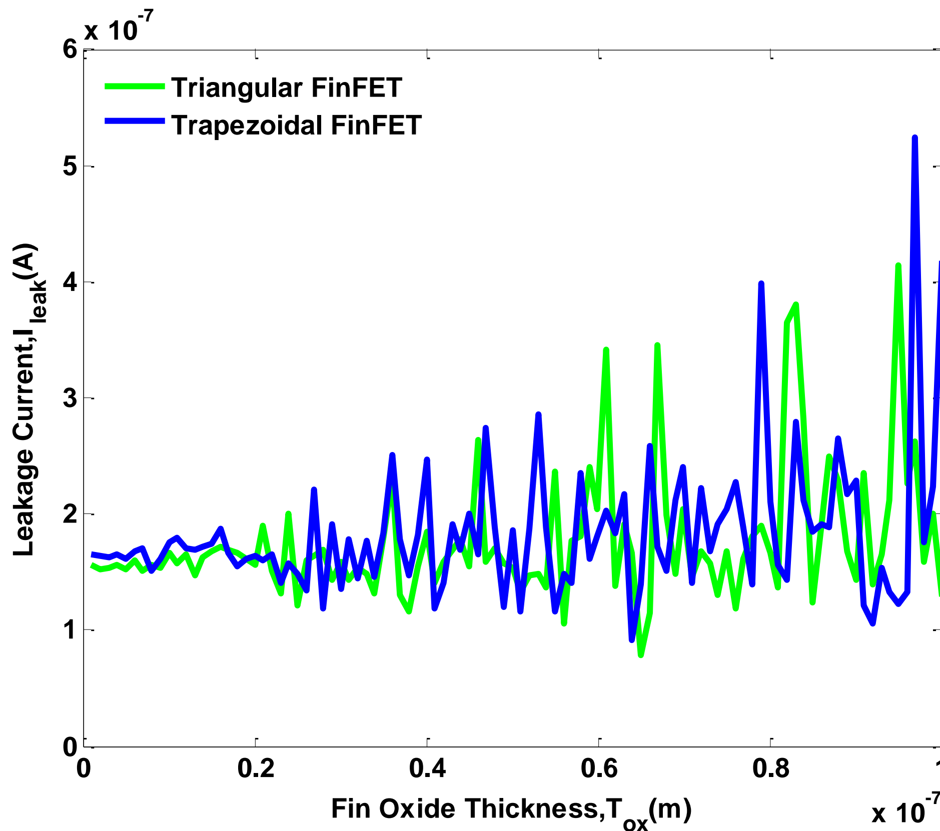


Figure 3.3.4: Leakage Current variation I_{leak} with changing Fin Oxide Thickness T_{ox} for Tz and Tr shaped TG FinFETs keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

Figure 3.3.4 shows that leakage current variation of Tr shape FinFET with changing H_{fin} is closely matched to that of Tz shaped FinFET. At some point leakage current variation of Tz shaped FinFET shows larger spike than Tr shaped FinFET due to randomness.

3.3.5 Comparison based on Threshold Voltage variation with Doping Concentration

For both the model of FinFETs equation (4) is programmed changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} the variation of V_{Th} with N_{si} is found which is shown in figure 3.3.5.

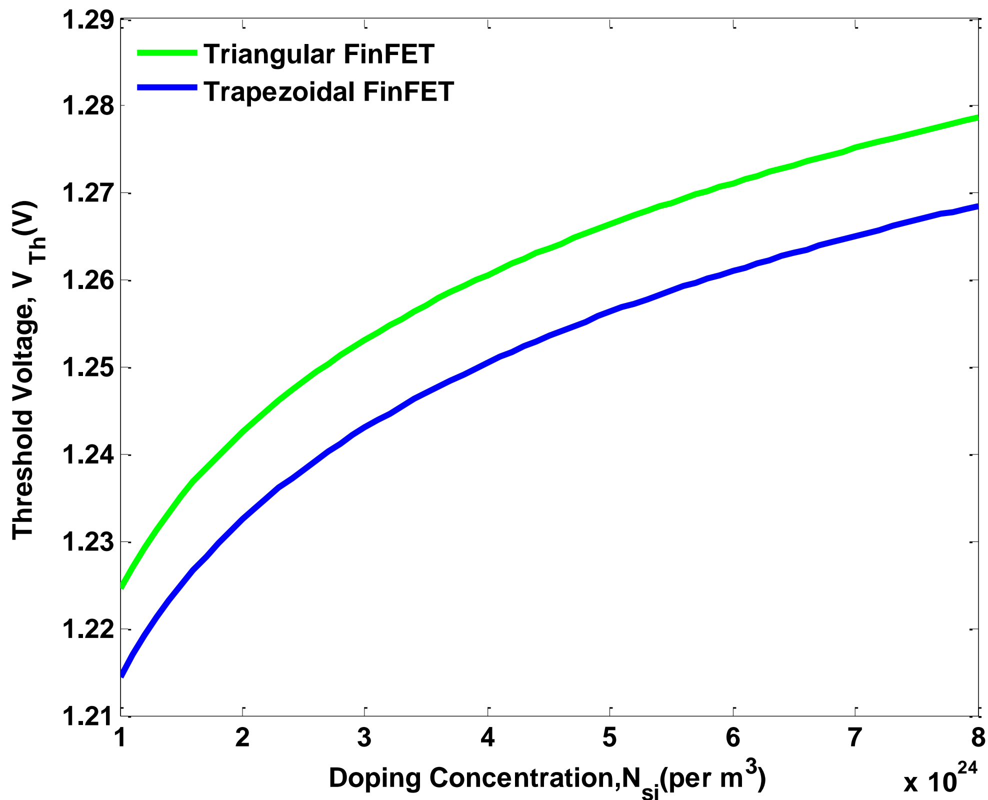


Figure 3.3.5: Variation of Threshold Voltage V_{th} with changing Doping Concentration N_{si} for Tz and Tr shaped TG FinFET keeping T_{ox}= 1 nm and H_{fin} = 30 nm

Threshold voltage variation with Doping Concentration is in similar pattern for Tr and Tz shaped TG FinFETs, deviation in threshold voltage variation from Tz to Tr shape model is not influencing factor. But the Tr shape shows higher range of threshold voltage value than Tz shape FinFET which may fill some criteria of application.

3.3.6 Comparison based on leakage current variation with Doping Concentration

Writing appropriate programming code for equation (14) corresponding to Tz shaped and Tr shape FinFETs changing only doping concentration from 1 m^{-3} to 1×10^{24} m^{-3} and keeping other parameters constant the variation of leakage current with N_{si} is found by monte carlo simulation which is shown in figure 3.3.6.

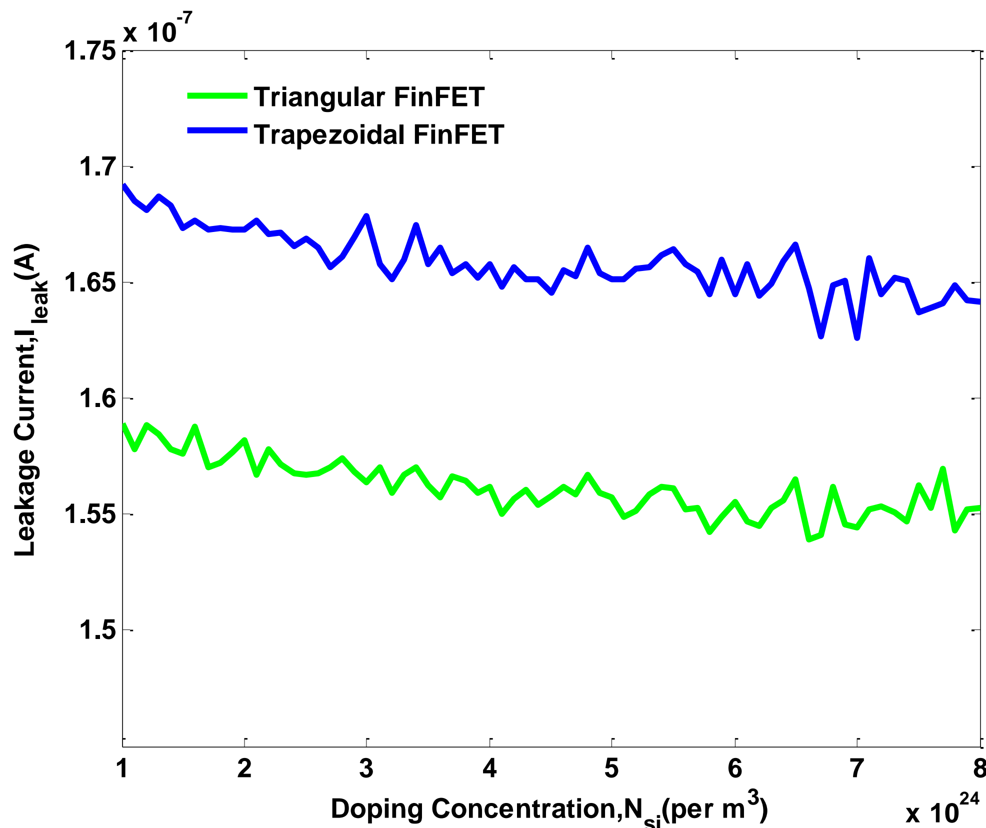


Figure 3.3.6: Leakage Current variation of I_{leak} with changing Doping Concentration N_{si} for Tz and Tr shape TG FinFET keeping T_{ox}= 1 nm and H_{fin} = 30 nm

From figure 3.3.6, leakage current variation of Tr shape FinFET with changing H_{fin} is less than that of Tz shaped FinFET. For doping variation due to fabrication Tz shape FinFET is more vulnerable to produce affective leakage current than Tr shape FinFET.

3.3.7 Comparison based on Leakage Current Distribution

Equation (14) is programmed showing leakage current as sum of lognormals [116]. The simulated leakage current distribution of Tz FinFET and Tr FinFET using statistical leakage current modeling method is shown in figure 3.2.7.

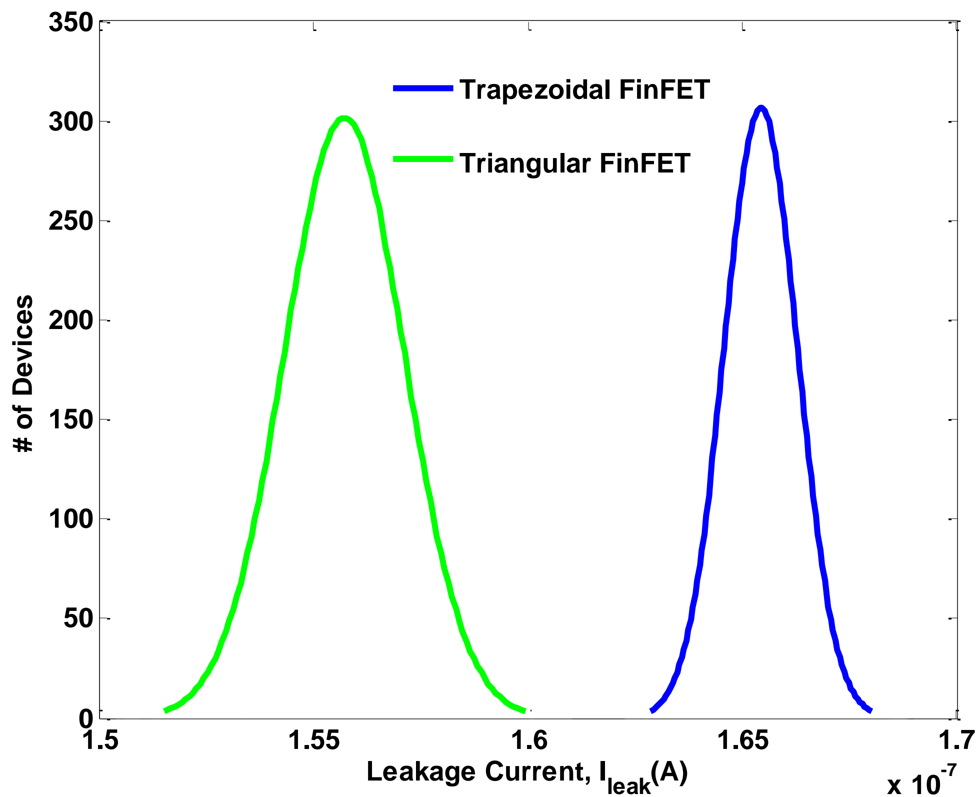


Figure 3.3.7: Leakage Current Distribution of Tr and Tz shaped FinFETs keeping T_{ox}= 1 nm, H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}. For Tz shape W_{bot}=15 nm, W_{top}=13 nm.For Tr W_{fin}=15 nm

It is notable from figure 3.3.7 that for trapezoidal FinFET the distribution of leakage current moves to the right. Therefore, Tr shaped FinFETs give less leakage current than the Tz shape FinFET.

3.4 Comparison among Trapezoidal, Rectangular and Triangular shape FinFETs

In chapter 3.2 and 3.3 the Tz shape FinFET is compare to Rect shape and Tr shape FinFETs respectively. In this section all the three model of different Fin shaped FinFETs are analyzed altogether based on their variation of threshold voltage and leakage current variation. Comparison based on distribution of leakage current directs to prediction of device speed. The results of the analysis are shown in the following figures.

3.4.1 Comparison based on Leakage Current Distribution

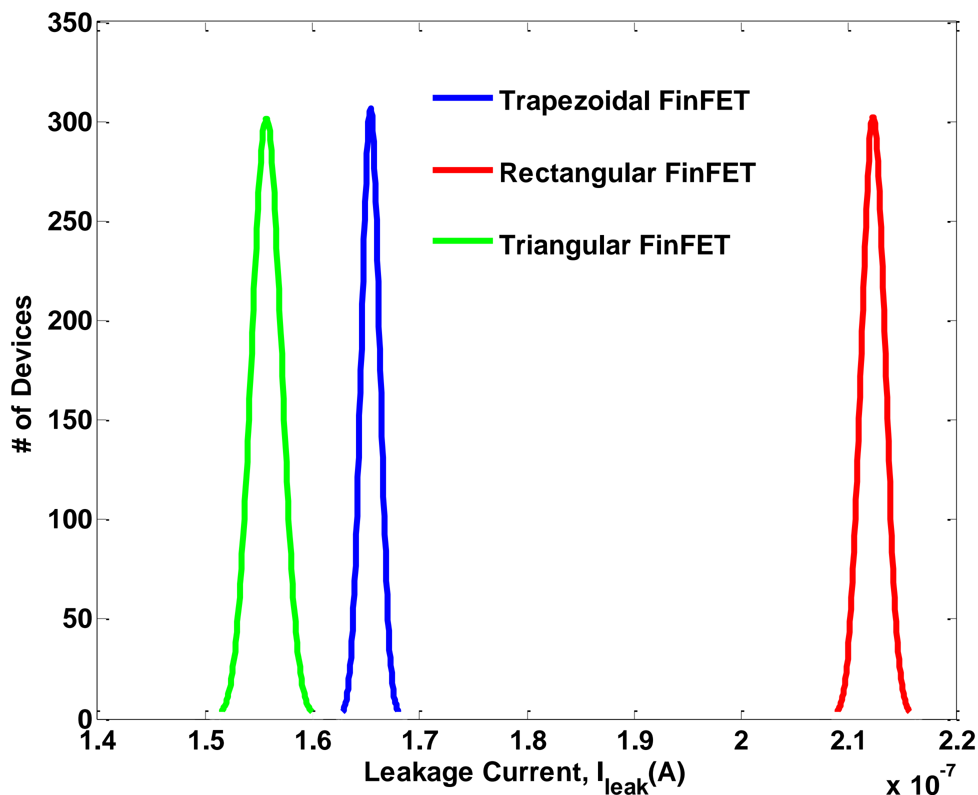


Figure 3.4.1: Leakage Current Distribution of Tz, Rect and Tr shaped FinFETs keeping T_{ox}= 1 nm, H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}. For Tz shape W_{bot}=15 nm, W_{top}=13 nm.For Tr W_{fin}=15 nm

3.4.2 Comparison based on Threshold Voltage and Leakage Current variation with Fin Height

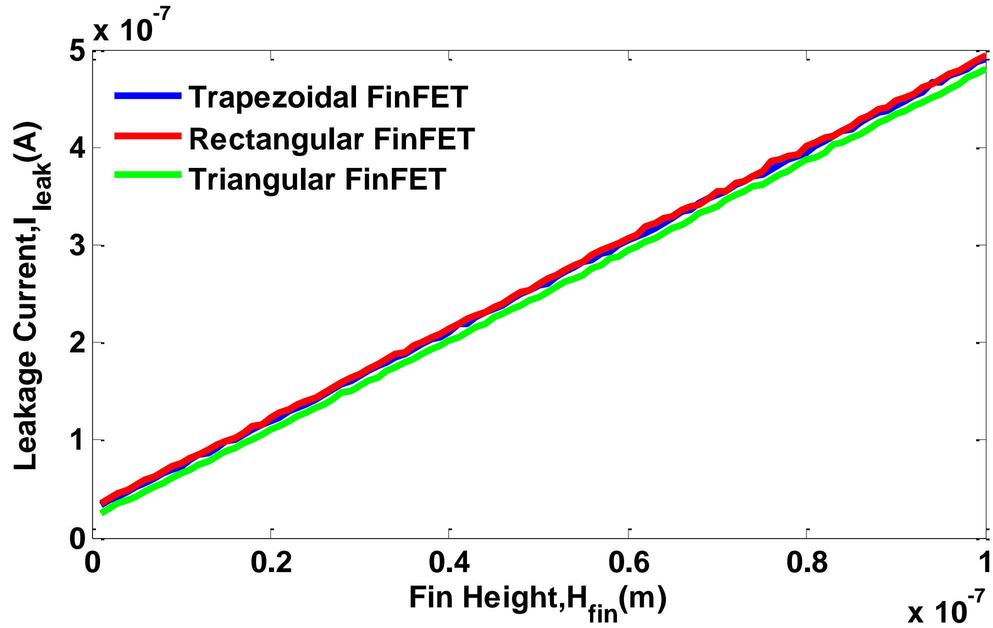


Figure 3.4.2(a): Variation of Threshold Voltage V_{Th} with Fin height H_{fin} for Tz, Rect and Tr shape TG FinFETs keeping T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

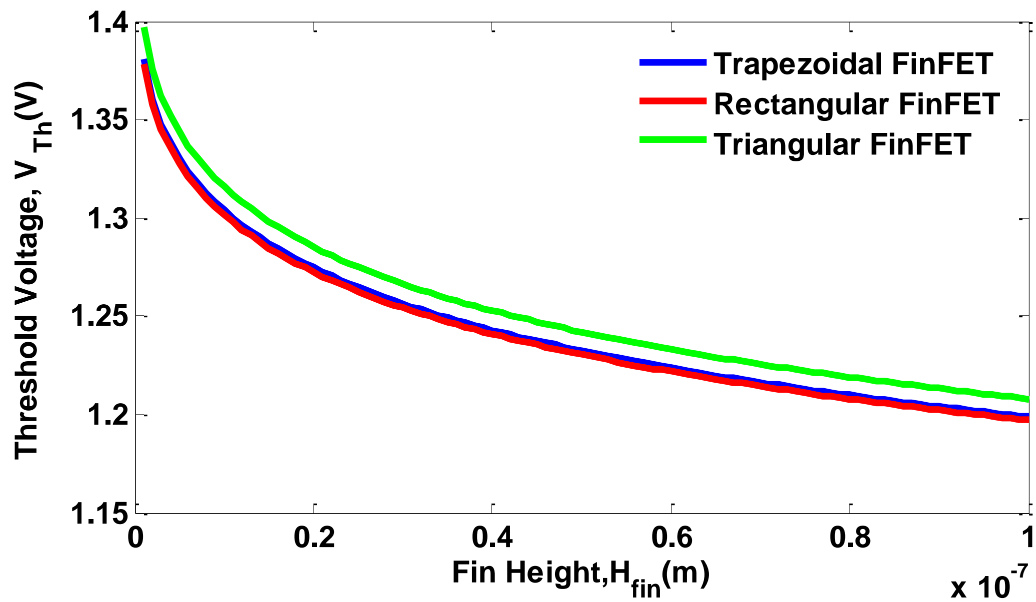


Figure 3.4.2(b): Leakage Current variation I_{leak} with Fin height H_{fin} forTz, Rect and Tr shape TG FinFETs keeping T_{ox}= 1 nm and N_{si}= 5×10^{18} cm^{-3}

3.4.3 Comparison based on Threshold Voltage and Leakage Current variation with Oxide Thickness

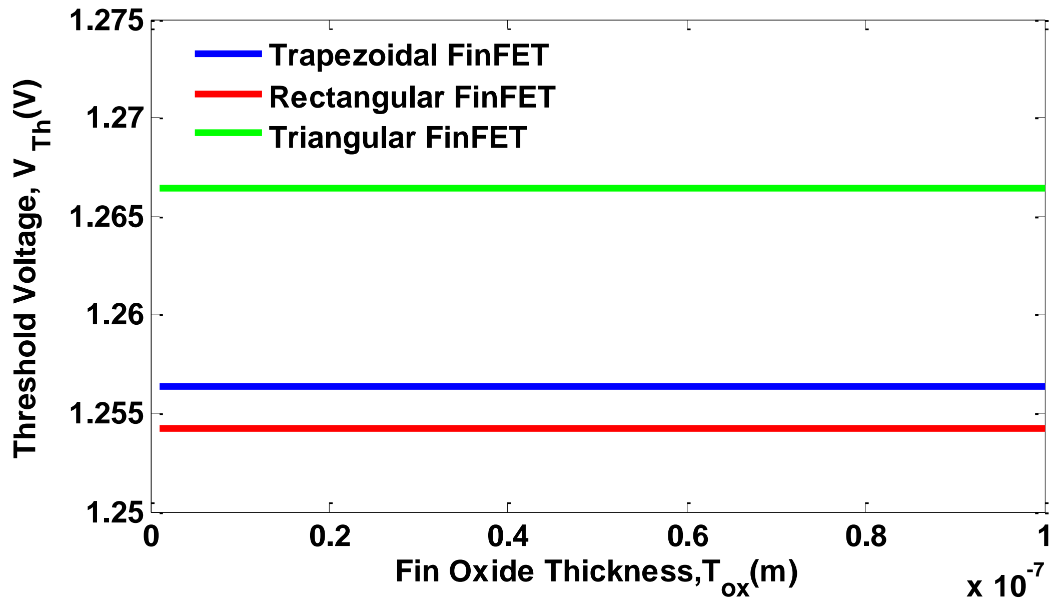


Figure 3.4.3(a): Variation of Threshold Voltage V_{Th} with Fin Oxide Thickness T_{ox} for Tz, Rect and Tr shape TG FinFET keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

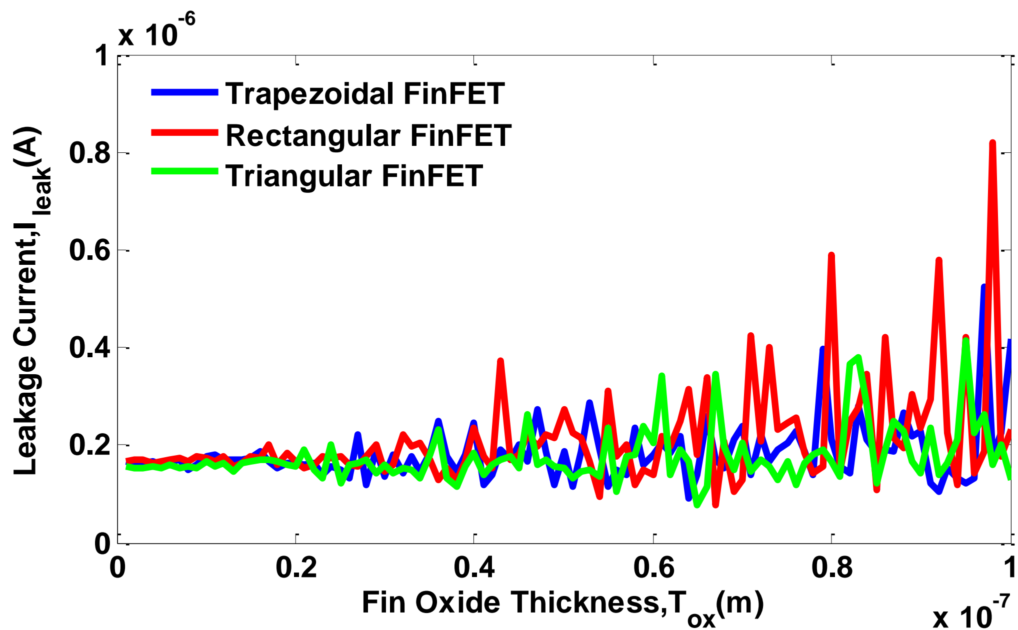


Figure 3.4.3(b): Leakage Current variation I_{leak} with changing Fin Oxide Thickness T_{ox} for Tz, Rect and Tr shaped TG FinFET keeping H_{fin}= 30 nm and N_{si}= 5×10^{18} cm^{-3}

3.4.4 Comparison based on Threshold Voltage and Leakage Current variation with Doping Concentration

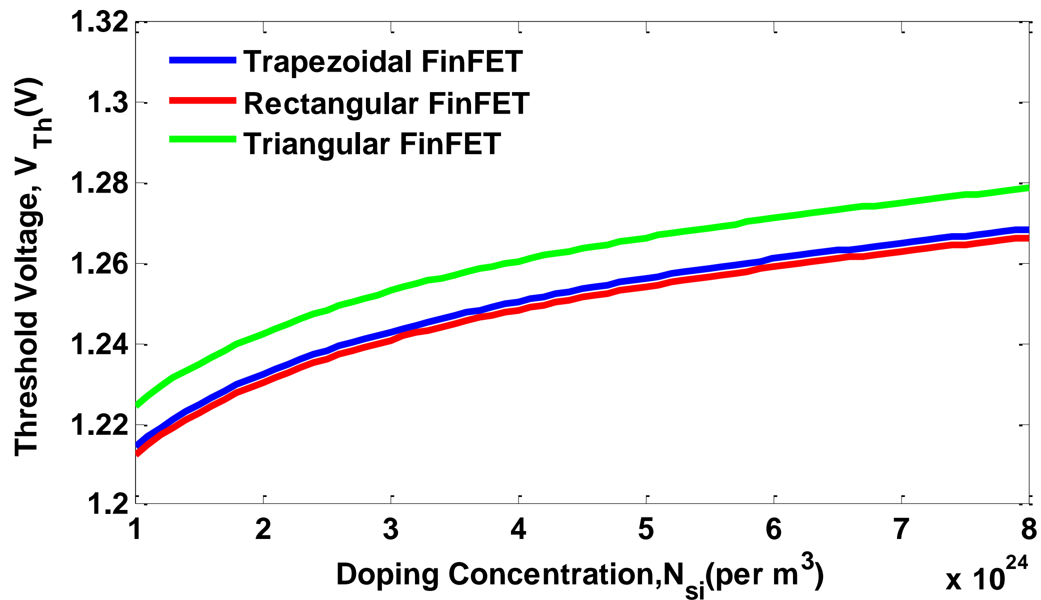


Figure 3.4.4(a): Variation of Threshold Voltage V_{Th} with changing Doping Concentration N_{si} for Tz, Rect and Tr shaped TG FinFET keeping T_{ox}= 1 nm and H_{fin} = 30 nm

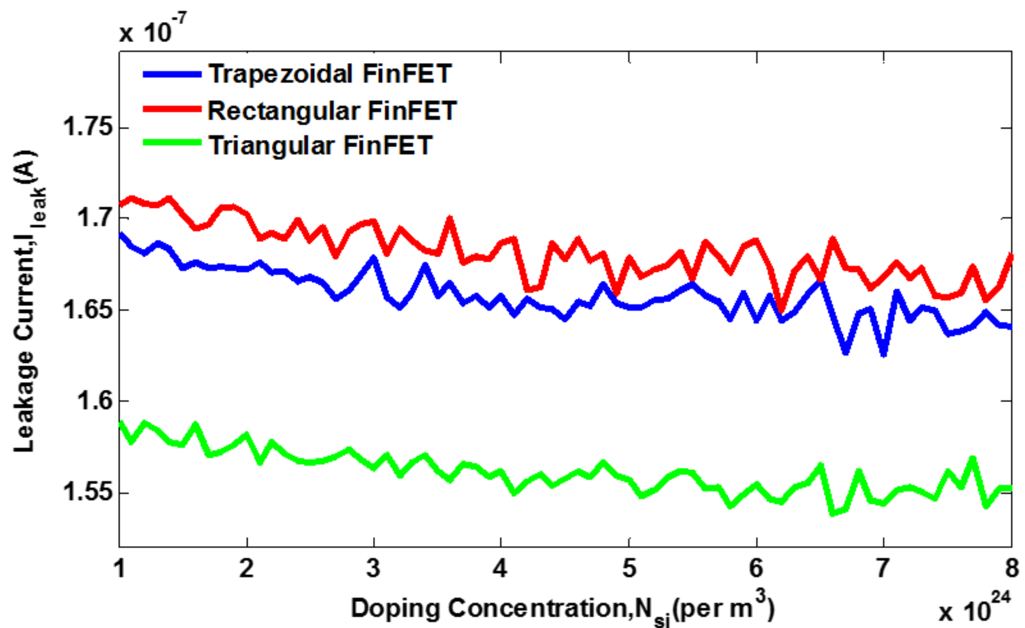


Figure 3.4.4(b): Leakage Current variation of I_{leak} with changing Doping Concentration N_{si} for Tz, Rect and Tr shape TG FinFET keeping T_{ox}= 1 nm and H_{fin} = 30 nm

CHAPTER FOUR

An overall discussion on prescribed working method and the outcome is necessary to reveal the impact of thesis work. In this chapter the idea and suggestions are summarized as per the simulated results found in previous chapters. Statements founded from simulated results is matched to practical phenomenon to apply the knowledge for further practical improvement. We discuss some scopes to extend this work in future for further improvement.

4.1 Conclusion

The continuous scaling of CMOS technology has dramatically improved the performance of modern microprocessors. However, it also creates more challenges for designers to overcome in order to take the advantages of the technology scaling. Among all the issues brought by the aggressively scaled transistor size, power and process variation poses the most serious threat to the circuits' performance. This thesis focuses on statistical leakage current analysis of trapezoidal shape trigate FinFET under process variation. Device leakage current varies considerably under process variation due to the exponential relationship between leakage current and threshold voltage. Accurate prediction of leakage current is crucial for maintaining the functionality of circuit as well as meeting the power budget. This work investigates the variation of threshold voltage of Tz shaped TG FinFET based on device parameters.The simulated results show dependency of threshold voltage on device dimension. Leakage current distribution under consideration of process inputs such as the mean threshold voltage (V_{Th}) and standard deviation of V_{Th} due to process parameter variation leads to accurate modeling of leakage current. We show that because of the lognormal function of leakage, the conventional modeling of threshold voltage variation underestimates both mean and standard deviation of leakage current. Again leakage current variation with physical parameters under the impact of atomistic Random Dopant Fluctuation

(RDF) is simulated by generating random dopant in each Fin of our multifin device taking in account the doping variation while processing. A Monte Carlo simulation results manifests the impact of process variation on leakage current more practically. The analysis unfolds the influence of different fin number leading the fact that four fin model process less leakage current variation. The comparative study of trapezoidal and rectangular shaped TG FinFETs interprets the performance improvement of trapezoidal shape FinFET. Though in a TG FinFET the faster gate operation is possible that subsequently process much reduced leakage current compared to traditional MOSFETs , Comparison of Tz and Rect shape FinFETs according to leakage current variation distinguish the two model on more logical and practical argument. The analysis incorporates effective width W_{eff} which is a helpful parameter to understand transistor model and it's operation after biasing. Distribution of leakage current for trapezoidal and rectangular shape FinFETs very accurately indicates faster speed operation of trapezoidal TG FinFET. From the statement of this study, further analysis of triangular and trapezoidal shaped TG FinFETs leads to better understanding of the impact of Fin shape on device performance on the basis of statistical leakage current modeling. The analysis method based on compact model of FinFET and simulated results would help to predict performance of FinFETs accurately regarding practical applications.

4.2 Future Scopes

If there is no charge present in the oxide or at the oxide-semiconductor interface, the flatband voltage simply equals the difference between the gate metal workfunction (φ_g) and the semiconductor workfunction (φ_s) that is flatband voltage, $V_{fb} = \varphi_g - \varphi_s$. When the band is flat in the body the surface electric field in the substrate is zero. Therefore the electric field in the oxide is also zero. In our thesis we consider V_{fb}as zero without studying the energy band diagram for a special bias condition which is called the flat-band condition. For further analysis V_{fb}calculation can be taken in account or some method for TG FinFET can be introduced to determine it.

Device performance is highly dependent on capacitance modeling. Fringing capacitance resulting from geometry changes has significant impact on FinFET performance. A 3-D fringing capacitance model can be carried out for the FinFET devices at 22-nm-technology node considering the 3-D device structures, such as spacer width and material, gate-electrode thickness, as well as fin pitchthrough fringing field.

Compact delay model for MOS devices is reported in various researches. But an appropriate delay model for TG FinFET can be done in future. Propagation delay Tp corresponds to process variation on subthreshold circuit delay. Thus delay modeling of FinFETs will help to understand its performance in switching circuit.

Statistical leakage current distribution is dependent on standard deviation of threshold voltage. In future work current distribution for trapezoidal TG FinFETs can simulated regarding this parameter. Variation in fin number can also be taken in account.

An analytical model for trapezoidal TG FinFET is considered for our simulation in MATLAB which is equation based. For further approach the device model can be simulated in design tool softwars such as ATLAS or CAD tool. This may help to define accuracy or sensitivity of analysis. Expressions found previously can be upgraded or approximated by relating the MATLAB results to that found by Designing softwar.

In our thesis work we evaluate FinFET performance on the basis of statistical leakage current analysis. More sophisticated technique can include statistical energy analysis. In further aspects statistical energy distribution under RDF consideration can be done to determine device performance.

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Appendix

Abbreviations

IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
BOX	Buried Oxide
MISFET	Metal Insulator Semiconductor Field-Effect Transistor
ITRS	International Technology Roadmap for Semiconductors
ULSI	Ultra Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
SCE	Short Chanel Effect
MuGFET	Multiple Gate Field Effect Transistor
MIGFET	Multiple Independent Gate Field Effect Transistor
SOI	Silicon on Insulator
DG	Double Gate
TG	Tri Gate
4T	Four Terminal
3T	Three Terminal
AMD	Advanced Micro Devices
IDF	Intel Developer Forum
SRAM	Static Random Access Memory
EOT	Effective Oxide Thickness
HVT	High Voltage Threshold
SVT	Standard Voltage Threshold

RDF	Random Dopant Fluctuation
SEM	Scanning Electron Microscope
V_{GS}	Gate to Source Voltage
RDD	*Random Discrete Dopants*
LER	Line Edge Roughness
MGG	Metal Gate Granularity
ITC	Interface Trapped Charges
VLSI	Very Large Scale Integration
CMC	Compact Model Council
BSIM-CMG	Berkeley Short-channel IGFET Model – Common Multi-Gate
Tz	Trapezoidal
Rect	Rectangular
Tr	Triangular
GIDL	Gate Induced Drain Leakage
BTBT	Band to Band Tunneling
WF	Work Function
G-S/D	Gate- Source/Drain
PDF	Probability Density Function
CDF	Cumulative Density Function
CMP	Chemical Mechanical Polishing
GER	Gate Edge Roughness