Chapter 1

Introduction

In most of the electronic systems the input and output signals are analog in nature. Hence there are analog processing devices like amplifiers as input and output devices. However most of the modifications to be carried out on the input signals before obtaining the outputs are carried out in digital domain. Therefore, there is a need to convert the analog input signals into digital signals at the input end, and after processing them in the digital domain; they have to be converted back into analog signals in most of the applications. The circuits that convert analog signals to digital signals are known as analog to digital converters and the circuits that convert digital signals to analog signals are called digital to analog converters (DACs).

The penetration of electronics into areas like computers, communications, instrumentation and embedded systems such as mobile phones, camcorders, HDTVs has given rise to the need for DACs with stringent requirements. Digital-analog converters (DAC's) are known in the most diversified specific embodiments and are always used when digital numerical values, which are stored, for instance, in a storage component have to be converted to (quasi) analog voltages.

A fault in a digital to analog converter often leads to functional disturbances in the entire circuit. If a chip manufacturer guarantees a certain maximum fault rate, this may be maintained possibly only by using fault detection circuits or testing circuits.

1.1 Problem Description

The thesis attempts at detecting fault of a digital to analog converter which is insensitive to mainly temperature to some extent. The techniques that are described here to detect fault of a digital to analog converter is to achieve higher accuracy, good speed and lower power have been adopted. It is therefore desirable to simplify the fault detection in a digital to analog converter circuit and particularly to make it available.

The fault detection of digital to analog converter has been achieved by two steps:

- By changing frequencies. This enables to understand the characteristics of faults at various frequency components.
- By making the components of the circuit (resistance & capacitance) by stuck on (or stuck-on) or stuck open (or stuck-off) fault detection process.

1.2 Thesis Contribution

The key contributions of this thesis are:

Fault detection and localization of 8-bit digital to analog converter. We compared between the faulty circuit and a fault free circuit (golden circuit) with the gain obtained by changing frequency.

This thesis therefore aims to describe the fundamentals of analog testing to analyze the difficulties of analog testing and to develop an approach to test the analog components. To test the circuit, stuck on (or stuck-on) & stuck open (or stuck-off) fault detection method is used. The proposed test method takes the advantage of good fault coverage through the use of a simple stuck open-stuck on based test technique. It describes the deviation of ideal of the transfer function which is categorized into gain error are used for fault diagnosis. Simulation results are provided to demonstrate the feasibility, usefulness, and relevance of the proposed implementations**.**

1.3 Thesis Organization

The thesis is organized as follows:

Chapter 1- Introduction: Introduction to the thesis

Chapter 2- Digital to Analog Converter & concerned faults: Overview of the various types of DAC and related faults

Chapter 3- Related Work: A survey of latest developments in fault detection process of benchmark circuits.

Chapter 4- Operation of 8 Bit DA Converter: Circuit & operation of DAC according to ITC'97 Benchmark Circuit

Chapter 5- Simulation & Result of Faulty & Fault free 8 bit DAC: all the tables & graphs we obtained for the faults of main circuit & op amps.

Chapter 6- Conclusion: Conclusion to our thesis

Chapter 2

Digital to Analog Converter & Concerned Faults

2.1 Basic Digital to Analog Converter

In electronics, a digital-to-analog converter (DAC, D/A, D2A or D-to-A) is a function that converts digital data (usually binary) into an analog sign (current, voltage, or electric charge).It is a process in which signals having a few (usually two) defined levels or states (digital) are converted into signals having a theoretically infinite number of states (analog). A DAC works by reading the digital data in a file and attempting to recreate a copy of the original analog signal recorded. A basic block diagram of N-bit DAC is shown in Fig. 2.1 .

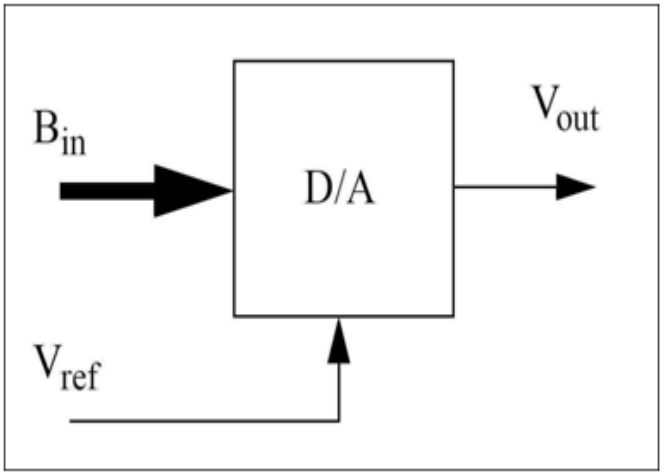


Fig 2.1: Ideal Digital to Analog Converter

Here, an input N-bit digital word (b_1; b_2,...b_N) has a value B_{in} given by the Equation.

$$B_{in} = b_1 2^{i1} + b_2 2^{i2} + \ldots\ldots + b_N\, 2^{iN}$$

As per the Nyquist–Shannon sampling theorem, a digital to analog converter can reconstruct the original signal from the sampled data provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). Digital sampling introduces quantization error that manifests as low-level noise added to the reconstructed signal.

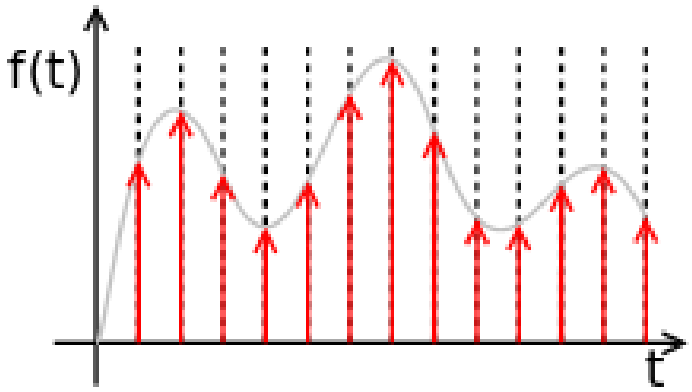


Fig 2.2: Ideally sampled signal

2.2 Digital to Analog Converter Classification

Basically, a digital to analog converter have an op-amp. It can be classified into two types. They are:

2.2.1. Digital to Analog Converter using Binary-Weighted Resistors:

A digital to analog converter using binary-weighted resistors is shown in the fig below. In the circuit, the op-amp is connected in the inverting mode. The op-amp can also be connected in the non-inverting mode. The circuit diagram represents a 4-digit converter. Thus, the number of binary inputs is four.

We know that, a 4-bit converter will have $2^4 = 16$ combinations of output. Thus, a corresponding 16 outputs of analog will also be present for the binary inputs.

Four switches from b0 to b3 are available to simulate the binary inputs: in practice, a 4-bit binary counter such as a 7493 can also be used.

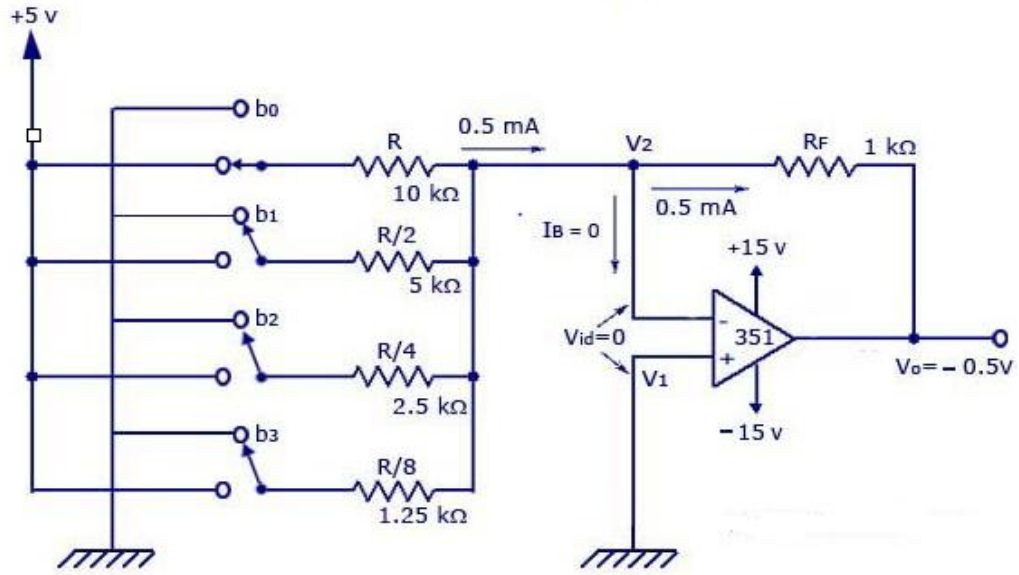


Fig 2.3: Digital to Analog Converter circuit-Binary-Weighted Resistor Method

The graph with the analog outputs versus possible combinations of inputs is shown below.

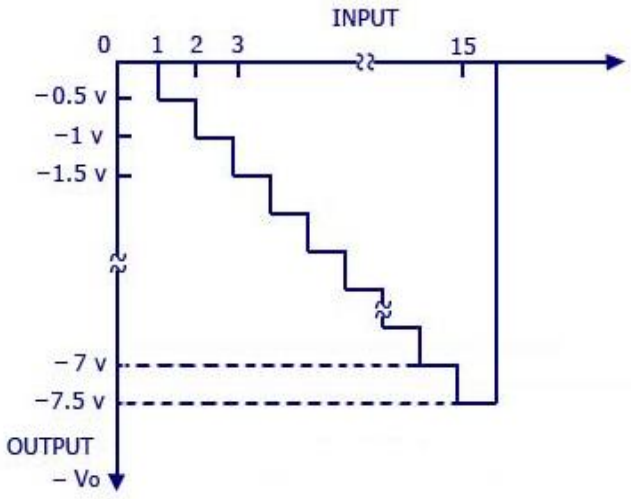


Fig 2.4: Digital to Analog Converter circuit-Binary-Weighted Resistor Method Graph

If the number of inputs (>4) or combinations (>16) is more, the binary-weighted resistors may not be readily available. This is why; R and 2R method is more preferred as it requires only two sets of precision resistance values.

Advantage:

As only one resistor is used per it in the resistor network, thus it is an economical D/A converter.

Limitations:

1. Resistors used in the network have a wide range of values, so it is very difficult to ensure the absolute accuracy and stability of all the resistors.
2. It is very difficult to match the temperature coefficients of all the resistors. This factor is especially important in D/A converters operation over a wide temperature range.
3. When n is so large, the resistance corresponding to LBS can assume a large value, which may be comparable with the input resistance of the amplifier. This leads to erroneous results.
4. As the switches represent finite impedance that are connected in series with the weighted resistors and their magnitudes and variations have to be taken in to account in a D/A converter design.

2.2.2. Digital to Analog Converter with R and 2R Resistors:

A D/A converter with R and 2R resistors is shown in the fig below. As in the binary-weighted resistors method, the binary inputs are simulated by the switches (b0-b3), and the output is proportional to the binary inputs. Binary inputs can be either in the HIGH (+5V) or LOW (0V) state. Let b3 be the most significant bit and thus is connected to the +5V and all the other switchs are connected to the ground.

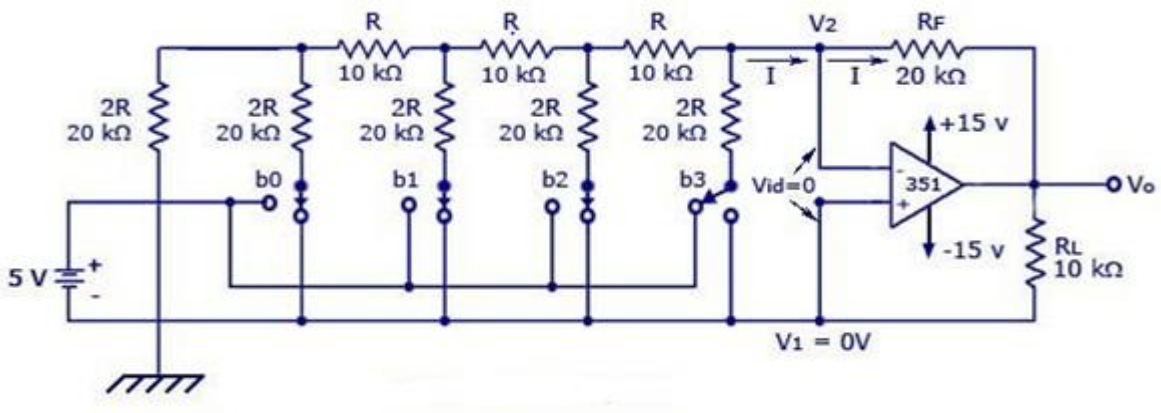


Fig 2.5: Digital to Analog Converter circuit- with R and 2R Resistors

The resultant circuit is shown in fig 2.6.

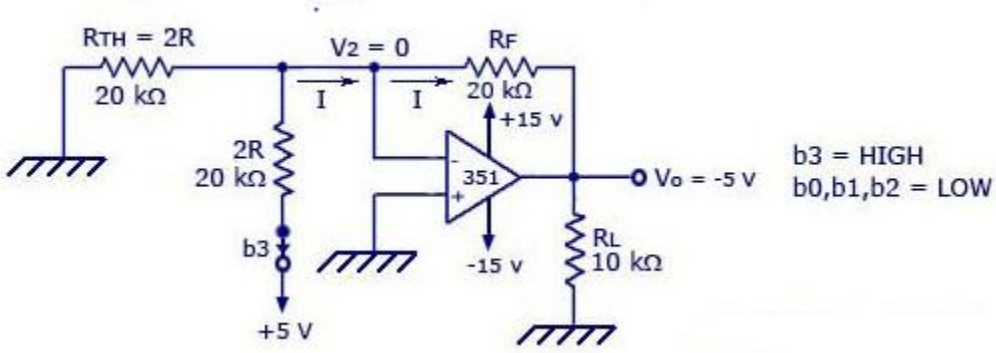


Fig 2.6: Digital to Analog Converter circuit- with R and 2R Resistors

Graph is given below:

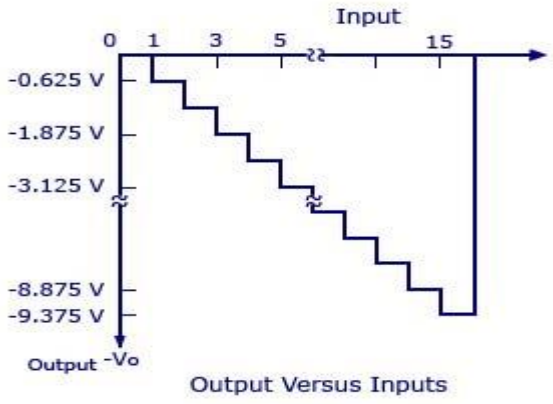


Fig 2.7: Digital to Analog Converter with R and 2R Resistors Graph

Advantage:

1. Only two values of resistors are used; R and 2R.
2. The actual value used for R is relatively less important as long as extremely large values, where stray capacitance enters the picture, are not employs only ratio of resistor values is critical.
3. 2R ladder network are available in monolithic chips. These are laser trimmed to be within 0.01% of the desired ratios.
4. The staircase voltage is more likely to be monotonic as the effect of the MSB resistor is not many times greater than that for LSB resistor.
5. In our thesis, we worked with a Digital to Analog Converter with R and 2R Resistors.

2.3 Fault models of digital to analog converter

A fault is the adjudged or hypothesized cause of a system failure. Fault detection (is there a fault?).and diagnosis (where is the fault?) are key steps in system design and maintenance .The aim of testing at the gate level is to verify that each logic gate in the circuit is functioning properly and the interconnections are good .If only a single stuck-at fault is assumed to be present in the circuit under test, then the problem is to construct a test set that will detect the fault by utilizing only the inputs & outputs of the circuit.

In our thesis, we worked on the single stuck-at fault technique of a basic DA converter.

2.3.1 Defect Model: Stuck-At Faults

The most commonly used fault model is the single stuck-at(SSA) model. It assumes that a fault location can be either be stuck-at 1 or stuck-at 0. If a fault at a wire is stuck-at 0, the logical value at the wire is always 0.in order to detect such a fault a particular fault model used by fault simulators and automatic test pattern generation (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0' and 'X'. For example, an output is tied to a logical 1 state during test generation to assure that a manufacturing defect with that type of behavior can be found with specific test pattern. Stuck open and stuck on faults can be emulated in a resistor or capacitor as illustrated in Fig 2.8.

A MOSFET stuck-on and stuck-off fault can be emulated using the stuck open and stuck on fault model as shown in Fig 2.8. For the fault- free case Rs=1ohm and Rp=100megohm.

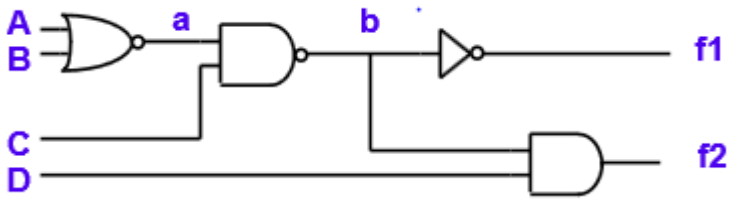


Fig 2.8: Defect Model: Stuck-At Faults

Any input or internal wire in circuit can be stuck-at-1 or stuck-at-0.

Single stuck-at-fault model: In the faulty circuit, a single line wire is S-a-0 or S-a-1

Multiple stuck-at fault models: In the faulty circuit any subset of circuit any subset of wires are S-a-0/ S-a-1(in any combination).

Three properties define a single stuck-at fault:

- Only one line is faulty.
- The faulty line is permanently set to 0 or 1.
- The fault can be at an input or output of a gate.

Advantages:

1. Matches circuit level, easy to use.
2. Moderate number of faults (2n for an n-line circuit).
3. Tests for stuck at faults provide good defect coverage (experiments).

At the switch level, a transistor can be stuck open or stuck short, also referred to as stuck off & stuck on respectively. The stuck at fault model cannot accurately reflect the behavior of stuck-open & stuck short faults in CMOS logic circuits because of the multiple transistors used to construct CMOS logic gates.

2.3.2 Stuck open Faults

Stuck open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incident of fault in the circuit. These faults can be simulated by adding a high resistance in series (Rs=100megohm) with the component to be faulted. We consider a two input CMOS NOR gate shown in the figure. Suppose transistor N_2 is stuck-open. When the input vector AB=01 is applied, output Z should be logic 0,but the stuck open fault causes Z to be isolated from ground(V_{ss}). Because transistor P_2 & N_1 are not conducting at this time, Z keeps it previous state either logic 0 or 1.In order to detect this fault, an ordered sequence of two test vectors AB=00⇒01 is required. For the fault free circuit, the input 00 produces Z=1 & 01 produces Z=0 such that a falling transition at Z appears. but for the faulty circuit, while the test vector 00 produces Z=1,the subsequent test vector 01 will retain Z=1 without a falling transition such that the faulty circuit behaves like a level-sensitive latch. Thus, a stuck open fault in a CMOS combinational circuit requires a sequence of two vectors for detection rather than a single test vector for a stuck at fault.

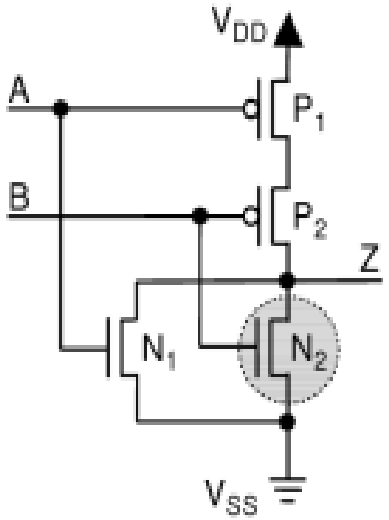


Fig 2.8: 2 input NOR CMOS

2.3.3 Stuck on faults

A stuck on fault, on the other hand, is a stuck on between terminals of the component. This type of fault can be emulated by connecting a small resistor in parallel (Rs=1ohm) with the component. Stuck on fault will produce a conducting path between V_{DD} & V_{ss}. For example, if transistor N_2 is stuck short, there will be a conducting path between V_{DD} & V_{SS} for the test vector 00. This creates a voltage divider at the output node Z where the logic level voltage will be a function of the resistances of the conducting transistors. This voltage may or may not be interrupted as an incorrect logic level by the gate inputs driven by the gate with the transistor fault; however, Stuck on transistor faults may be detected by monitoring the power supply current to detect transistor Stuck on faults is referred to as I_{DDQ} testing.

Chapter 3

Related Work

This chapter describes the relevant literature connected with growth of fault diagnosis of Digital to Analog Converter. The progress in the development of fault testing of DAC has not been studied through published work. Some review of previous work on DA converter & fault detection techniques are reported in this chapter.

3.1 Fault Testing of Benchmark Circuits

A transition fault model for sequential circuits is first proposed. In this fault model, a transition fault is characterized by the fault site, the fault type, and the fault size. The fault type is either slow-to-rise or slow-to-fall. The fault size is specified in units of clock cycles. Fault simulation and test generation algorithms for this fault model are presented. The fault simulation algorithm is a modification of PROOFS, a parallel, differential fault simulation algorithm for stuck faults. Experimental results show that neither a comprehensive functional verification sequence nor a test sequence generated by a sequential circuit test generator for stuck faults produces high fault coverage for transition faults. Deterministic test generation for transition faults is required to raise the coverage to a reasonable level. With the use of a novel fault injection technique, tests for transition faults can be generated by using a stuck fault test generation algorithm with some modifications.

The IEEE 1997 International Test Conference benchmark circuits are a set of analog and mixed-signal circuits provided for the evaluation and performance of different testing approaches. However, the fault models for these benchmark circuits, along with a list of standard faults and range of acceptable component variations were not specified but are a major concern in analog device testing. The set of benchmark circuits consists of some of the circuits taken from ITC'97 benchmark circuits along with others from different sources like Statistical Fault Analyzer (SFA). These circuits are listed in the following table along with their source and the number of components (Rs, Cs, BJTs, and MOSFETs) and number of operational amplifiers that constitute the benchmark circuits which faults have been recognized.

Table3.1: Benchmark Circuits

Name of Circuit	Source	Number of Components
Operational Amplifier #1	ITC'97 [1]	11
Continuous-Time State-Variable Filter	ITC'97 [1]	9 & 3 op amps
Operational Amplifier #2	ITC'97 [1]	10
Leapfrog Filter	ITC'97 [1]	17 & 6 op amps
Differential Amplifier	SFA [5][6]	9
Comparator	SFA [5][6]	3 & 1 op amp
Single Stage Amplifier	SFA [5][6]	6
Elliptical Amplifier	SFA [5][6]	22 & 3 op amps
Low-Pass Filter	Lucent Tech	4 & 1

Experimental results on large benchmark circuits show that high transition fault coverage can be achieved for the partial scan circuits designed using the cycle breaking technique

.

Here is the table shows the comparison of gain detection between the benchmark circuits.

Table3.2: Comparison of gain detection between the benchmark circuits

Circuit	Total no. of possible faults	Gain detect	Gain detect %
Opamp1	28	28	100
Opamp2	20	20	80
comparator	26	21	80.76923077
CTSV Filter	84	67	79.76190476
elliptical amplifier	104	77	74.03846154
leap frog filter	154	116	75.32467532
low pass filter	28	24	85.71428571

Chapter 4

Digital-to-Analog Converter ITC'97

In this thesis, an 8 bit digital to analog converter with two stage CMOS operational amplifier is used. The components used in the operational amplifier are shown in the following table.

Table 4.1: Components of Operational amplifier used in digital-to-analog converter

Component	Nominal Values
Operational amplifier:1(CMOS 2-stage)	CMOS-2-OA
Resistors	R, R1-R16, R=40KΩ , 2R=80KΩ
Capacitors	C=15pF

Table 4.2: Fault Table of DA Converter

Hard Fault Table	Fault	No. of Faults
CMOS-2-OA	Op amp faults	1x36=36
M1-M16	Stuck open/stuck on	2x16=32
R, R1-R16	Stuck open/stuck on	2x17=34
C	Stuck open/stuck on	1x2=2
Total no. of faults		104

4.1 Operation of 8 Bit Digital to Analog Converter

Operation of the 8 bit R-2R ladder is straight forward. First, it can be shown, by starting from the right & working toward the left, that the resistance to the right of each ladder node, is equal to 2R. Thus the current flowing to the right, away from each node, is equal to the current flowing downward to ground and twice that current flow into the node from the left side.

Fig 5.1 shows the basic arrangement of 8 bit digital to analog converter. The circuit consist of a reference voltage V_{ref} , the p-mos and n-mos are controlled by the 8 bit digital input word D,

$$D = \frac{b1}{2^1} + \frac{b2}{2^2} + \cdots + \frac{b_8}{2^8}$$

Where b_1, b_2, and so on are bit coefficients that are either 1 or 0. Note that the bit b_8 is the least significant bit (LSB) and b_1 is the most significant bit (MSB). In the circuit in fig 5.1, b_1 controls M1 and M2, and b_2 controls M3 and M4 and so on. When b_1 is 0, p-mos M1 conducts and when b_1 is 1 n-mos M2 conducts.

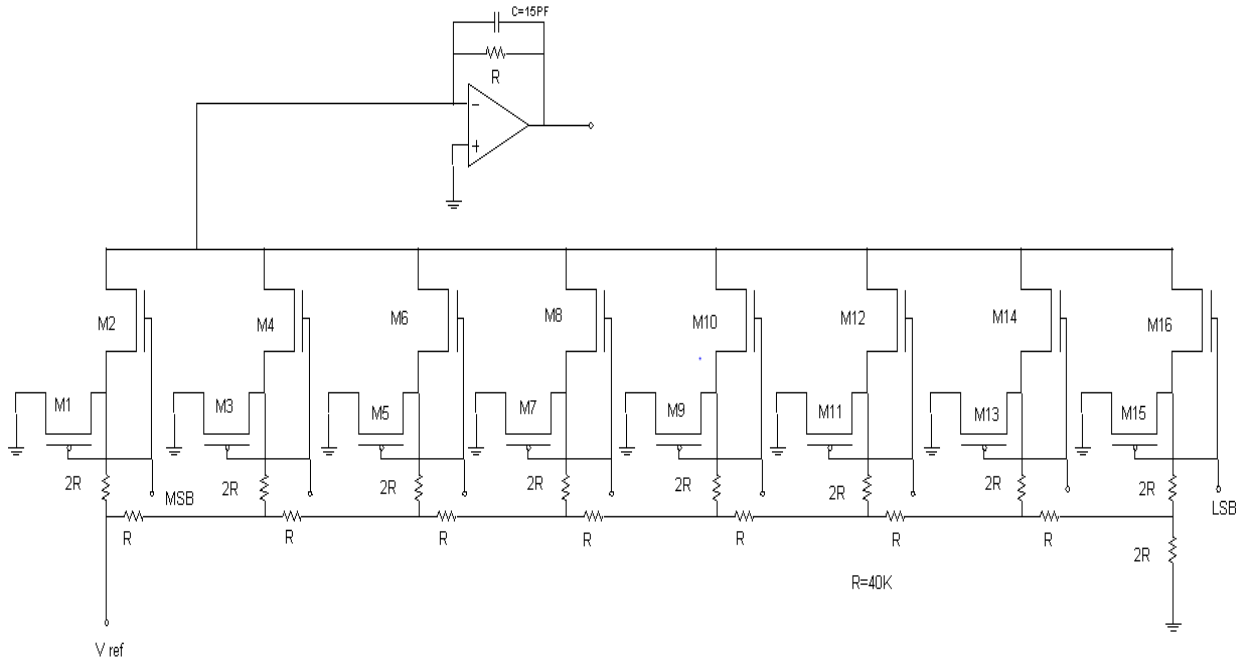


Fig 4.1: 8 Bit digital to analog converter

Since all p-mos are connected with ground and all n-mos are connected with virtual ground of an output summing op amp, the current through each resistor remain constant. It follows that,

$$I = 2\,I_1 = 4\,I_2 = \ldots\ldots\ldots = 2^N\,I_N$$

Where I_1 to I_N are binary weighted constant current which are switched between ground and virtual ground of an output summing op amp. I_1 corresponds to the MSB and I_N corresponding to the LSB of the DAC.

Thus, the output current will be given by,

$$i_0 = \frac{V_{ref}}{R} D$$

Chapter 5

Simulation & Result of Faulty & Fault free 8 bit Digital to Analog Converter

For our analysis, we have taken 8 bit digital to analog converter. We mentioned the recognized 104 stuck-at faults, 52 of them are stuck open and rests 52 of them are stuck on. The main circuit faults & faults in the operational amplifiers are presented here sequentially.

5.1 Main Circuit Faults

With the purpose of simplification, the explanation of the graph & table, we have considered 3 bit DAC.

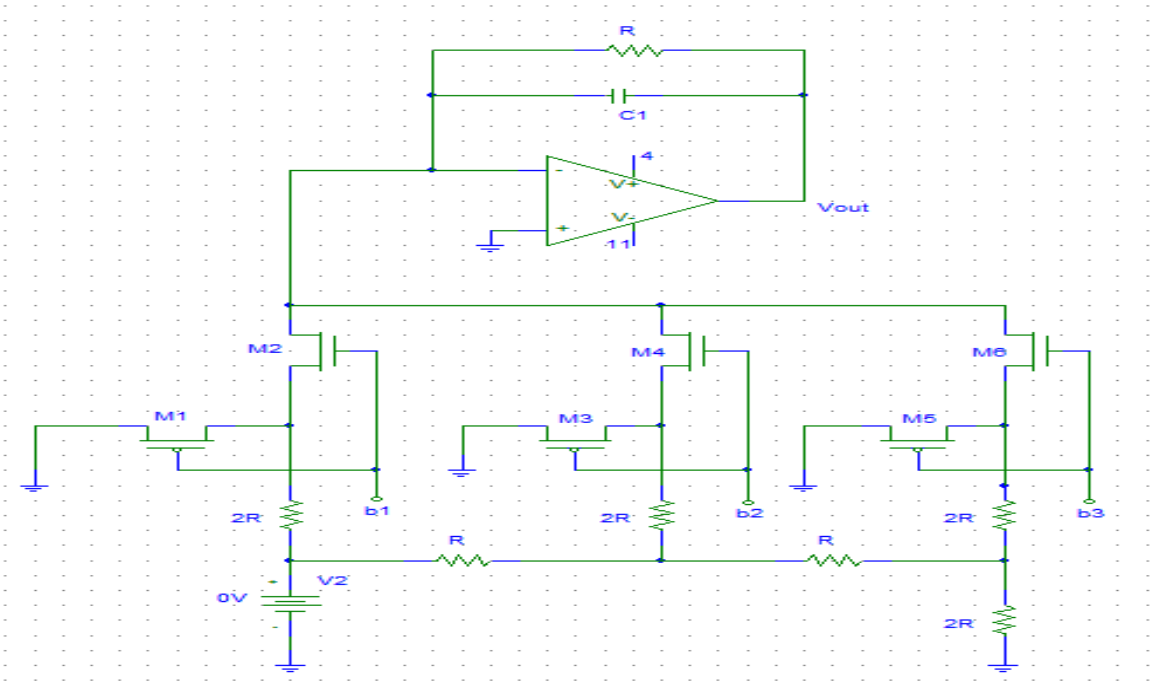


Fig 5.1: 3 Bit Digital to Analog Converter

Table 5.1**:** Pmos faults (stuck open) in DAC

Fault Name	RMS error, Gain(dB)
M1stuck open	0.0011352
M3 stuck open	0.0017996
M5 stuck open	0.00089551
M7 stuck open	0.0009618
M9 stuck open	0.0025872
M11stuck open	0.016146
M13 stuck open	0.0087776
M15 stuck open	0.00014989

Comment:

Assuming that, M1 is stuck open. Taking input bit 110, M2 and M4 will be connected with the virtual ground and M5 will be connected with the ground for both faulty and fault free circuit. The equivalent circuit will be,

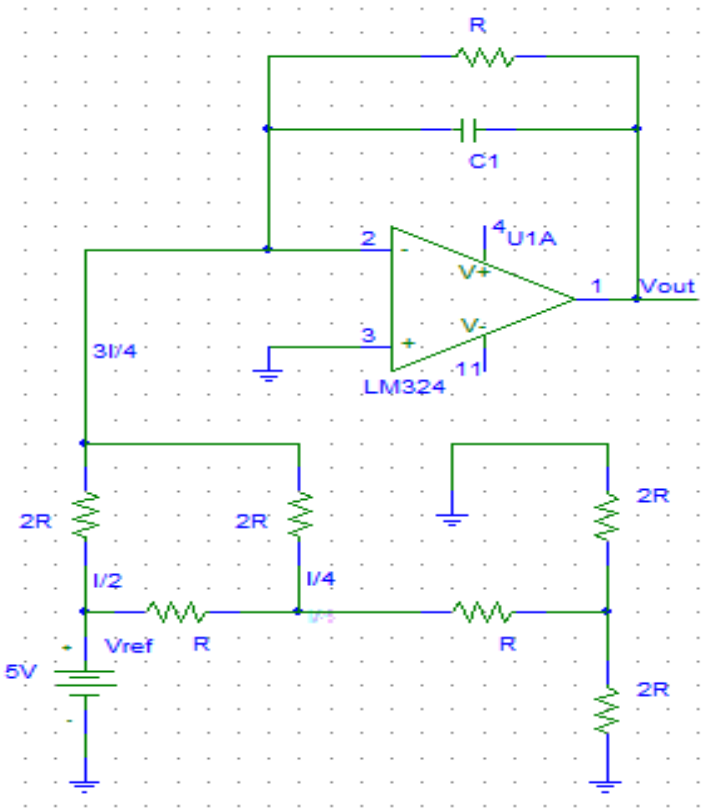


Fig 5.2: faulty circuit when M1 is stuck open

The input current of op-amp for the faulty circuit is $\frac{3I}{4}$.

Similarly for the fault free circuit; we get the same input current of op-amp. As the current is same, we will get the same output voltage and gain for both faulty and fault free circuit. From the bellow graph, we can see that the gain error is negligible.

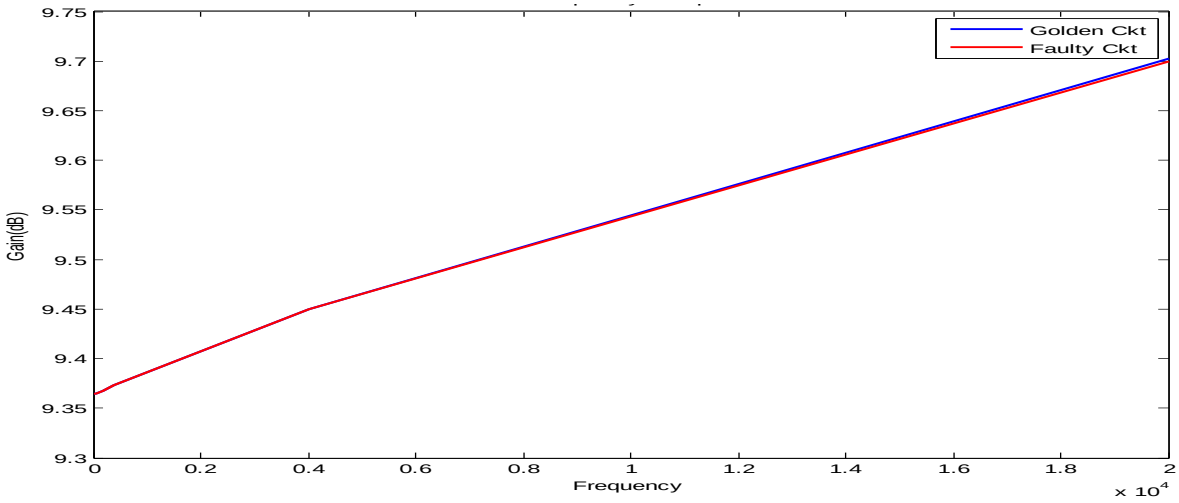


Fig 5.3: Gain Vs Frequency comparison between golden circuit and faulty circuit for M1 stuck open

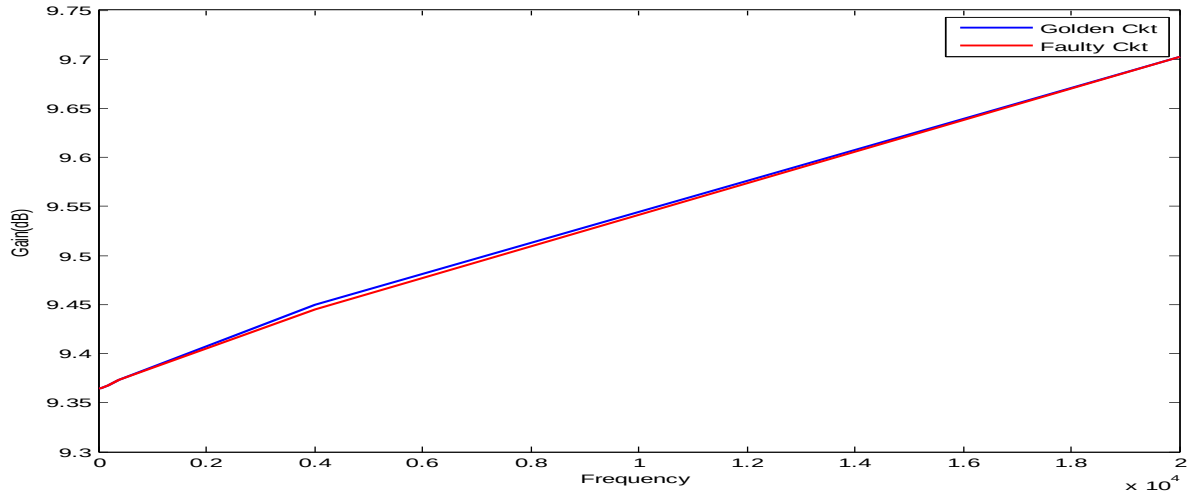


Fig 5.4: Gain Vs Frequency comparison between golden circuit and faulty circuit for M3 stuck open

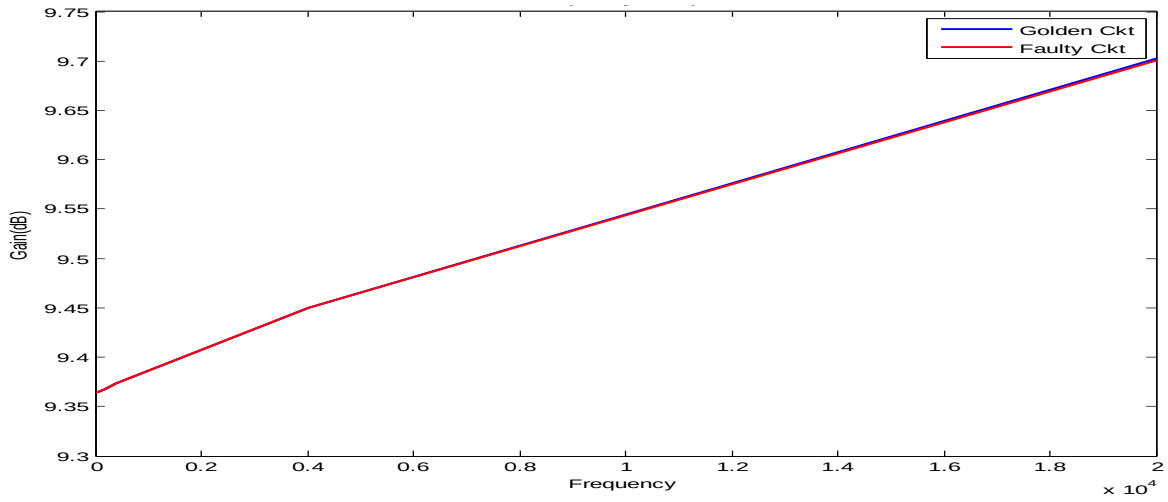


Fig 5.5: Gain Vs Frequency comparison between golden circuit and faulty circuit for M5 stuck open

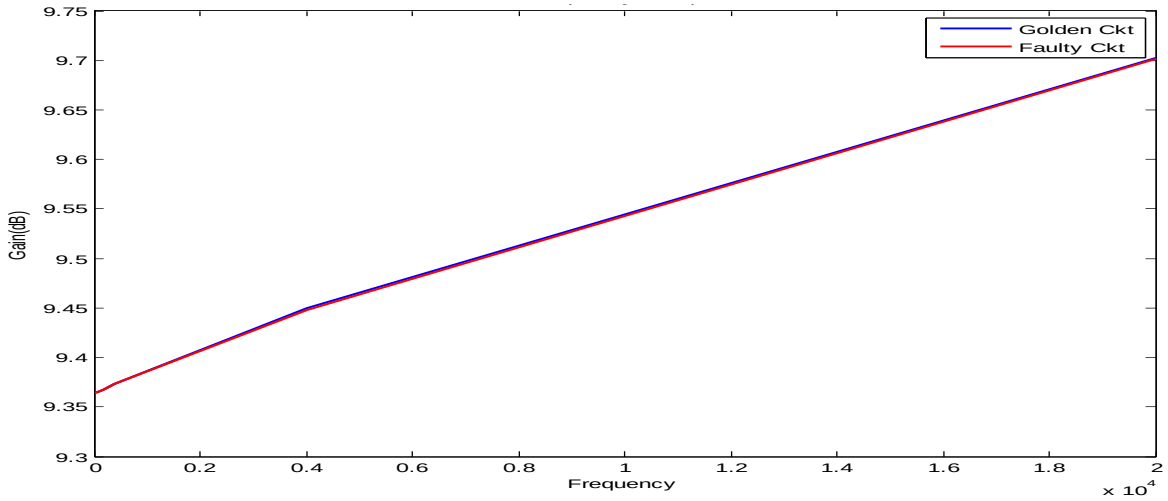


Fig 5.6: Gain Vs Frequency comparison between golden circuit and faulty circuit for M7 stuck open

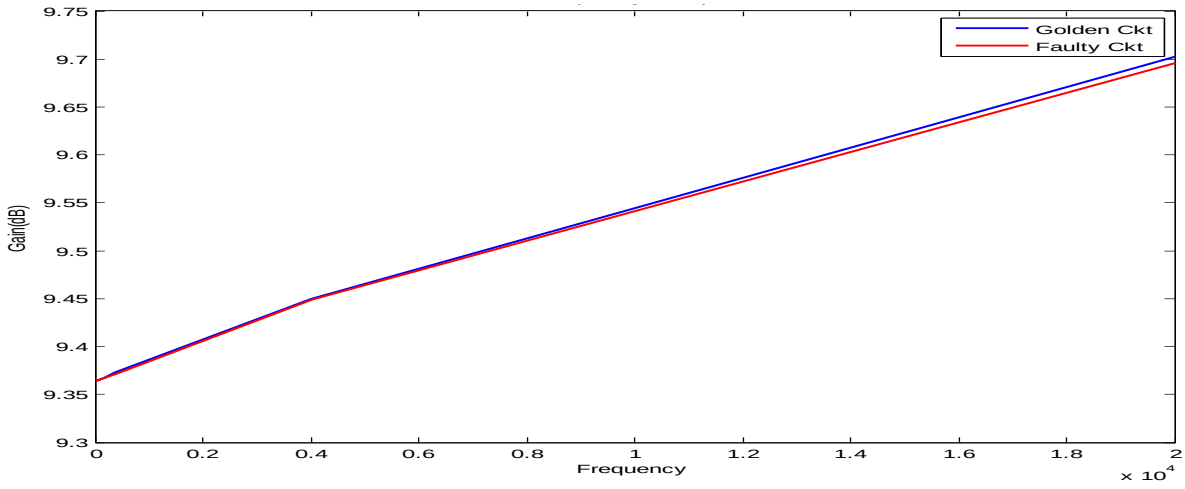


Fig 5.7: Gain Vs Frequency comparison between golden circuit and faulty circuit for M9 stuck open

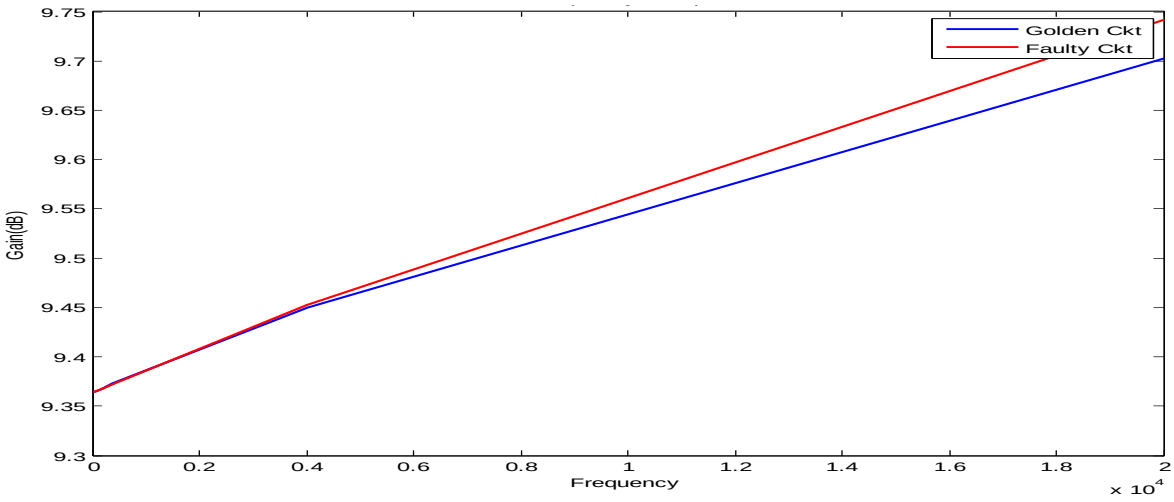


Fig 5.8: Gain Vs Frequency comparison between golden circuit and faulty circuit for M11 stuck open

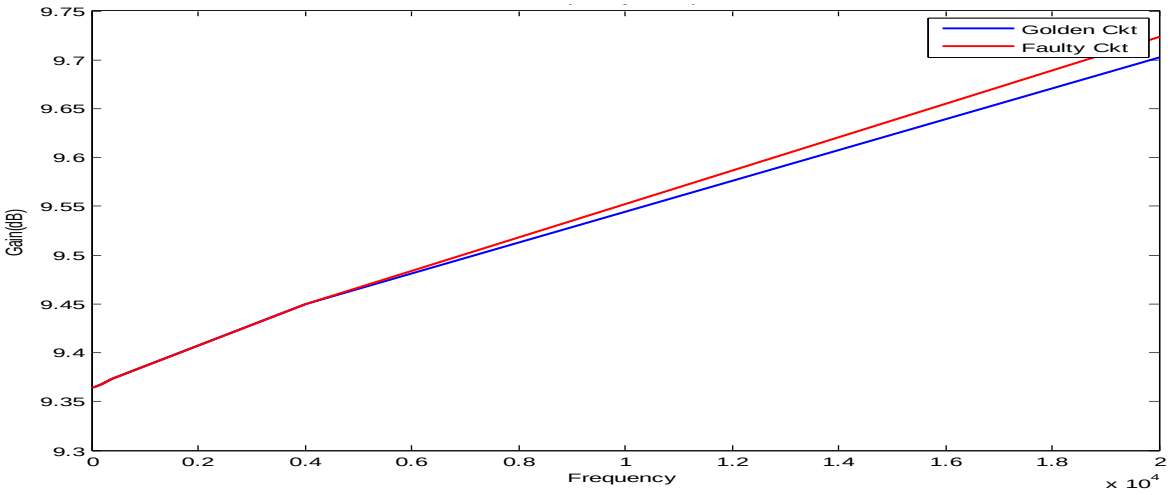


Fig 5.9: Gain Vs Frequency comparison between golden circuit and faulty circuit for M13 stuck open

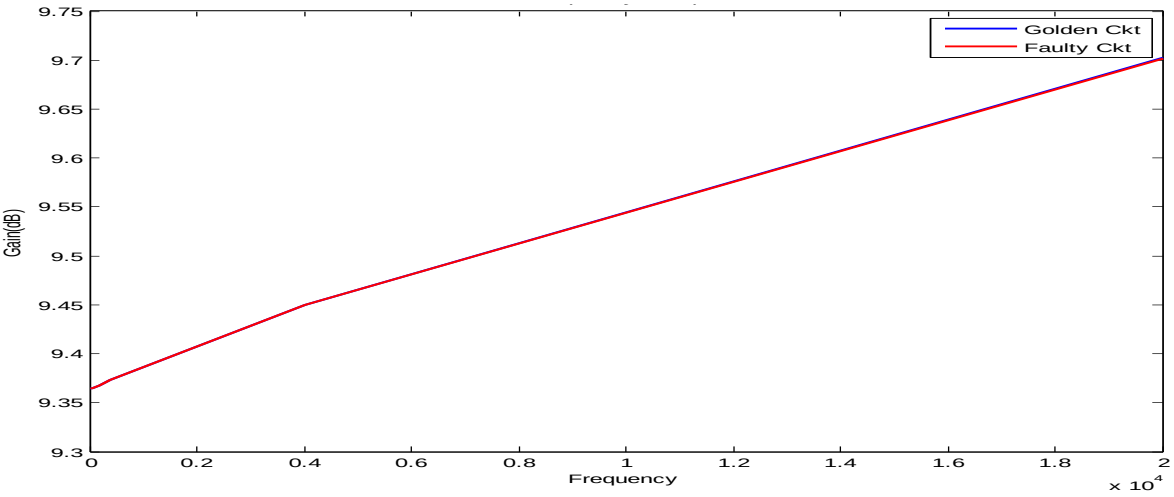


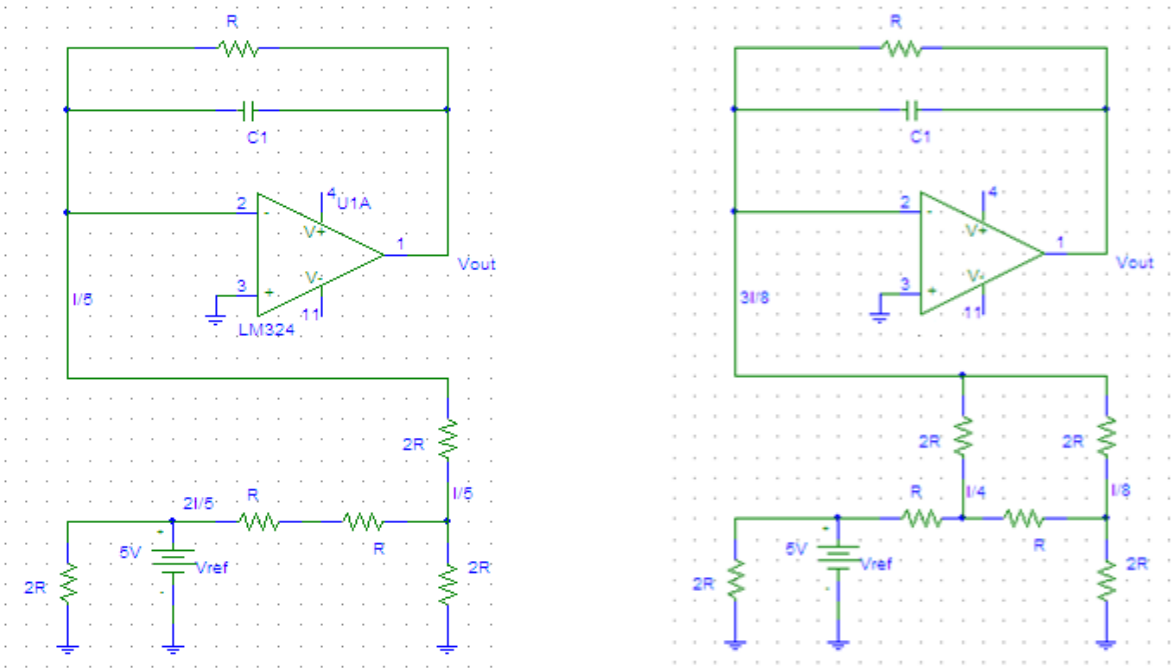
Fig 5.10: Gain Vs Frequency comparison between golden circuit and faulty circuit for M15 stuck open

Table 5.2: Nmos faults(stuck open) in DAC

Fault Name	RMS Error Gain(dB)
M2 stuck open	2.6001
M4 stuck open	0.24921
M6 stuck open	0.41807
M8 stuck open	0.4875
M10 stuck open	0.30599
M12stuck open	0.075207
M14 stuck open	0.63105
M16 stuck open	2.1976

Comment:

Assuming that, M4 is stuck open. Taking input bit 011. As M4 is stuck opened in faulty circuit 2R resistance connected with M4 will be eliminated but in fault free circuit it will be connected with virtual ground. The equivalent circuit will be,



(a) (b)

Fig 5.11(a): faulty circuit when M4 is stuck open;

(b): fault free circuit

The input current of op-amp for the faulty circuit is $\frac{I}{5}$.

The input current of op-amp for the fault free circuit is $\frac{3I}{8}$.

Here, we can see that, the current of fault free circuit is greater than faulty circuit. So both output voltage & gain of fault free circuit will be greater than faulty circuit, which is shown in the following graph:

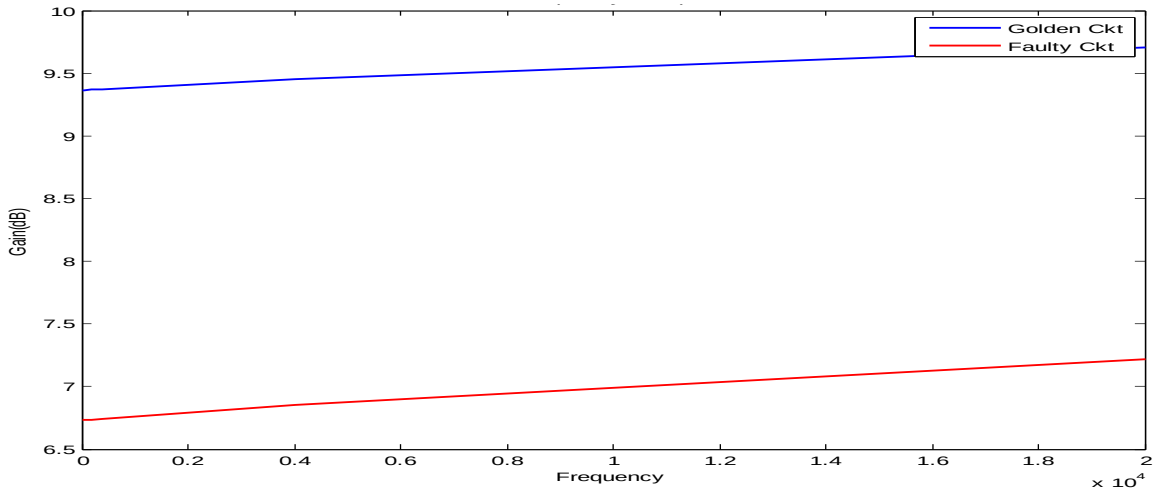


Fig5.12: Gain Vs Frequency comparison between golden circuit and faulty circuit for M2 stuck open

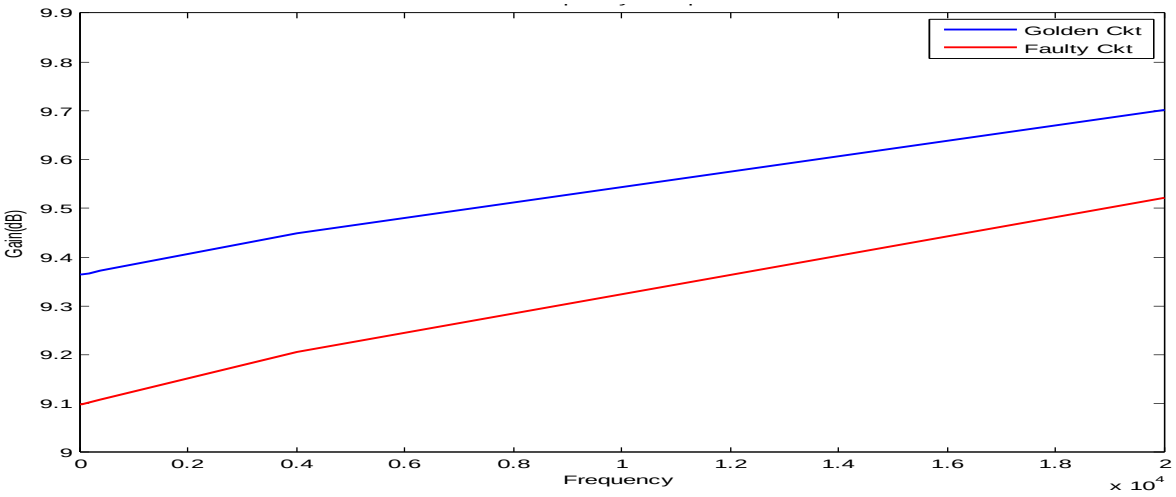


Fig 5.13: Gain Vs Frequency comparison between golden circuit and faulty circuit for M4 stuck open

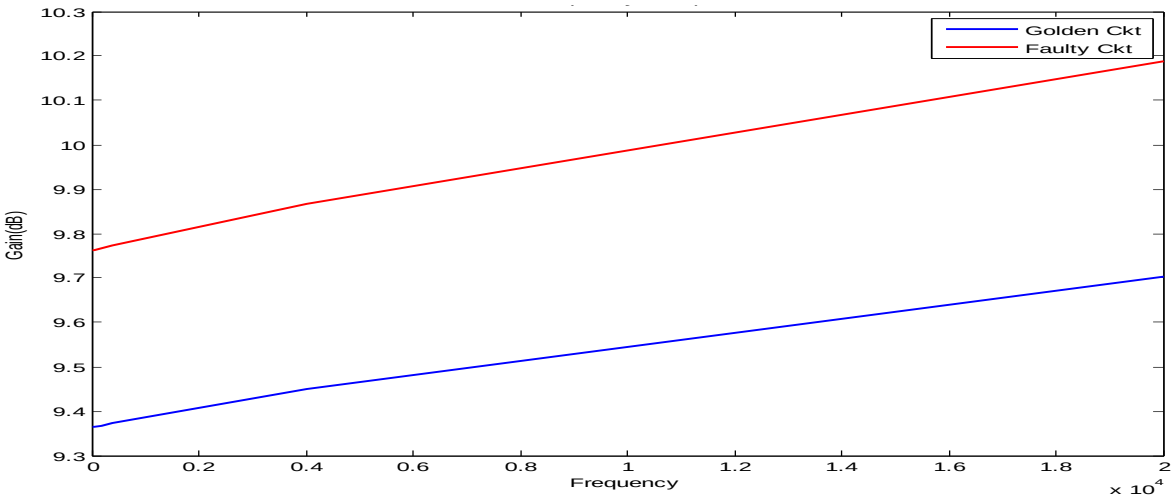


Fig5.14: Gain Vs Frequency comparison between golden circuit and faulty circuit for M6 stuck open

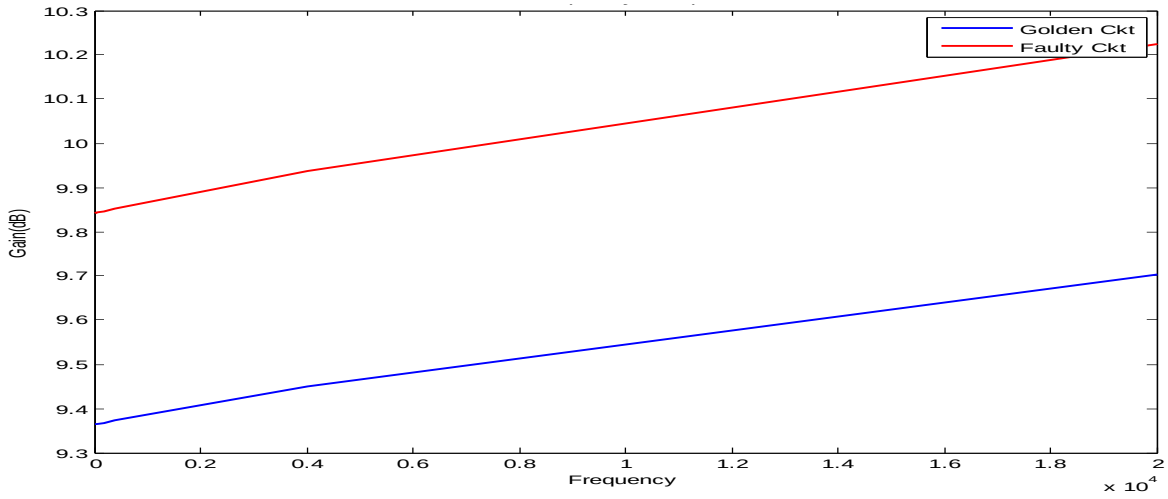


Fig 5.15: Gain Vs Frequency comparison between golden circuit and faulty circuit for M8 stuck open

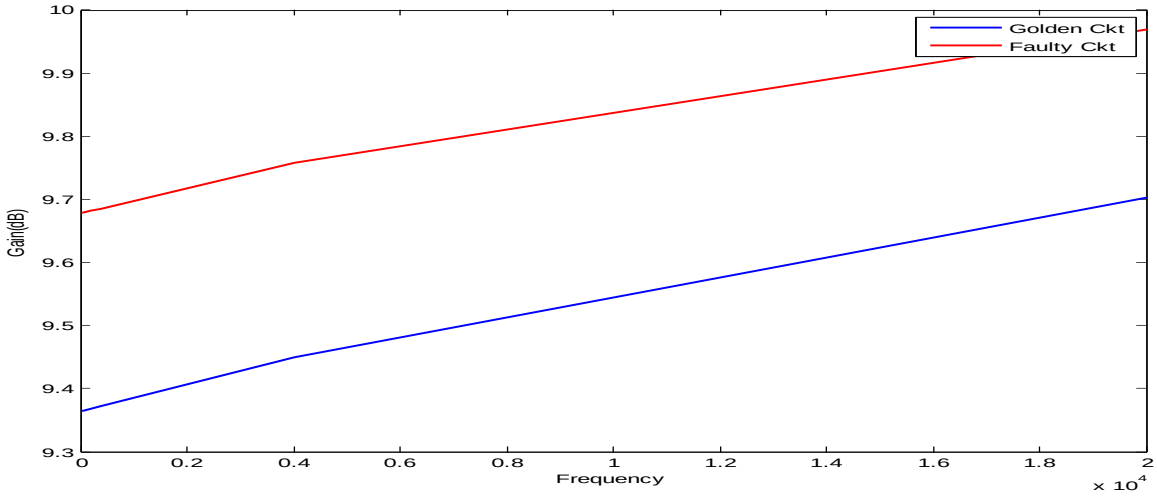


Fig 5.16: Gain Vs Frequency comparison between golden circuit and faulty circuit for M10 stuck open

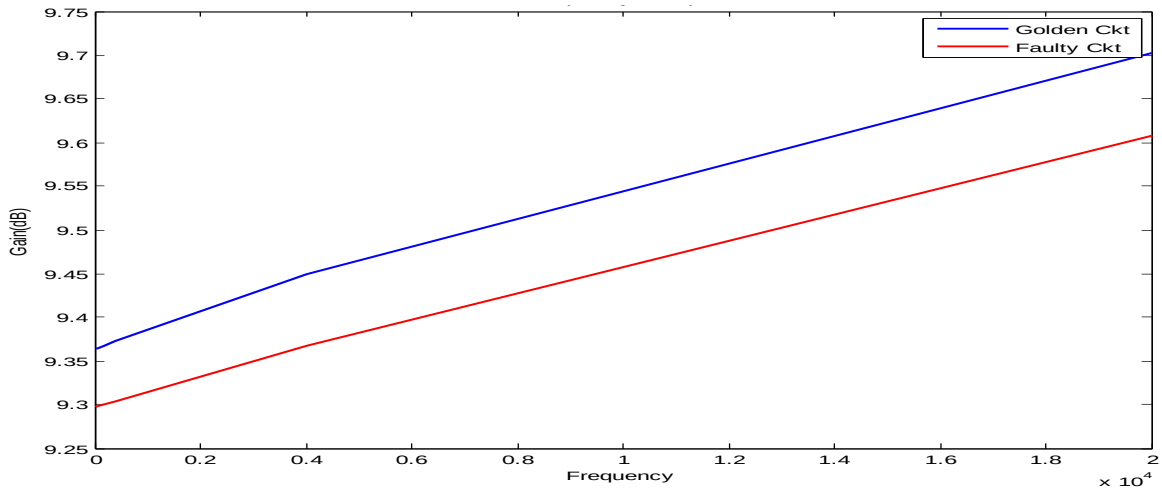


Fig 5.17: Gain Vs Frequency comparison between golden circuit and faulty circuit for M12 stuck open

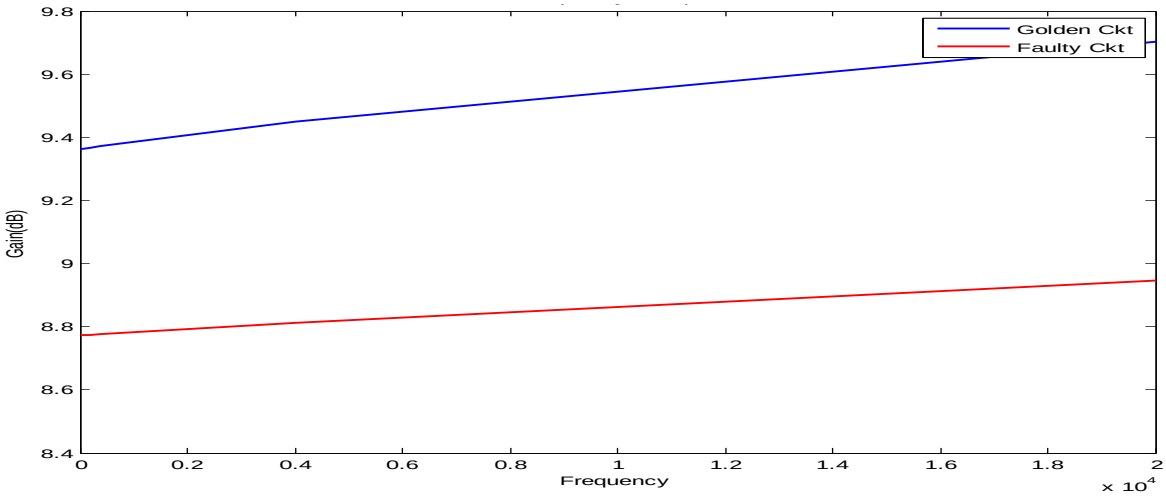


Fig 5.18: Gain Vs Frequency comparison between golden circuit and faulty circuit for M14 stuck open

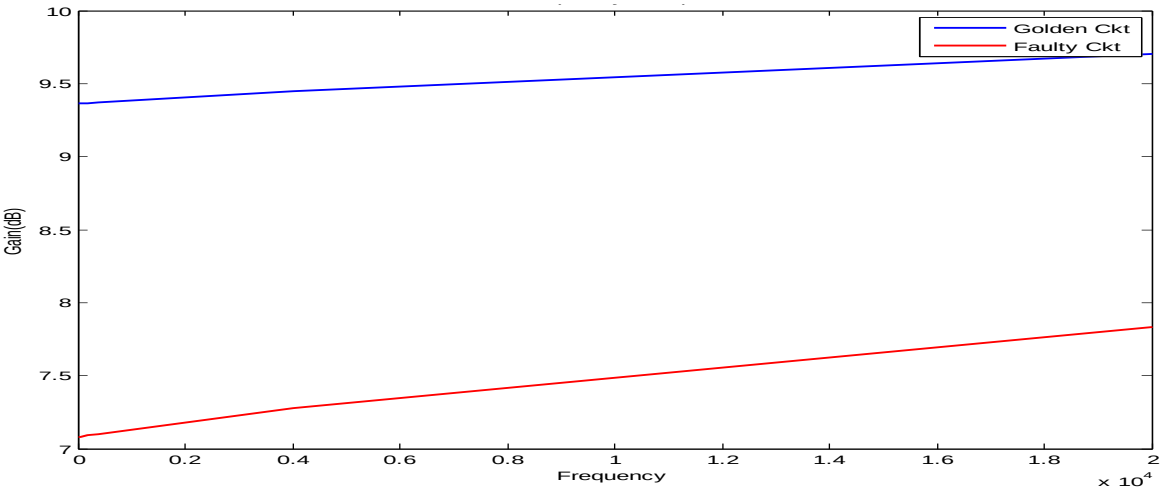


Fig 5.19: Gain Vs Frequency comparison between golden circuit and faulty circuit for M16 stuck open

Table 5.3: Pmos faults(stuck on) in DAC

Fault Name	RMS error,Gain(dB)
M1stuck on	2.6207
M3 stuck on	1.5787
M5 stuck on	1.2216
M7 stuck on	1.2857
M9 stuck on	1.7474
M11 stuck on	2.4029
M13 stuck on	3.5613
M15stuck on	8.1128

Comment:

Assuming that, M3 is stuck on. Taking input bit 011. As M3 is stuck oned, 2R resistance connected with M3 will be connected with ground instead virtual ground of the am-opm in faulty circuit. The equivalent circuit will be,

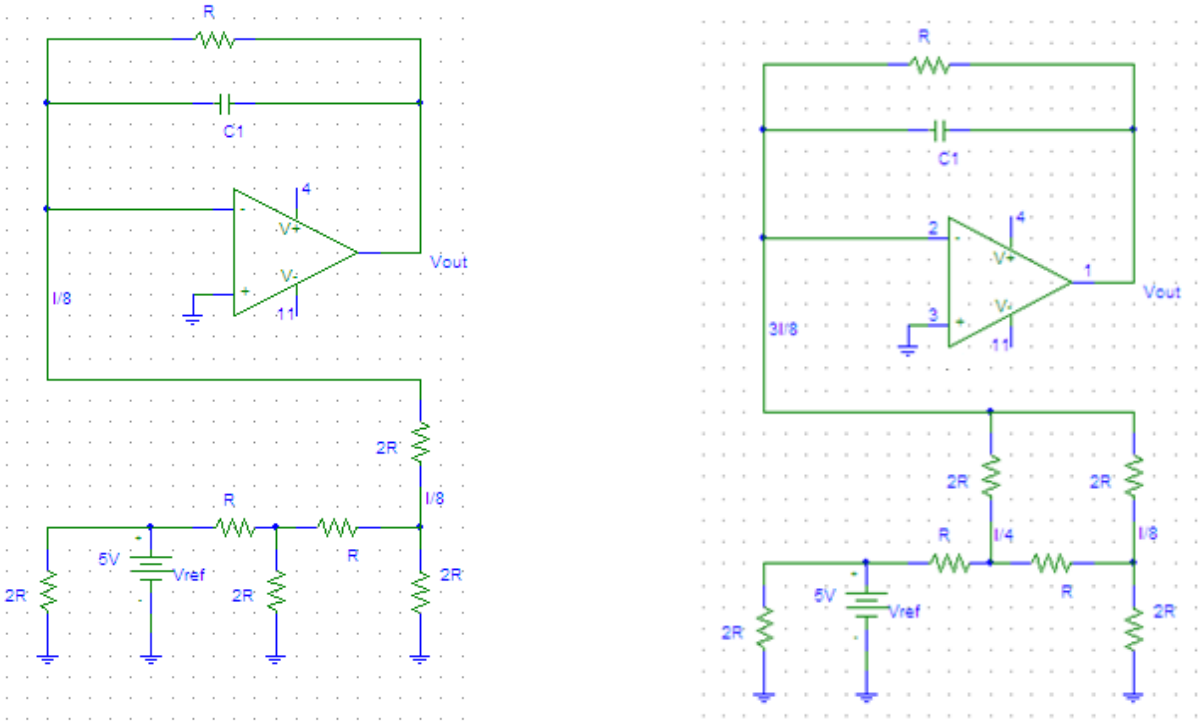


Fig 5.20(a): faulty circuit when M3 is stuck on; (b): fault free circuit

The input current of op-amp for the faulty circuit is $\frac{I}{8}$

The input current of op-amp for the fault free circuit is $\frac{3I}{8}$

Here, we can see that, the current of fault free circuit is greater than faulty circuit. So both output voltage & gain of fault free circuit will be greater than faulty circuit, which is shown in the following graph:

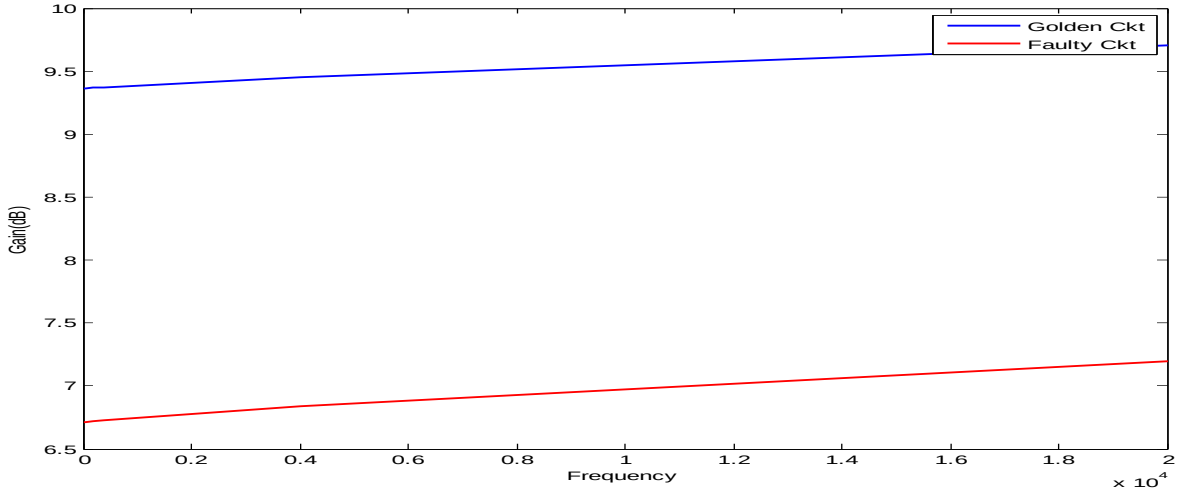


Fig 5.21: Gain Vs Frequency comparison between golden circuit and faulty circuit for M1 stuck on

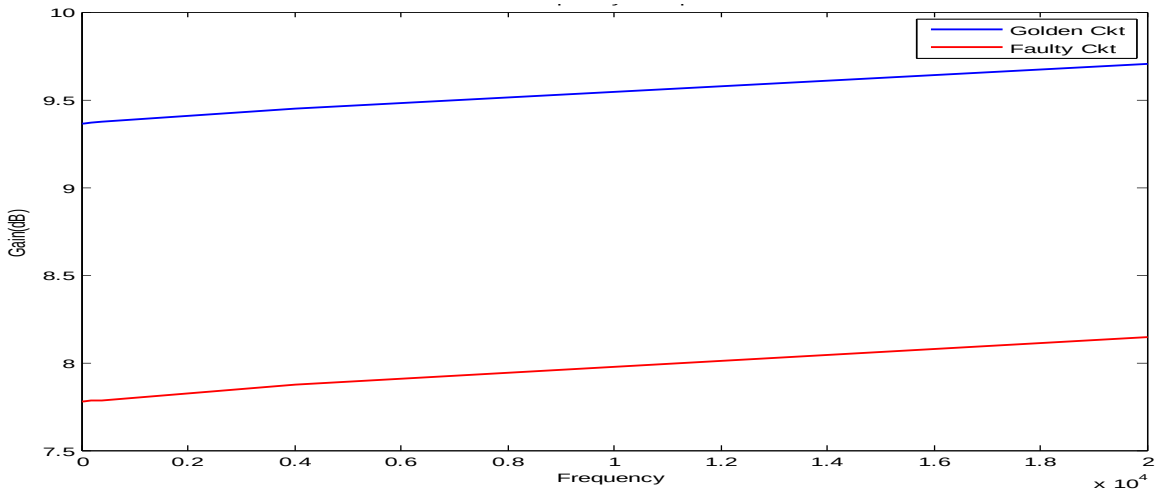


Fig 5.22: Gain Vs Frequency comparison between golden circuit and faulty circuit for M3 stuck on

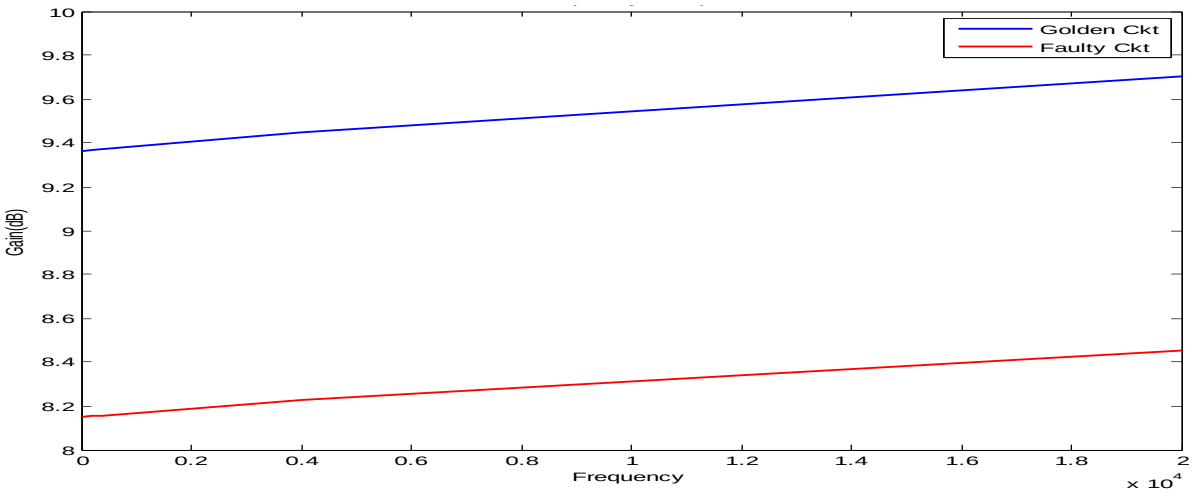


Fig 5.23: Gain Vs Frequency comparison between golden circuit and faulty circuit for M5 stuck on

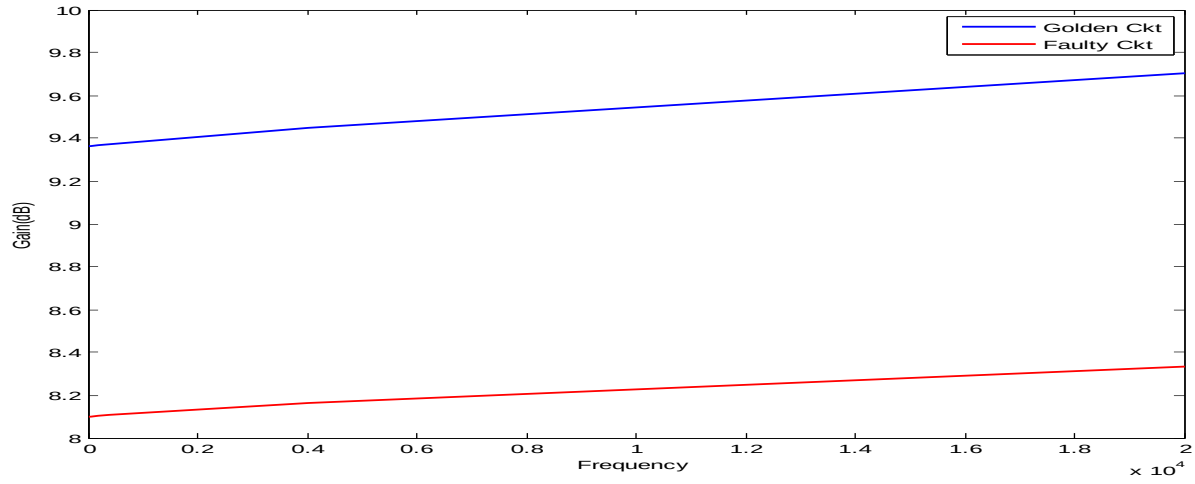


Fig 5.24: Gain Vs Frequency comparison between golden circuit and faulty circuit for M7 stuck on

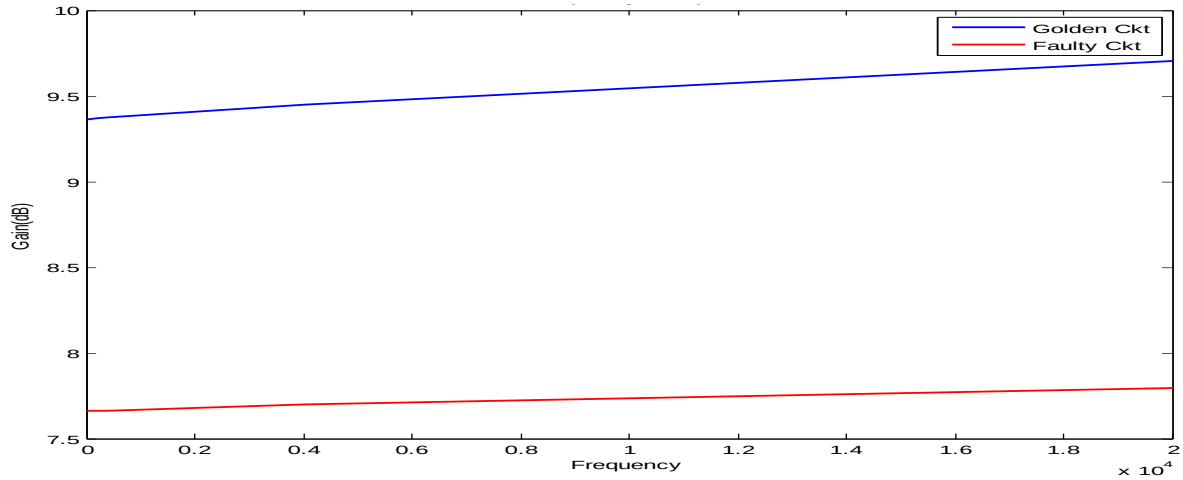


Fig 5.25: Gain Vs Frequency comparison between golden circuit and faulty circuit for M9 stuck on

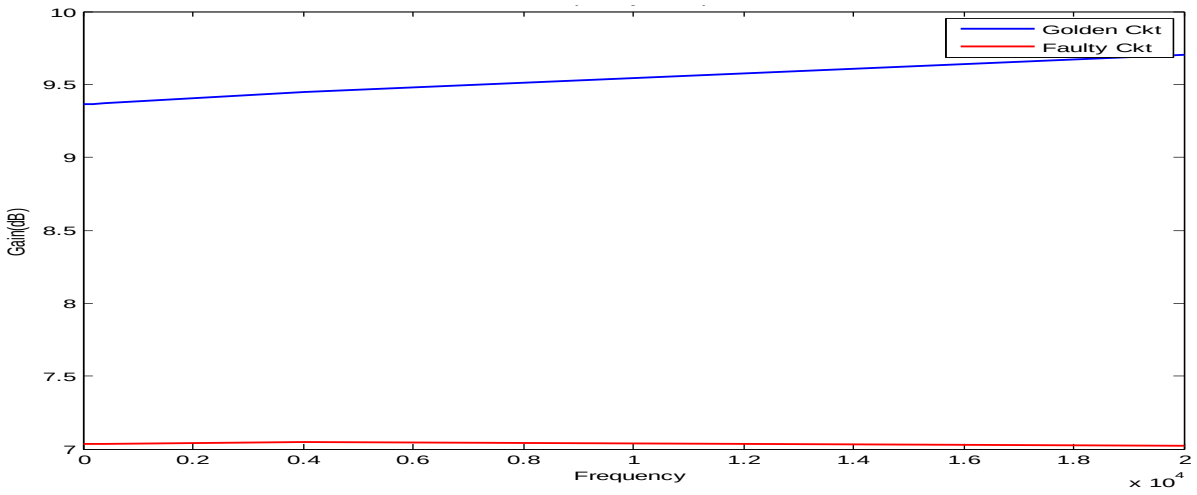


Fig 5.26: Gain Vs Frequency comparison between golden circuit and faulty circuit for M11 stuck on

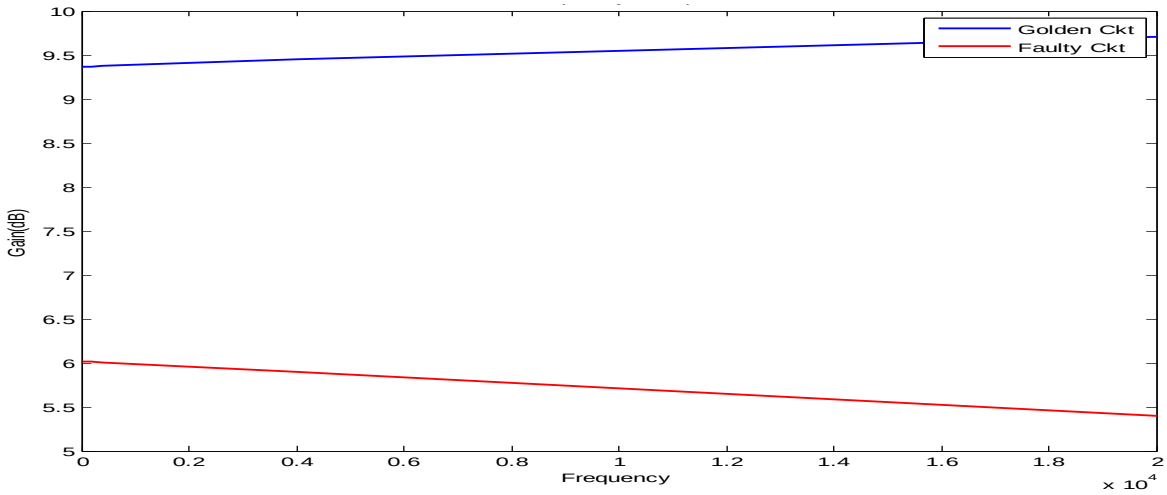


Fig 5.27: Gain Vs Frequency comparison between golden circuit and faulty circuit for M13 stuck on

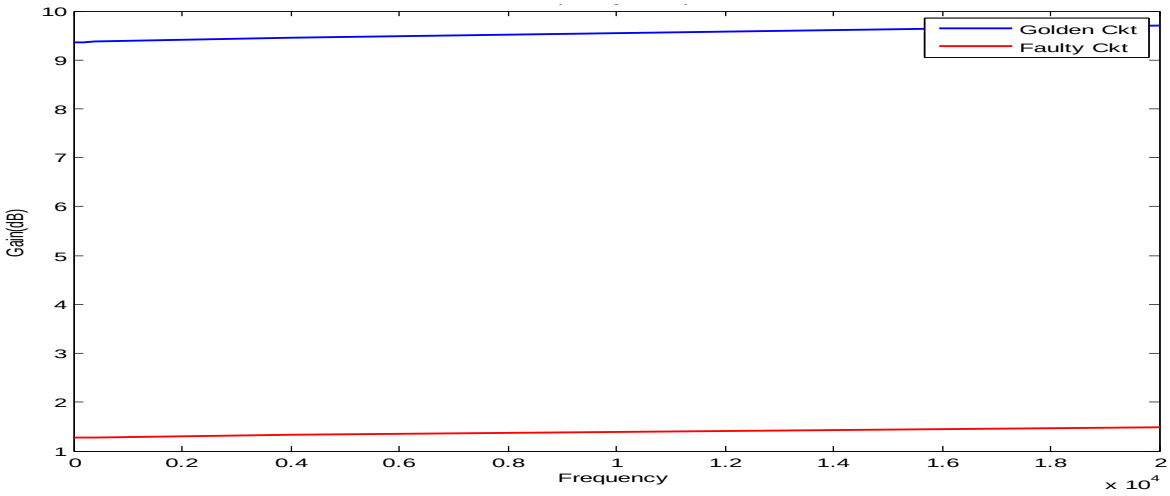


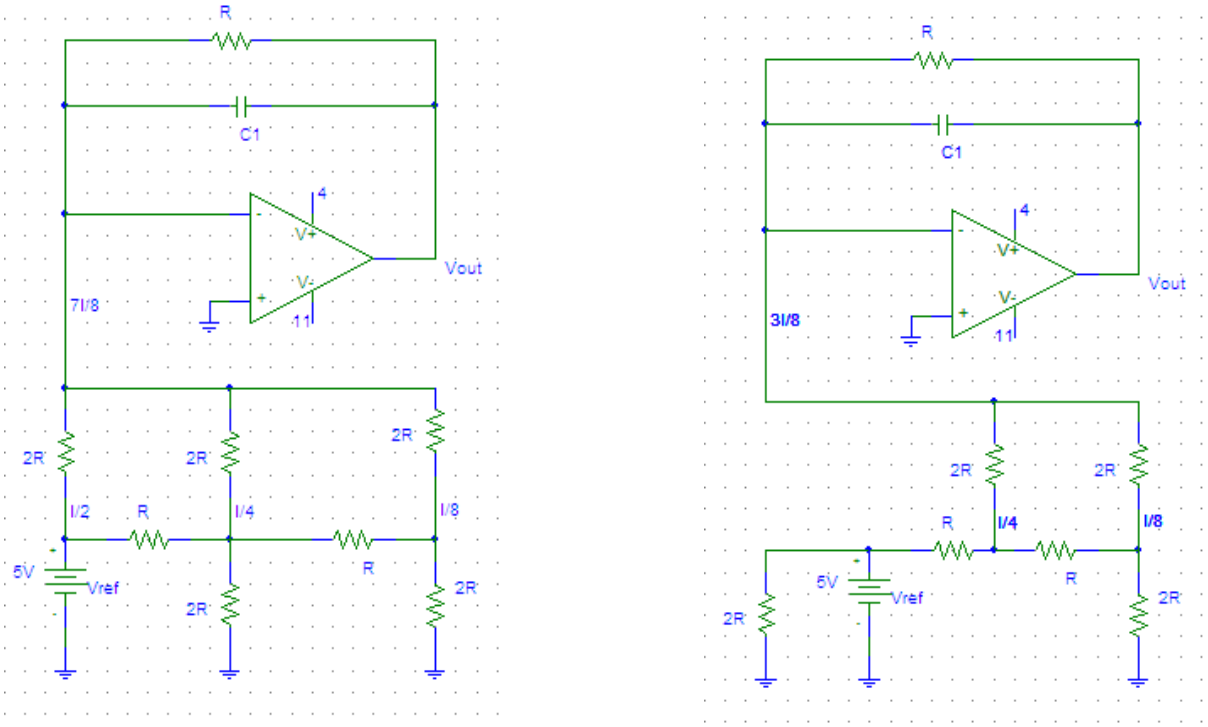
Fig 5.28: Gain Vs Frequency comparison between golden circuit and faulty circuit for M15 stuck on

Table 5.4: Nmos faults(stuck on) in DAC

Fault Name	RMS error, Gain(dB)
M2 stuck on	19.9954
M4 stuck on	15.0909
M6 stuck on	11.0337
M8 stuck on	7.8275
M10 stuck on	5.2082
M12 stuck on	3.1156
M14 stuck on	1.6319
M16 stuck on	0.028451

Comment:

Assuming that, M2 is stuck on. Taking input bit 011. As M2 is stuck oned, 2R resistance connected with M2 will be connected with virtual ground of the op-amp instead of ground. The equivalent circuit will be,



(a) (b)

Fig 5.29 (a): faulty circuit when M2 is stuck on; (b): fault free circuit

The input current of op-amp for the faulty circuit is $\frac{7I}{8}$

The input current of op-amp for the fault free circuit is $\frac{3I}{8}$

Here, we can see that, the current of faulty circuit is greater than fault free circuit. So both output voltage & gain of faulty circuit will be greater than fault free circuit, which is shown in the following graph:

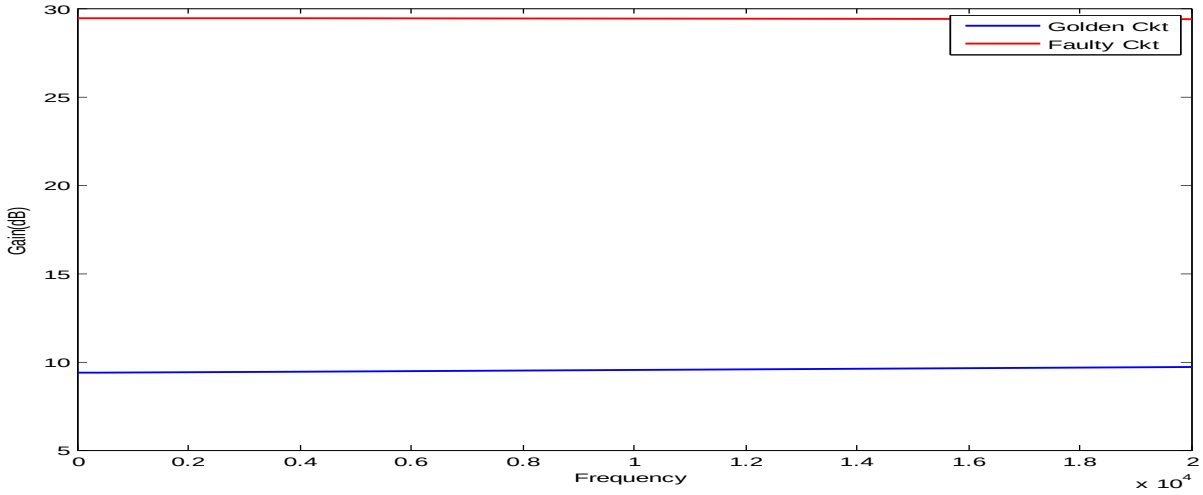


Fig 5.30: Gain Vs Frequency comparison between golden circuit and faulty circuit for M2 stuck on

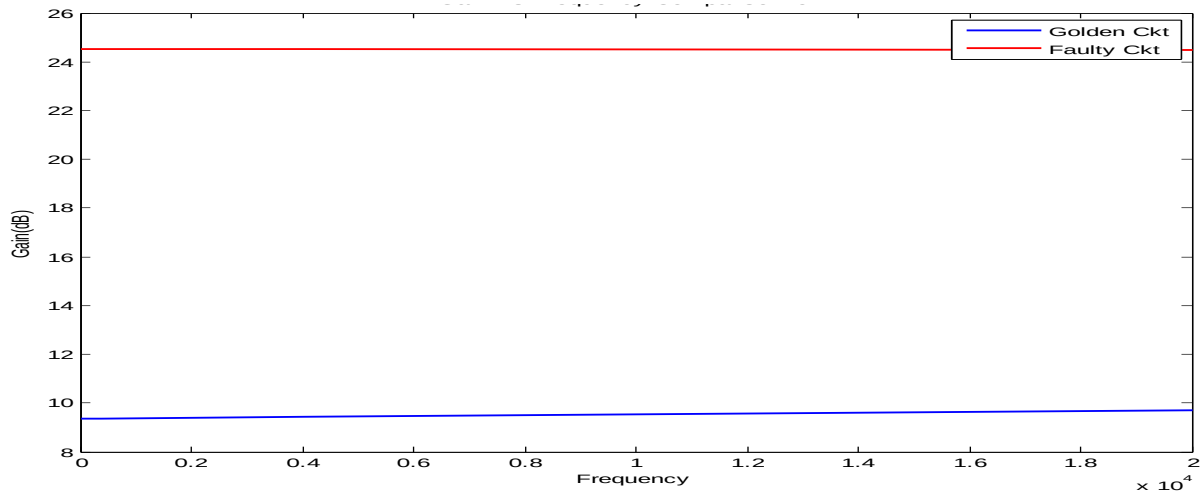


Fig 5.31: Gain Vs Frequency comparison between golden circuit and faulty circuit for M4 stuck on

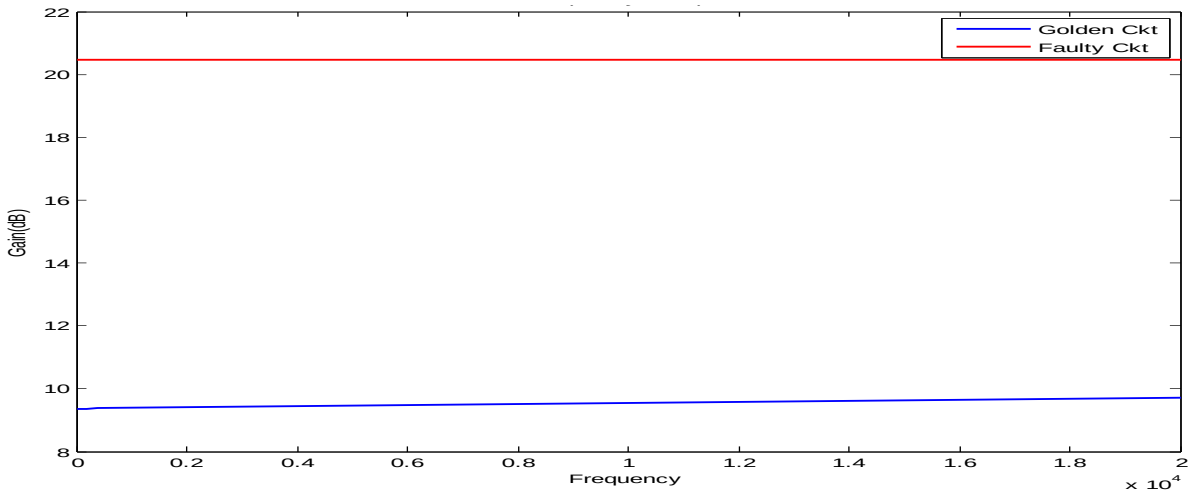


Fig 5.32: Gain Vs Frequency comparison between golden circuit and faulty circuit for M6 stuck on

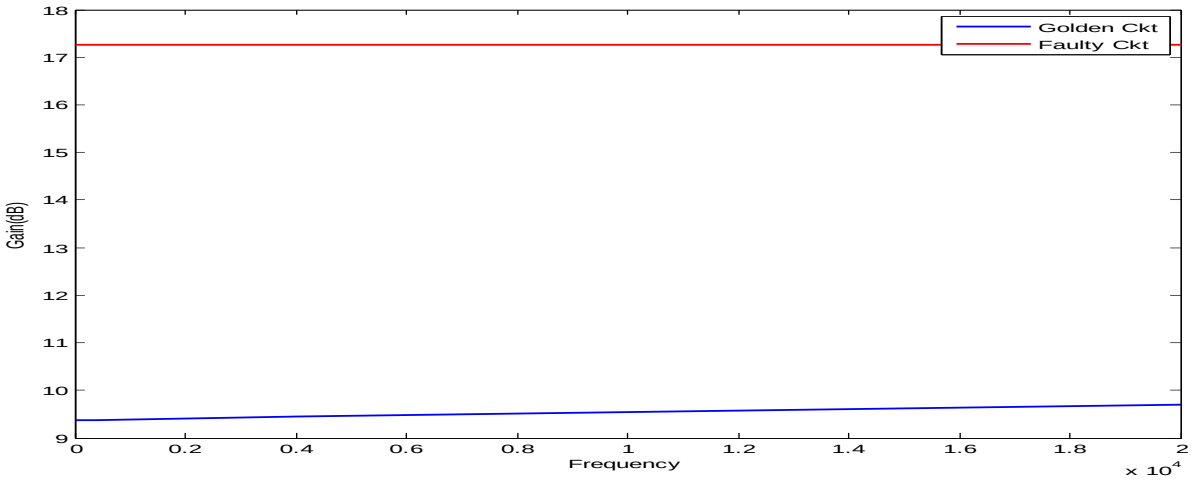


Fig 5.33: Gain Vs Frequency comparison between golden circuit and faulty circuit for M8 stuck on

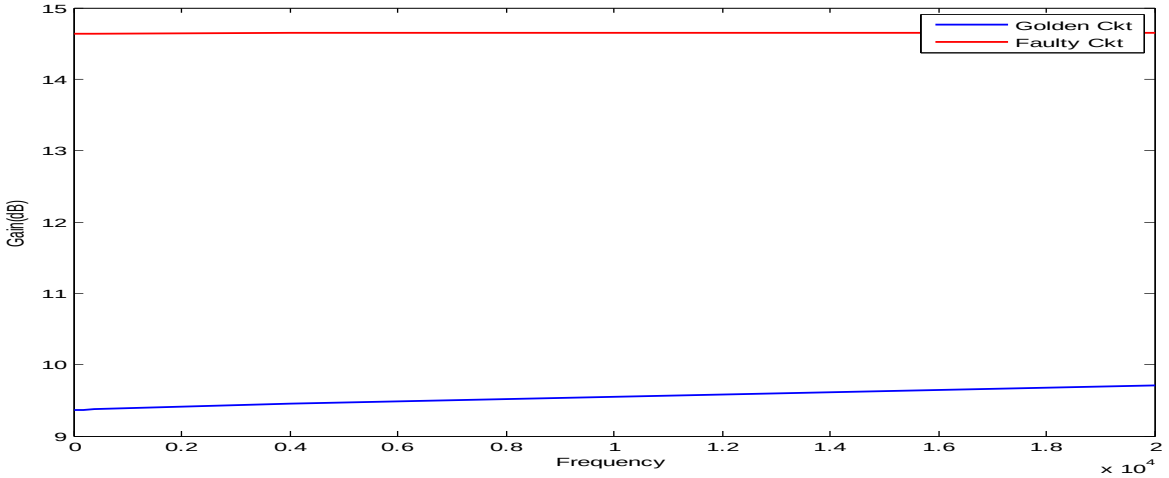


Fig 5.34: Gain Vs Frequency comparison between golden circuit and faulty circuit for M10 stuck on

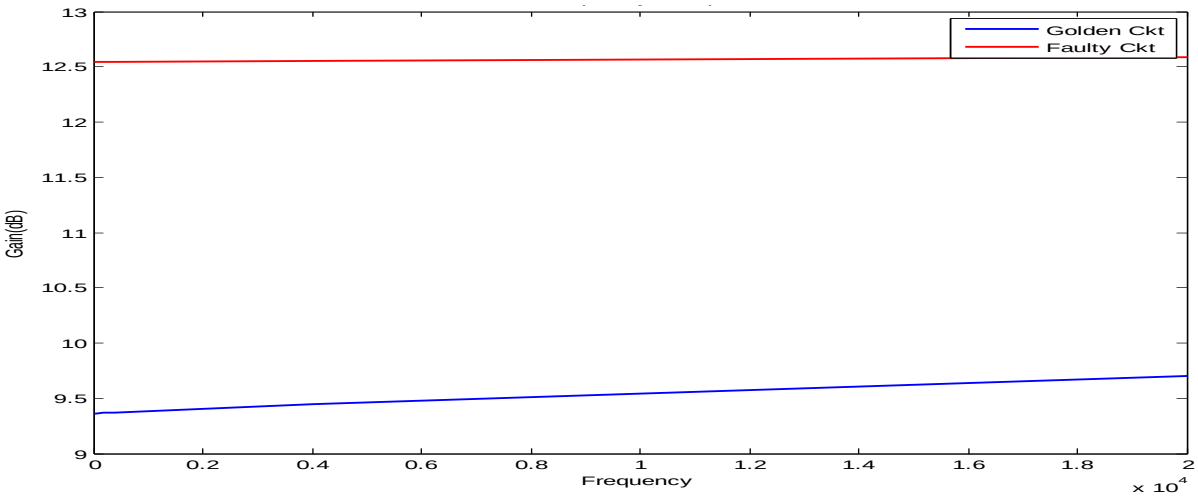


Fig 5.35: Gain Vs Frequency comparison between golden circuit and faulty circuit for M12 stuck on

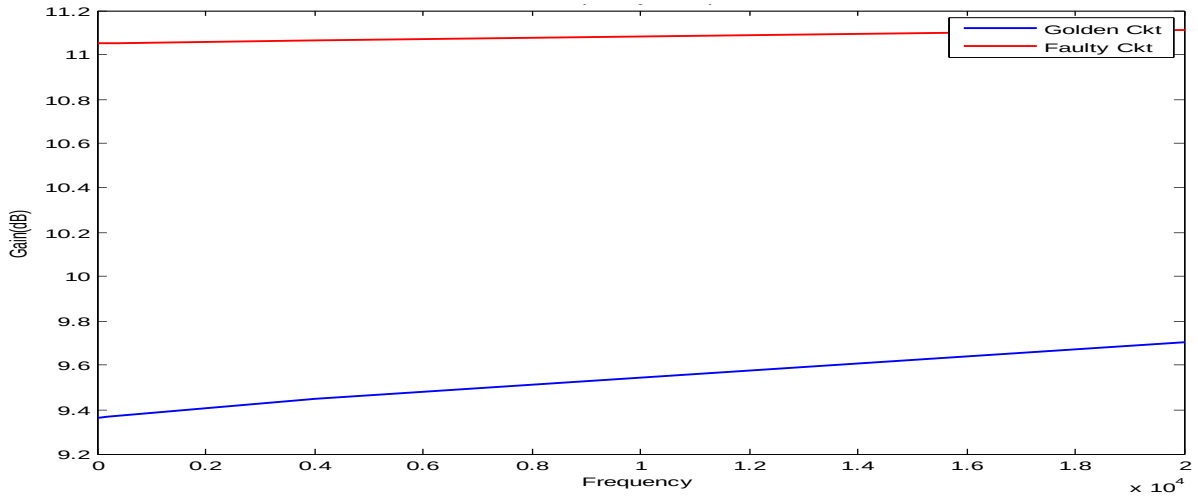


Fig 5.36: Gain Vs Frequency comparison between golden circuit and faulty circuit for M14 stuck on

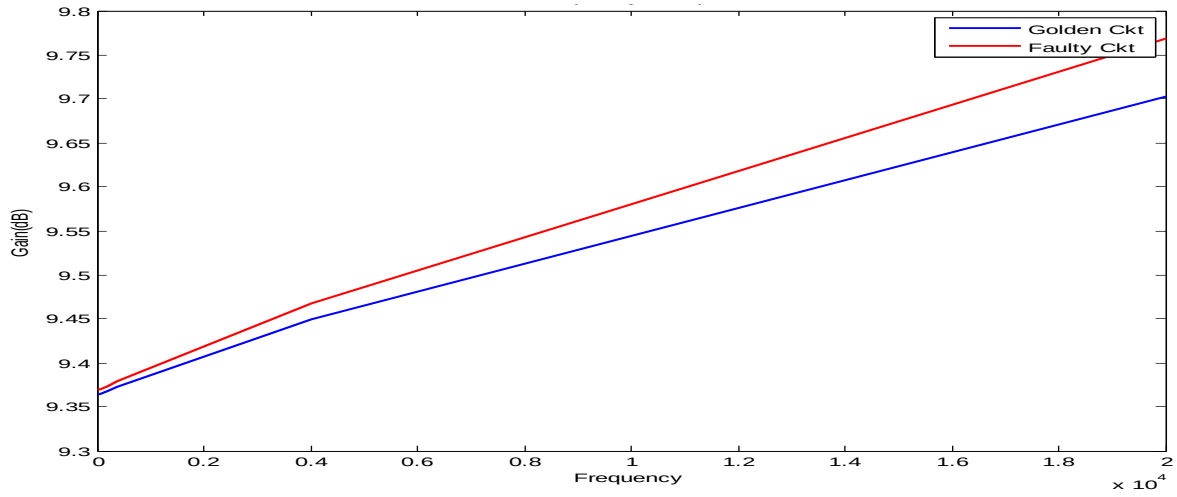


Fig 5.37: Gain Vs Frequency comparison between golden circuit and faulty circuit for M16 stuck on

Table 5.5: Fault(short) in Resistance in DAC

Fault Name	RMS error, Gain(dB)
R1 short	23.8282
R2 short	3.3685
R3 short	0.088391
R4 short	1.4513
R5 short	1.4591
R6 short	1.0048
R7 short	1.2307
R8 short	0.90566
R9 short	0.50368
R10 short	0.933
R11 short	0.37779
R12 short	0.87619
R13 short	1.1975
R14 short	0.44941
R15 short	3.0031
R16 short	3.0442

Comment:

For above faults, if any of the resistance is shorted, then the input current of op-amp in faulty circuit is expected to be greater than fault free circuit. So, both output voltage and gain of faulty circuit is expected to be greater than fault free circuit. This trend is observed in all faults excepting R5, R7 & R9 short where a minor deviation is observed as shown in following graph,

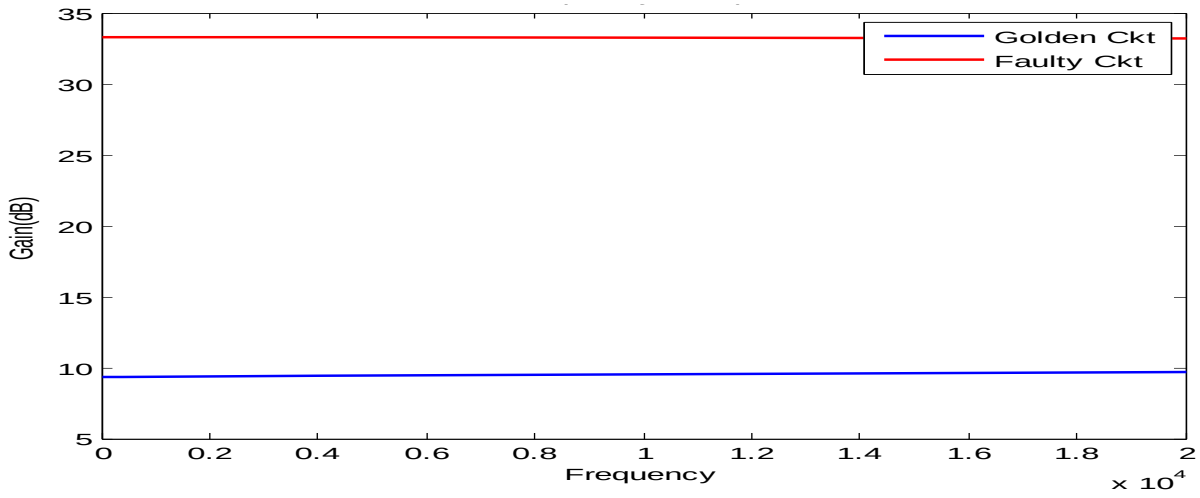


Fig 5.38: Gain Vs Frequency comparison between golden circuit and faulty circuit for R1 short

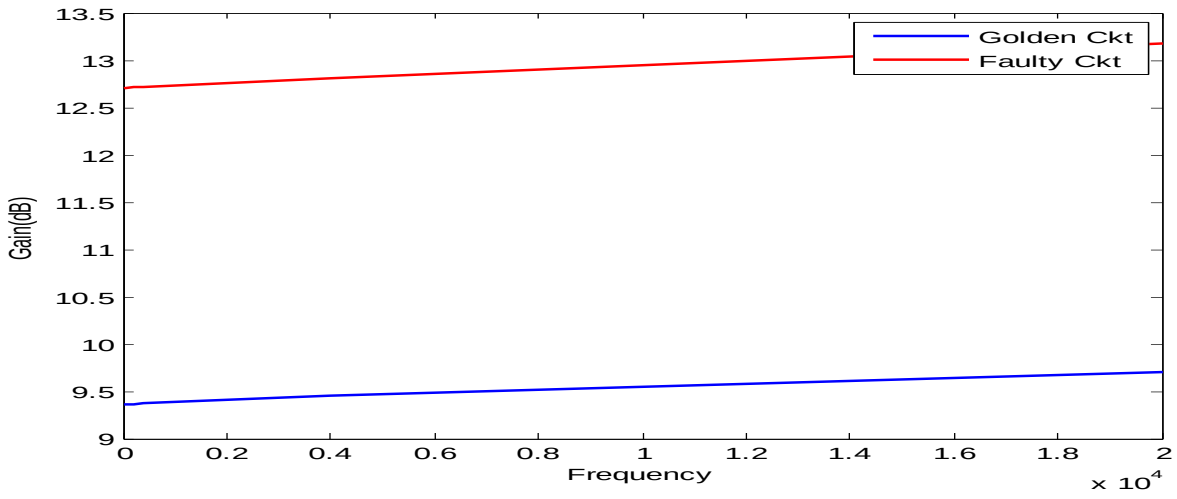


Fig 5.39: Gain Vs Frequency comparison between golden circuit and faulty circuit for R2 short

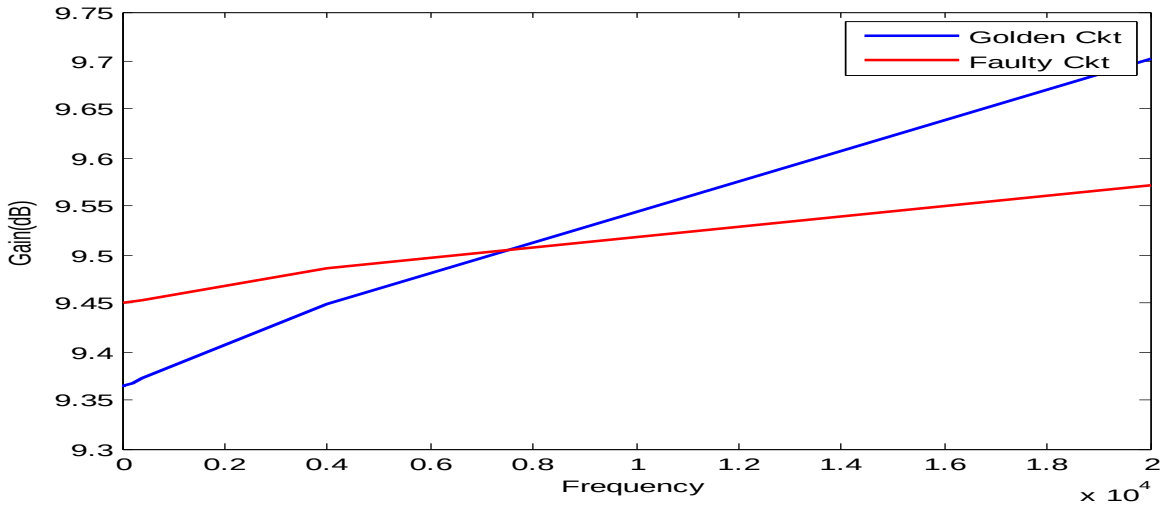


Fig 5.40: Gain Vs Frequency comparison between golden circuit and faulty circuit for R3 short

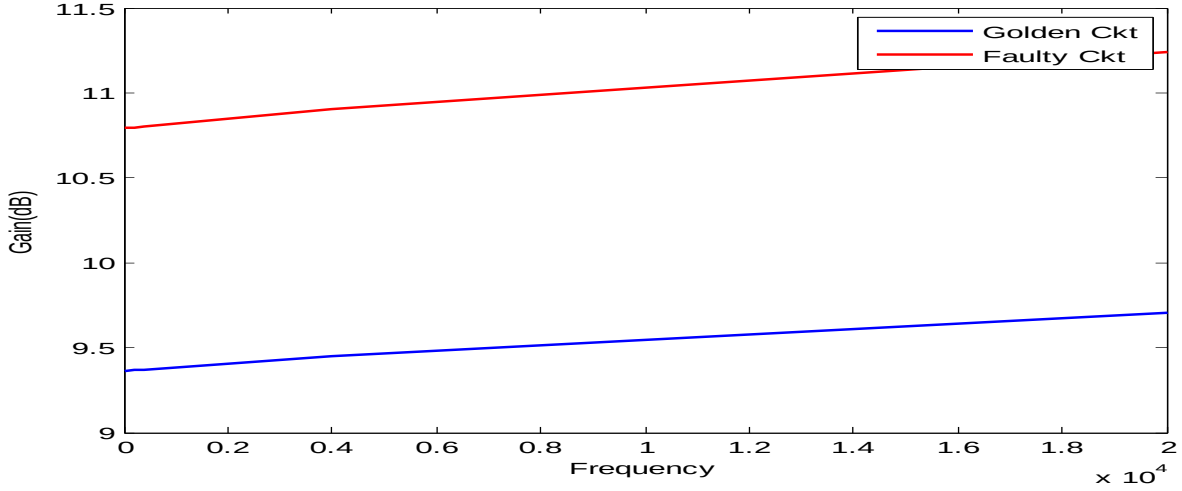


Fig 5.41: Gain Vs Frequency comparison between golden circuit and faulty circuit for R4 short

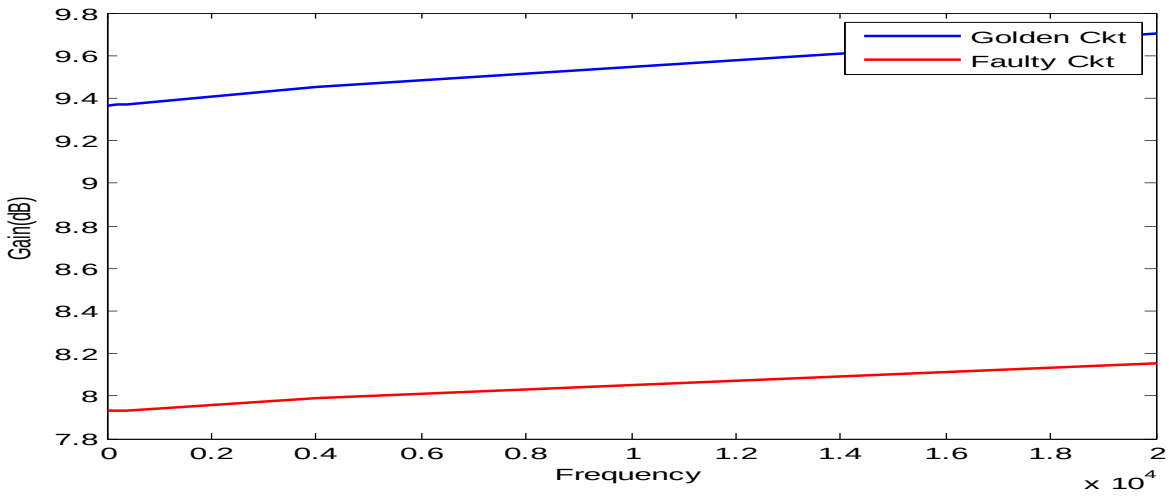


Fig 5.42: Gain Vs Frequency comparison between golden circuit and faulty circuit for R5 short

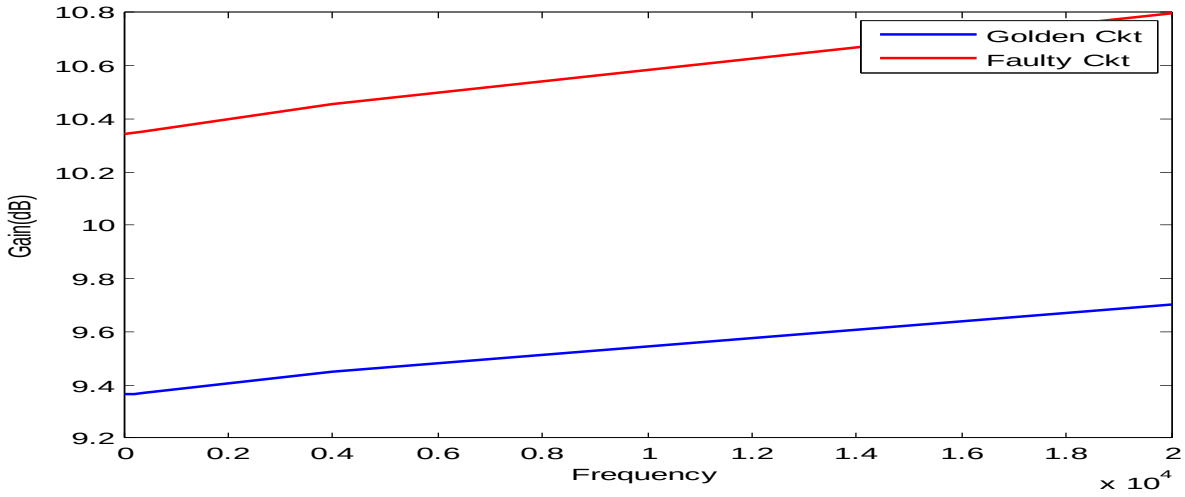


Fig 5.43: Gain Vs Frequency comparison between golden circuit and faulty circuit for R6 short

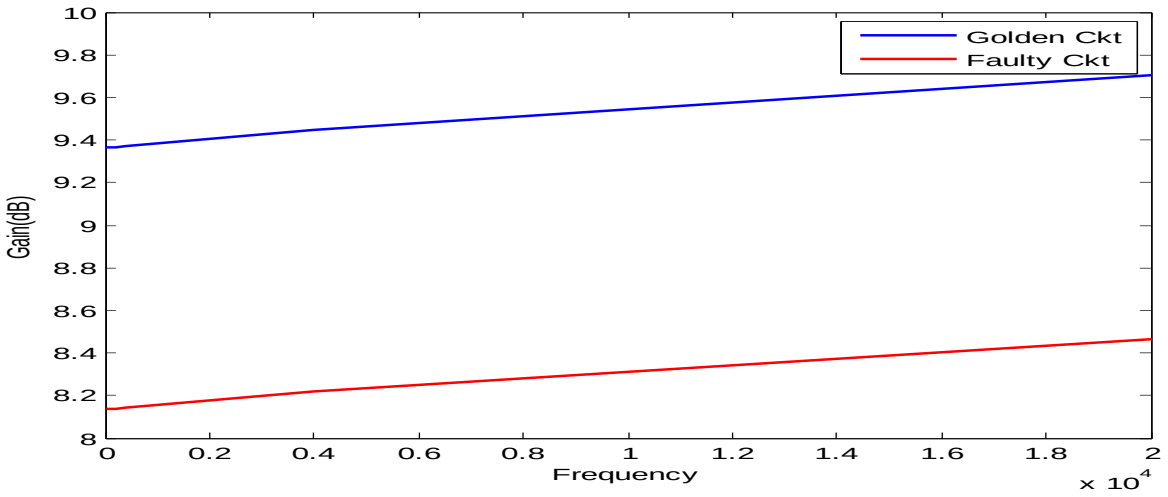


Fig 5.44: Gain Vs Frequency comparison between golden circuit and faulty circuit for R7 short

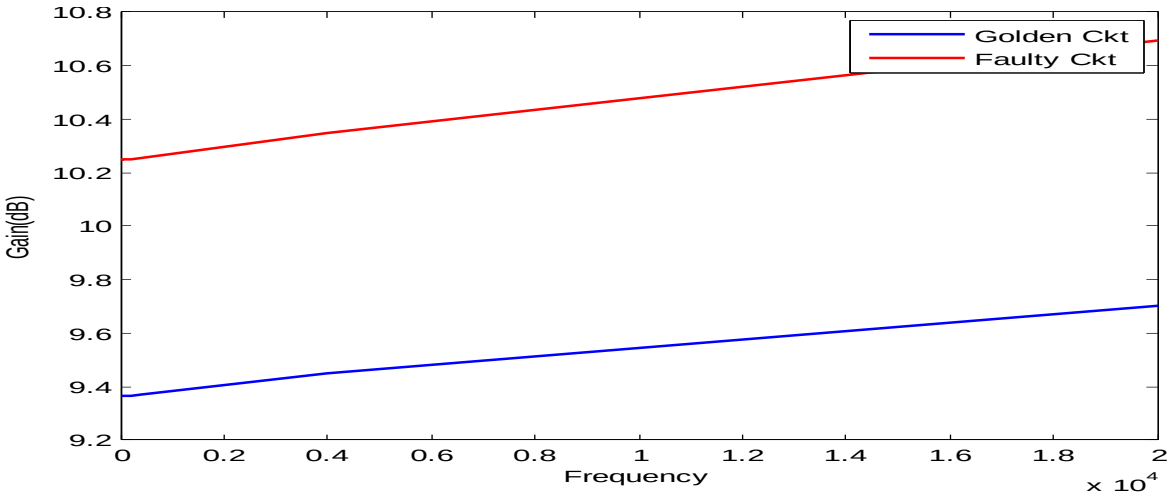


Fig 5.45: Gain Vs Frequency comparison between golden circuit and faulty circuit for R8 short

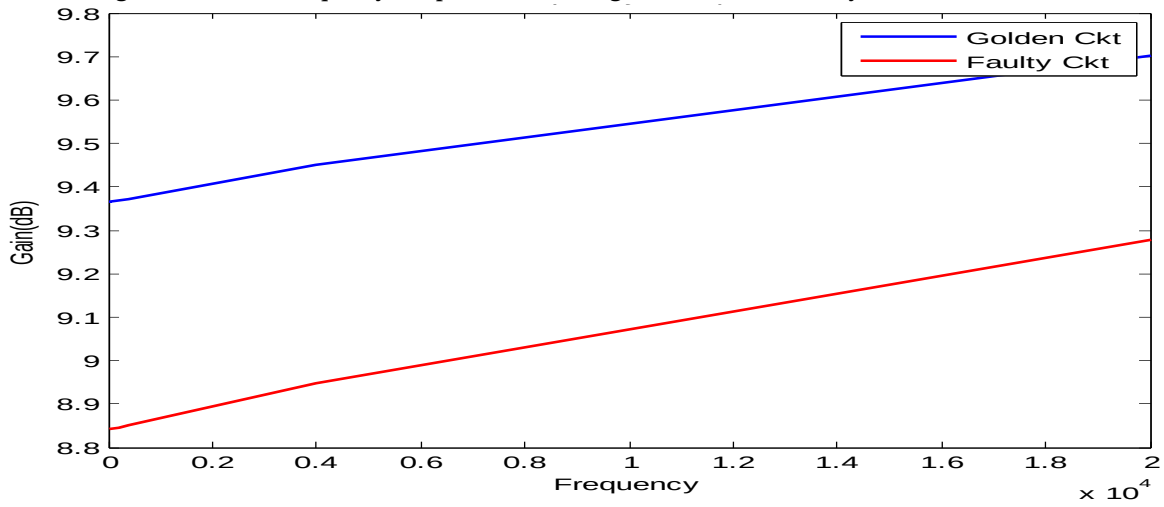


Fig 5.46: Gain Vs Frequency comparison between golden circuit and faulty circuit for R9 short

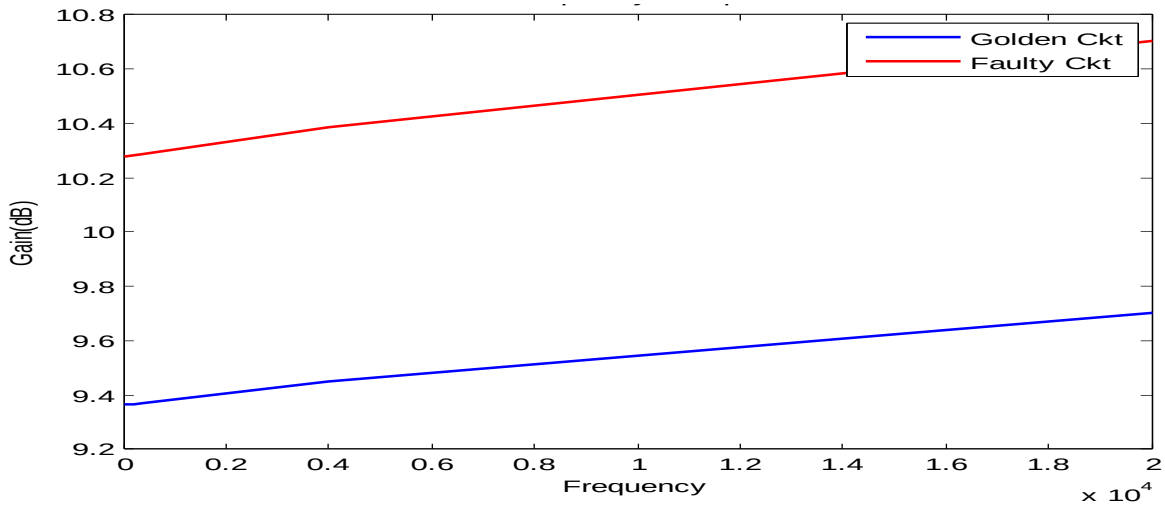


Fig 5.47: Gain Vs Frequency comparison between golden circuit and faulty circuit for R10 short

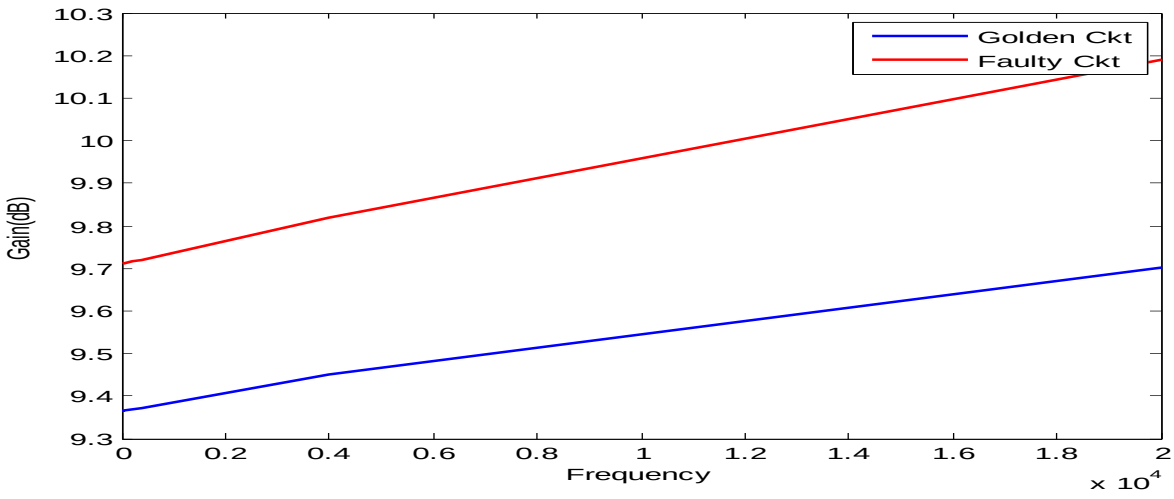


Fig 5.48: Gain Vs Frequency comparison between golden circuit and faulty circuit for R11 short

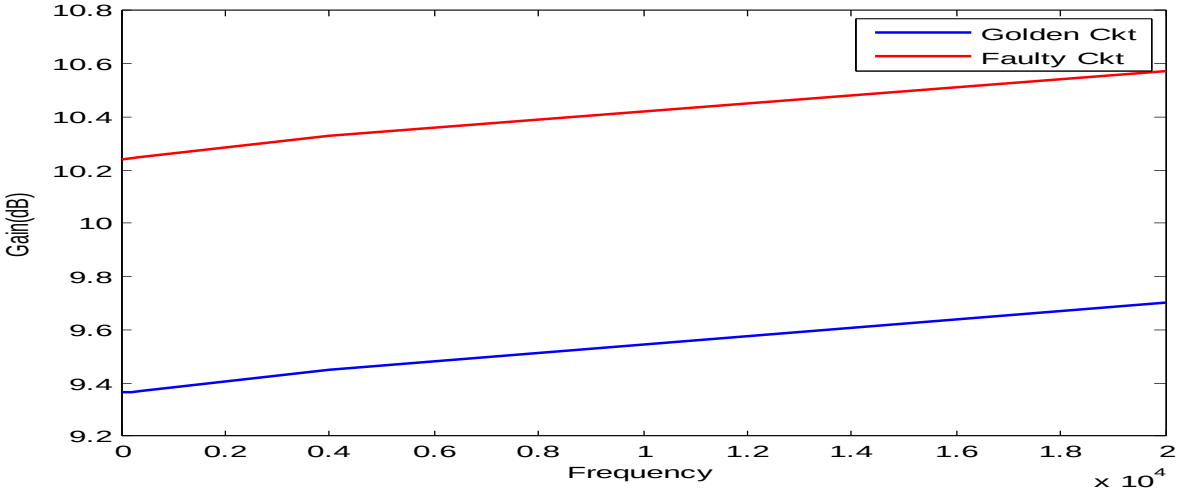


Fig 5.49: Gain Vs Frequency comparison between golden circuit and faulty circuit for R12 short

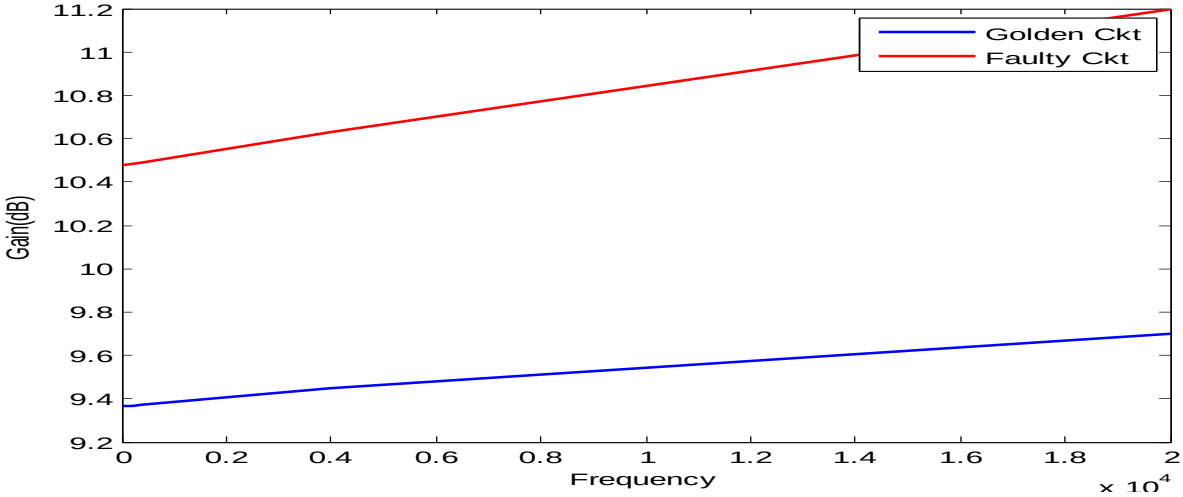


Fig 5.50: Gain Vs Frequency comparison between golden circuit and faulty circuit for R13 short

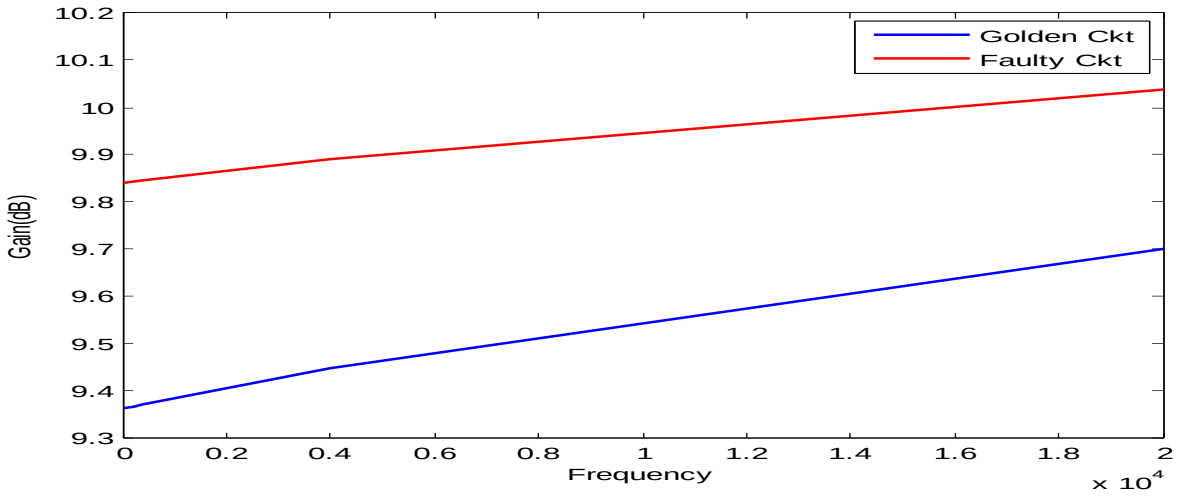


Fig 5.51: Gain Vs Frequency comparison between golden circuit and faulty circuit for R14 short

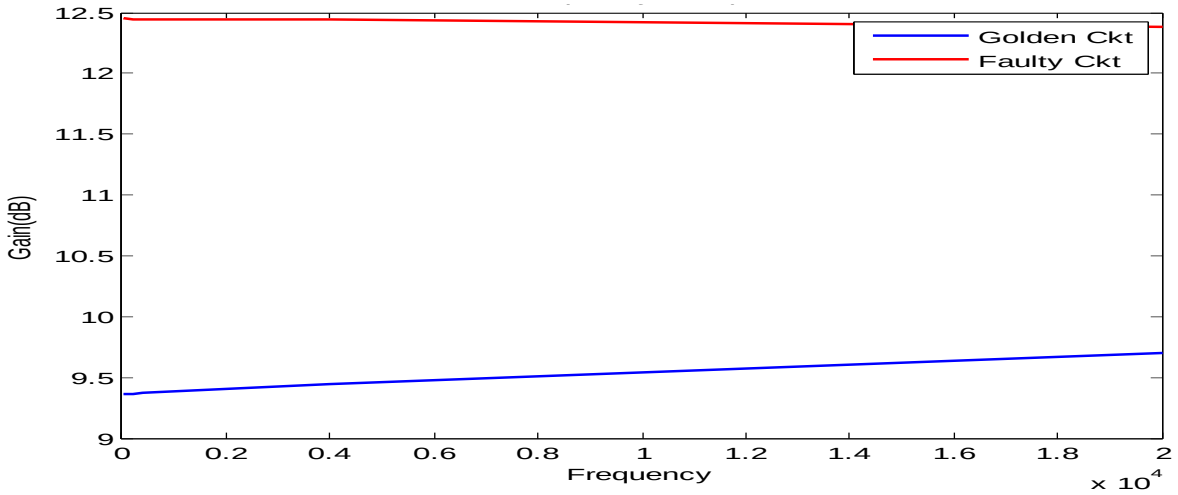


Fig 5.52: Gain Vs Frequency comparison between golden circuit and faulty circuit for R15 short

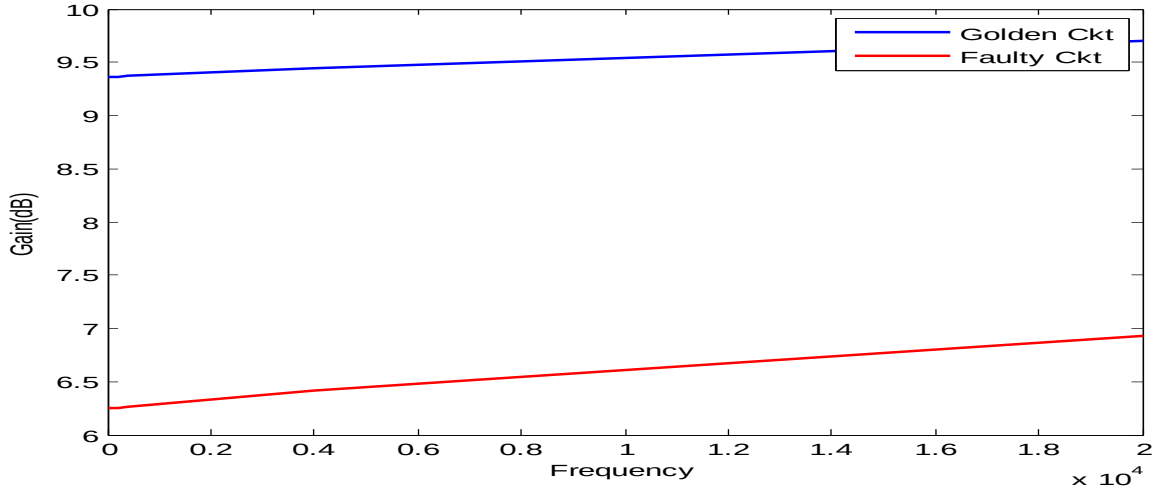


Fig 5.53: Gain Vs Frequency comparison between golden circuit and faulty circuit for R16 short

Table 5.6: Fault (stuck on) in Resistance & Capacitance across op-amp

Fault Name	RMS error, Gain(dB)
r short	18.5537
C2 short	18.553

Comment:

When r & C2 are stuck oned, current doesn't pass through the op-amp, so it cannot amplify. For this reason, both output voltage & gain of faulty circuit are less than fault free circuit as shown in graph,

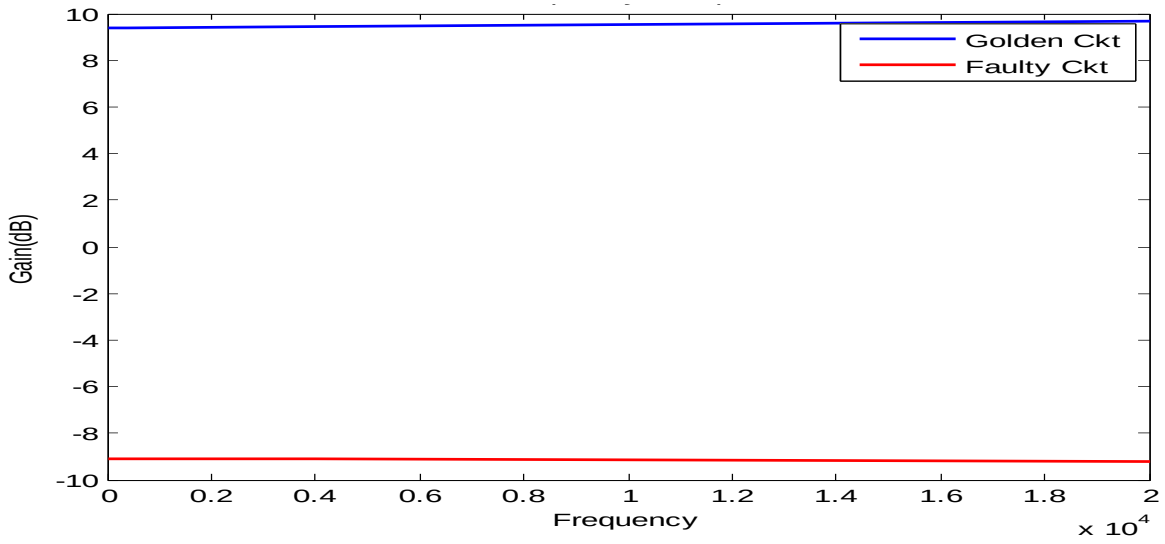


Fig 5.54: Gain Vs Frequency comparison between golden circuit and faulty circuit for r short

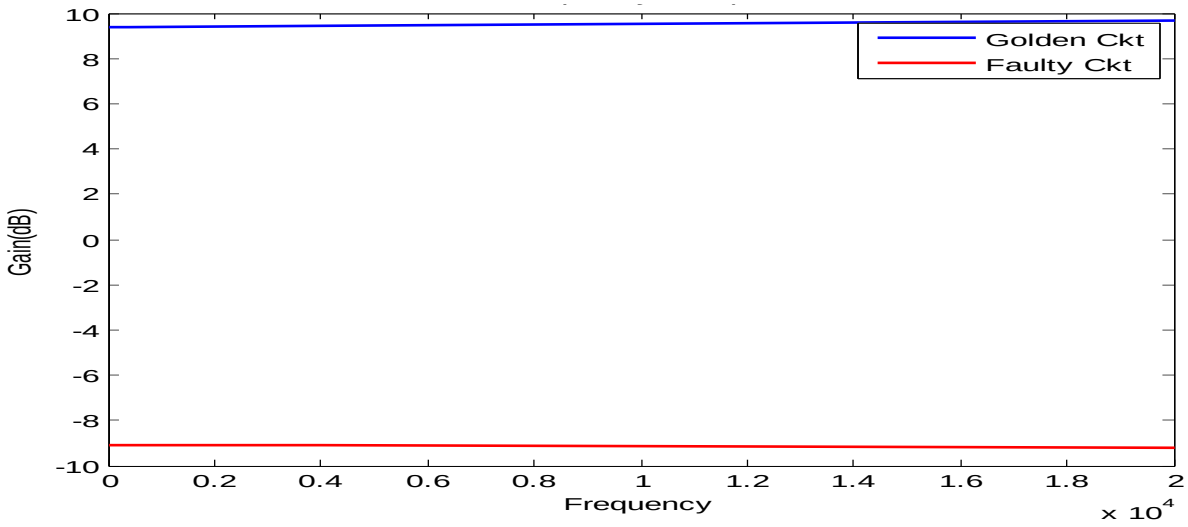


Fig 5.55: Gain Vs Frequency comparison between golden circuit and faulty circuit for C2 short

Table 5.7: Fault (open) in Resistance & Capacitance in DAC

Fault Name	RMS error, Gain(dB)
R1 open	2.6007
R2 open	10.5566
R3 open	0.24823
R4 open	6.631
R5 open	0.41945
R6 open	5.242
R7 open	0.48689
R8 open	4.6046
R9 open	0.30722
R10 open	4.0319
R11 open	0.092466
R12 open	3.133
R13 open	0.62976
R14 open	1.4569
R15 open	2.1973
R16 open	1.4254

Comment:

For above faults, if any of the resistance is stuck opened, then the input current of op-amp in faulty circuit is expected to be less than fault free circuit. So, both output voltage and gain of faulty circuit is expected to be less than fault free circuit. This trend is observed in all faults excepting R5,RR7 & R9 stuck open where a minor deviation is observed as shown in following graph,

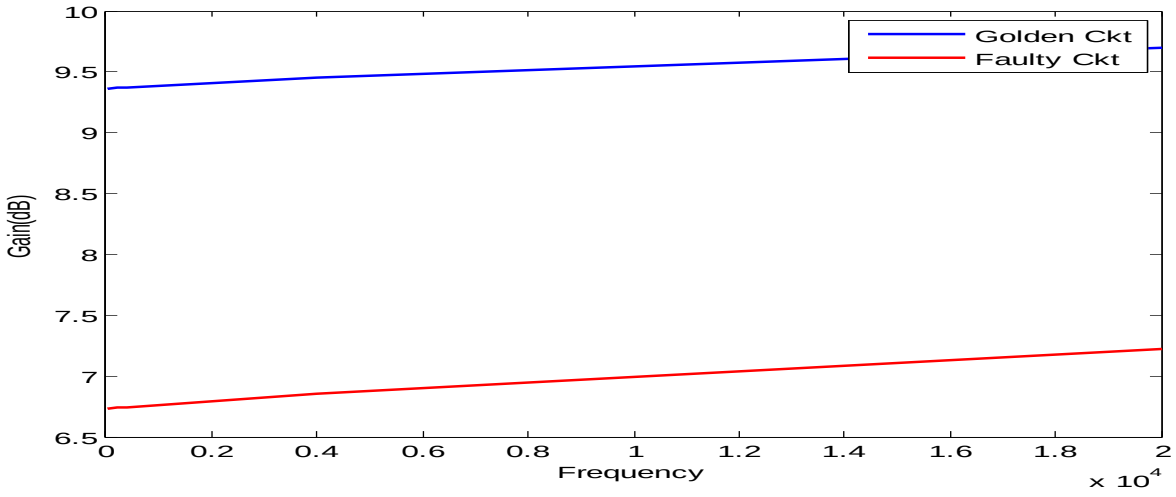


Fig 5.56: Gain Vs Frequency comparison between golden circuit and faulty circuit for R1 open

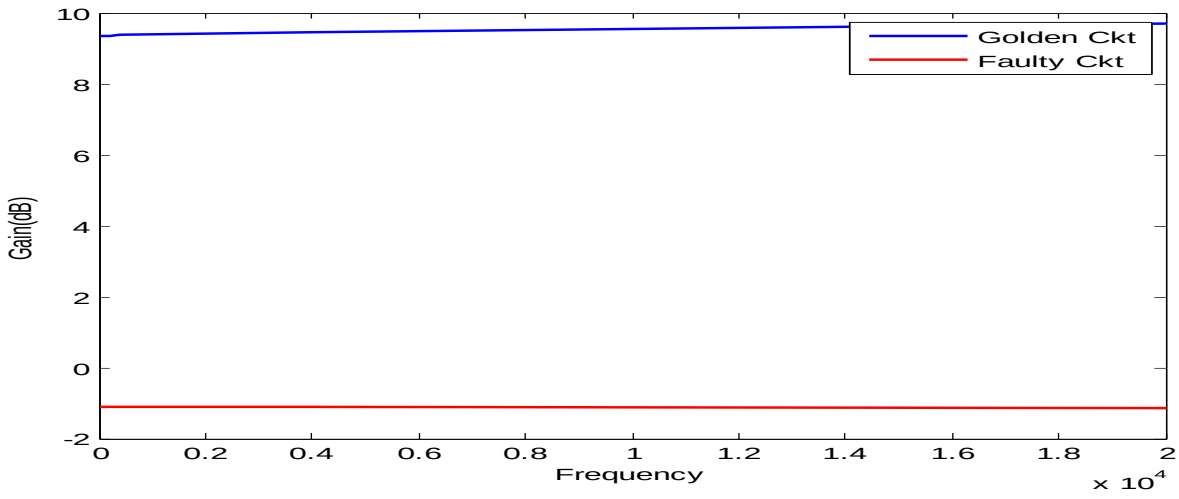


Fig 5.57: Gain Vs Frequency comparison between golden circuit and faulty circuit for R2 open

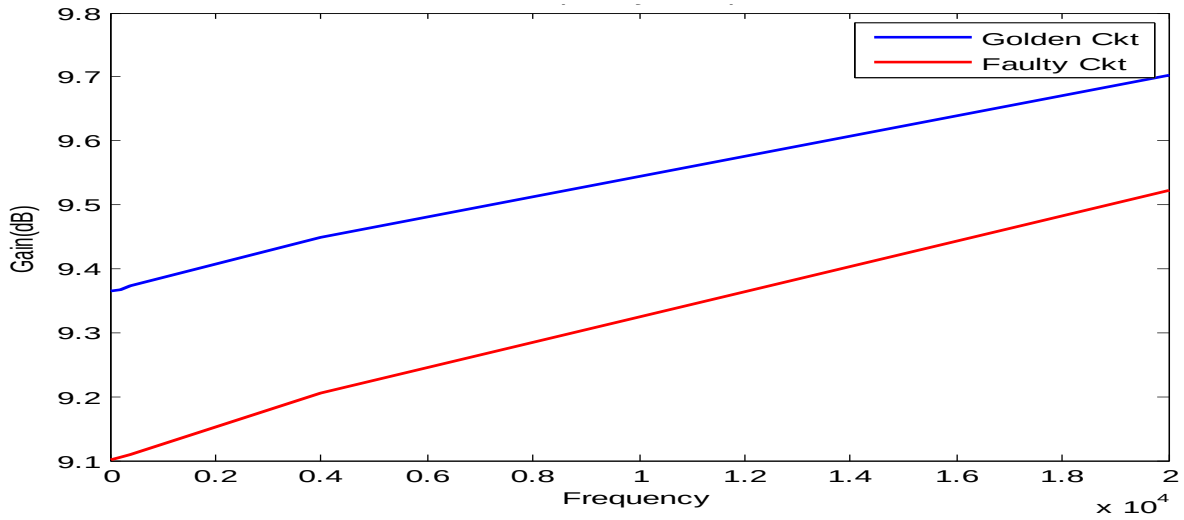


Fig 5.58: Gain Vs Frequency comparison between golden circuit and faulty circuit for R3 open

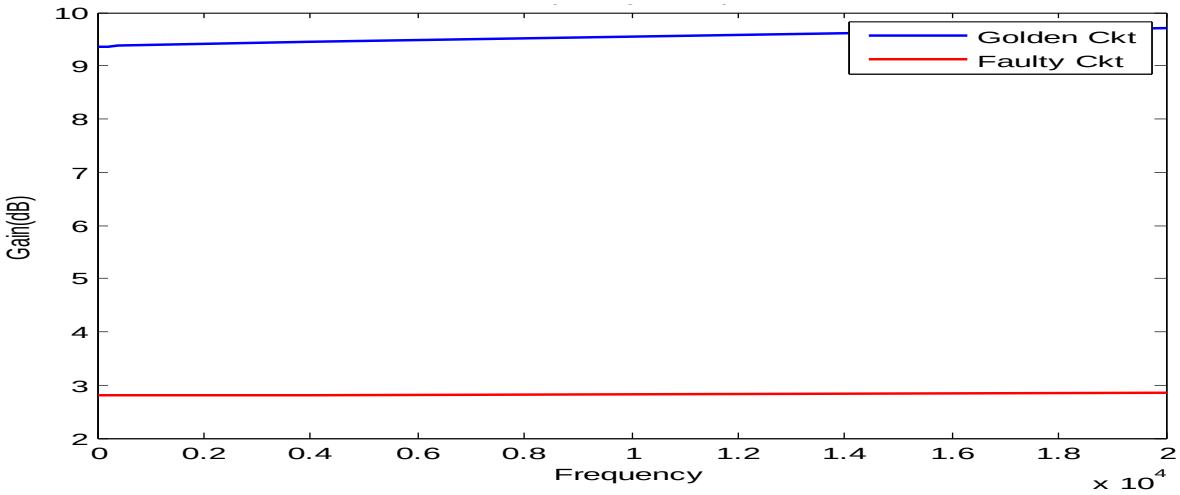


Fig 5.59: Gain Vs Frequency comparison between golden circuit and faulty circuit for R4 open

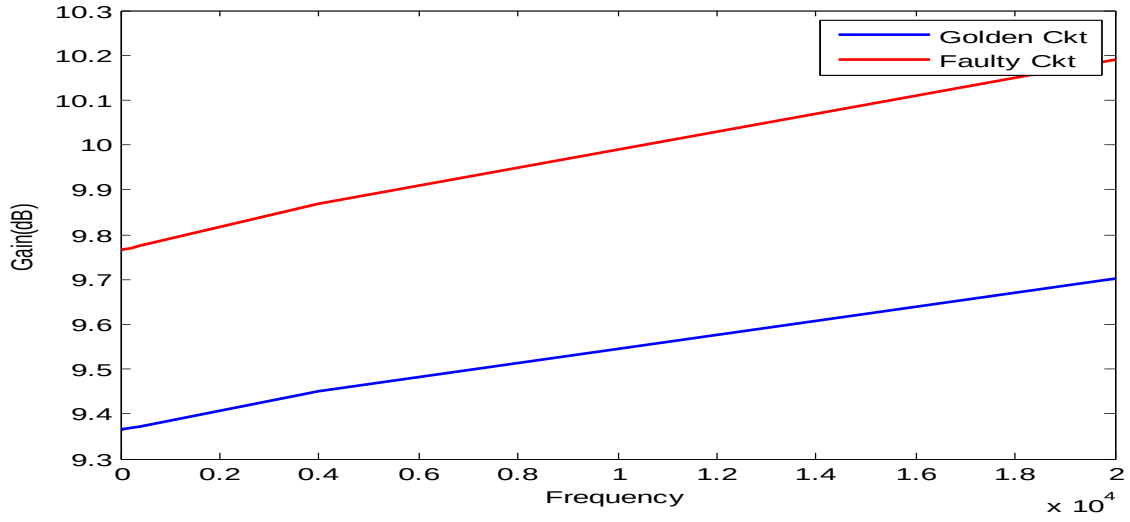


Fig 5.60: Gain Vs Frequency comparison between golden circuit and faulty circuit for R5 open

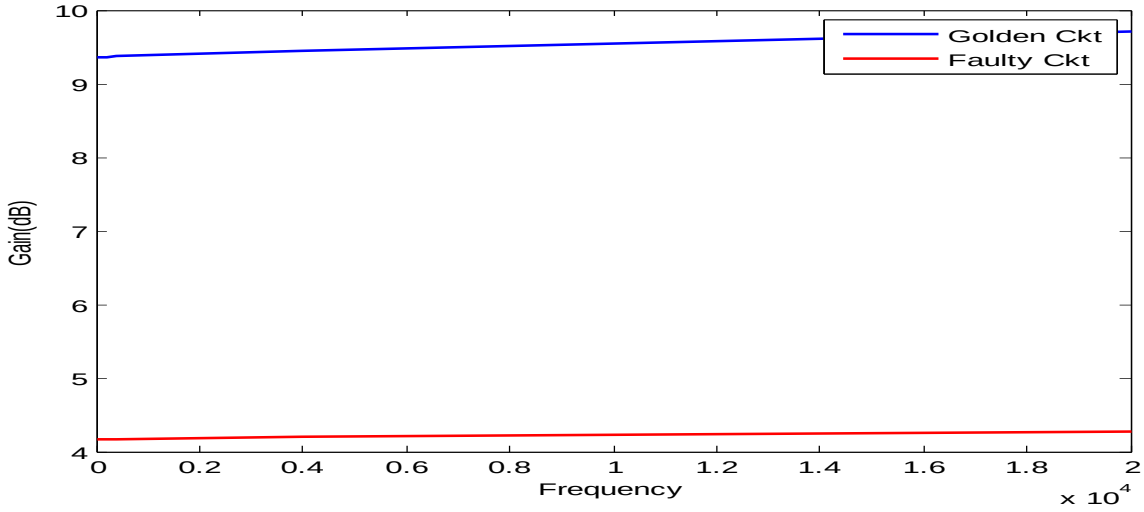


Fig 5.61: Gain Vs Frequency comparison between golden circuit and faulty circuit for R6 open

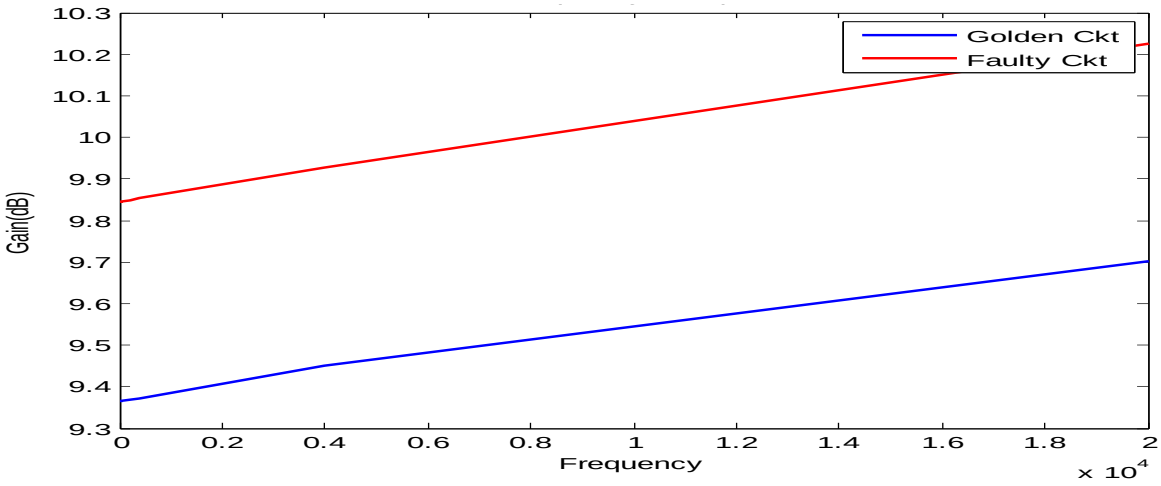


Fig 5.62: Gain Vs Frequency comparison between golden circuit and faulty circuit for R7 open

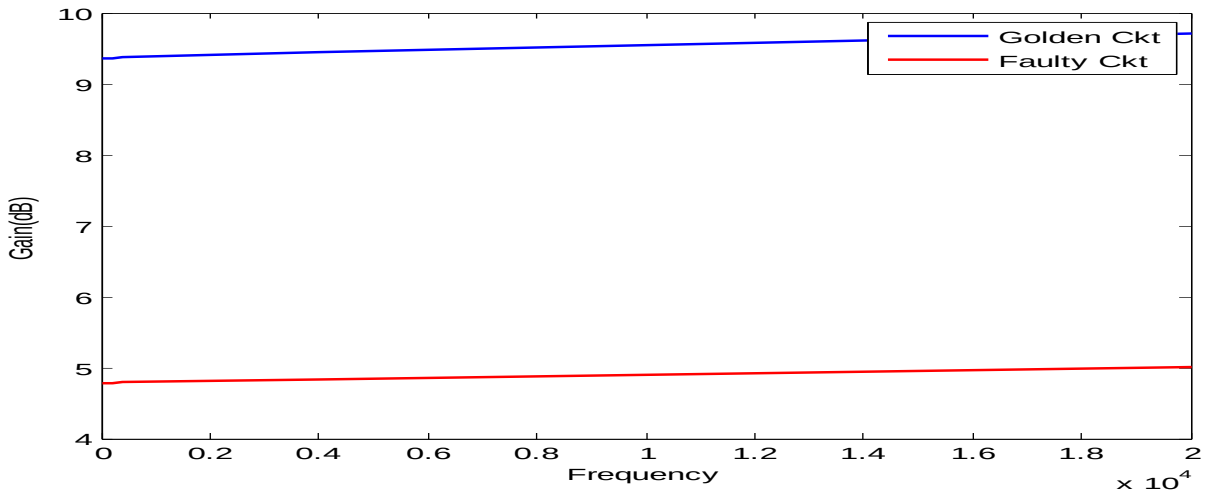


Fig 5.63: Gain Vs Frequency comparison between golden circuit and faulty circuit for R8 open

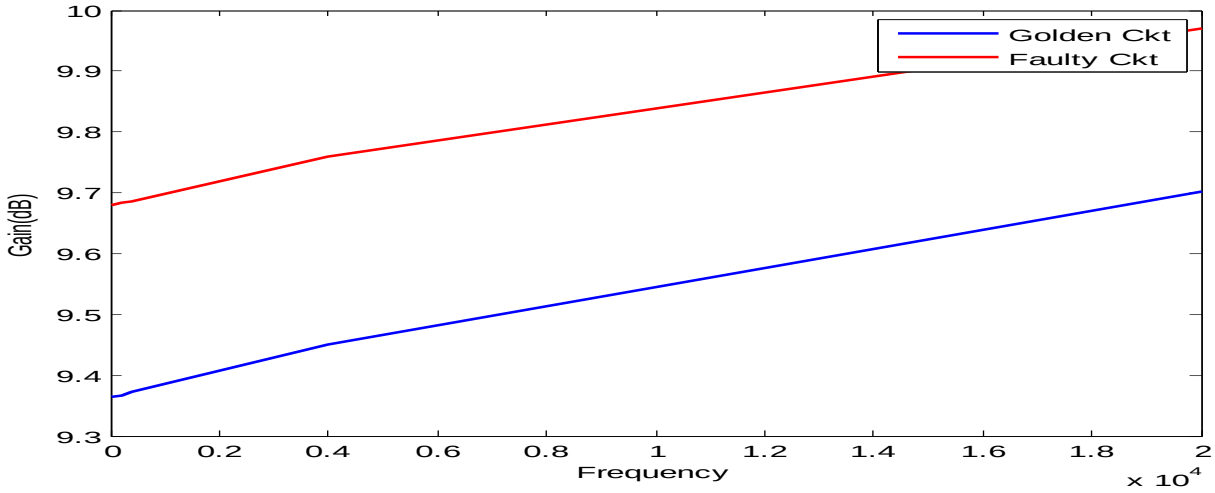


Fig 5.64: Gain Vs Frequency comparison between golden circuit and faulty circuit for R9 open

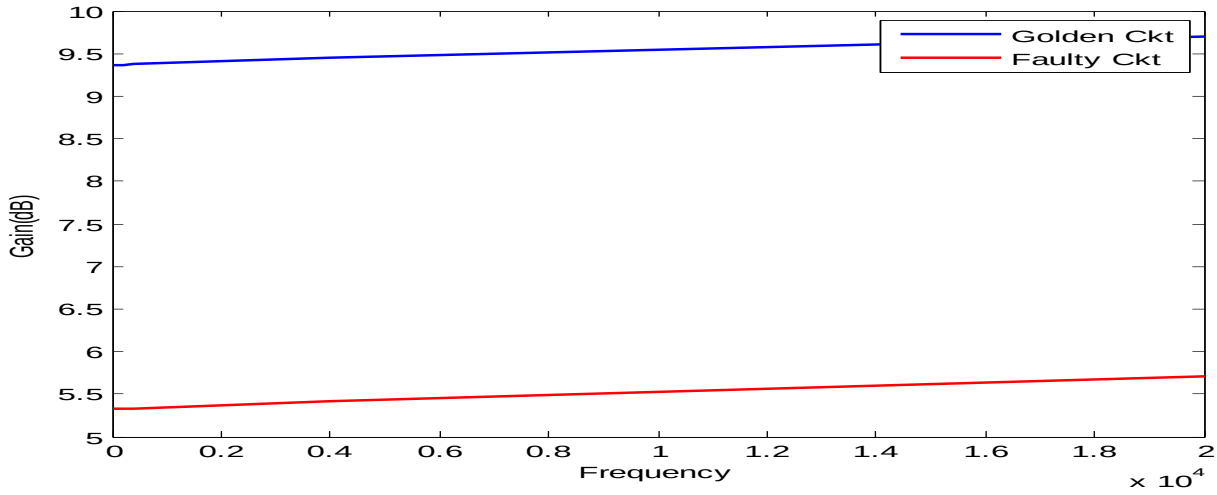


Fig 5.65: Gain Vs Frequency comparison between golden circuit and faulty circuit for R10 open

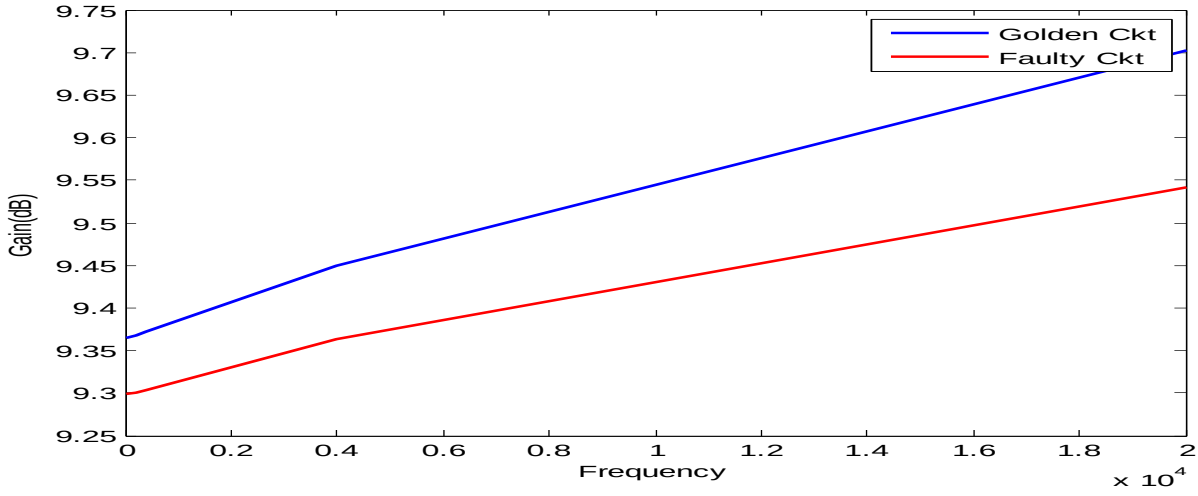


Fig 5.66: Gain Vs Frequency comparison between golden circuit and faulty circuit for R11 open

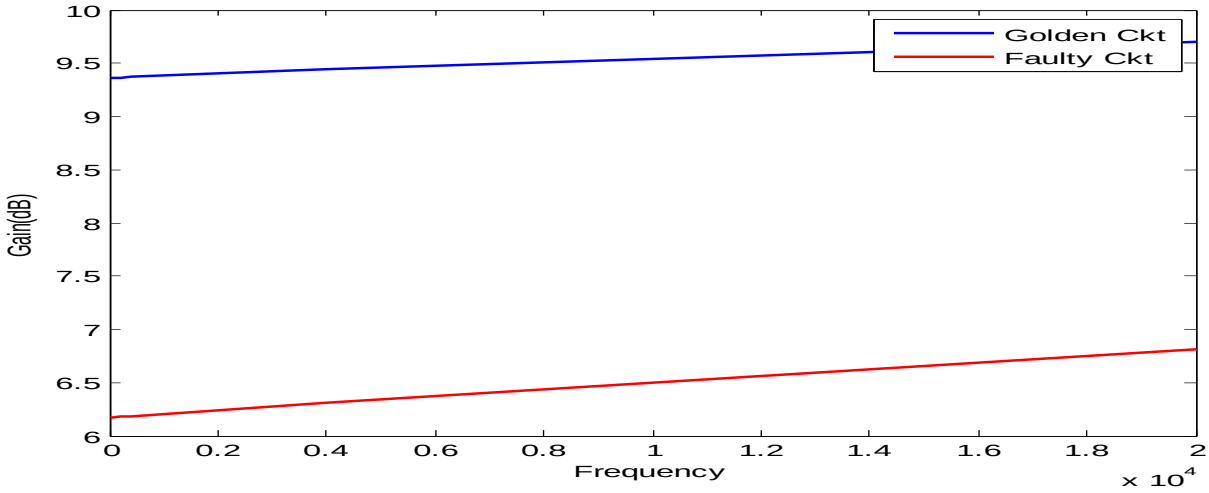


Fig 5.67: Gain Vs Frequency comparison between golden circuit and faulty circuit for R12 open

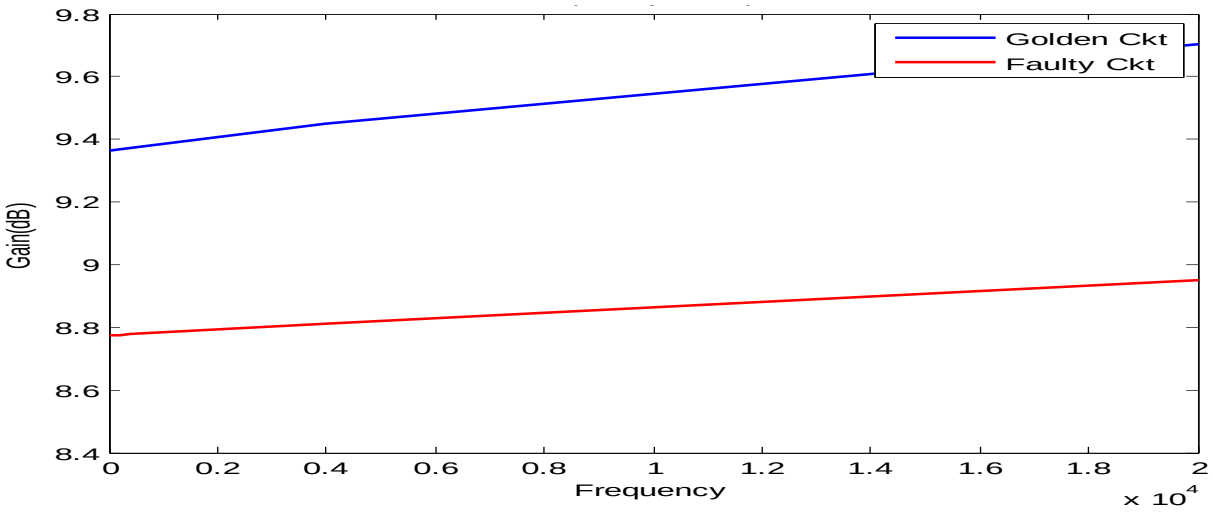


Fig 5.68: Gain Vs Frequency comparison between golden circuit and faulty circuit for R13 open

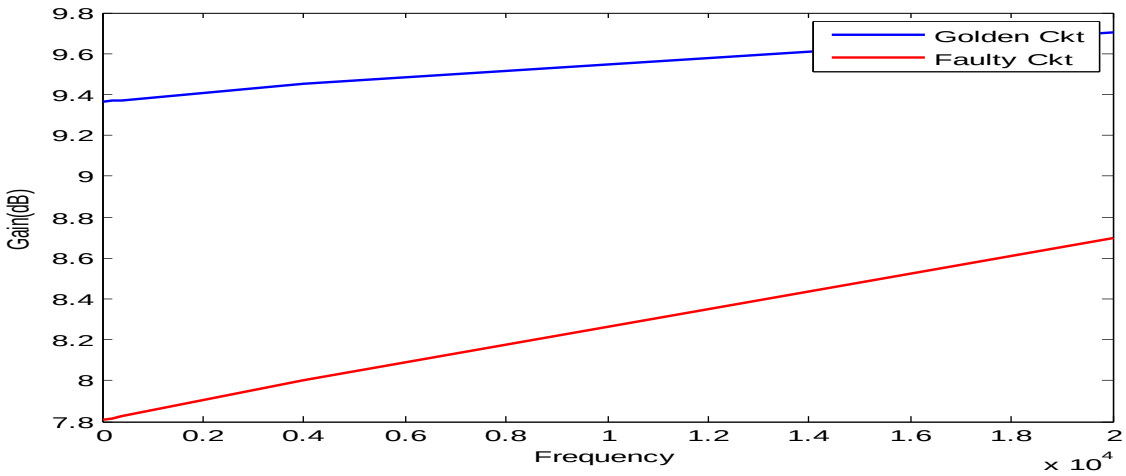


Fig 5.69: Gain Vs Frequency comparison between golden circuit and faulty circuit for R14 open

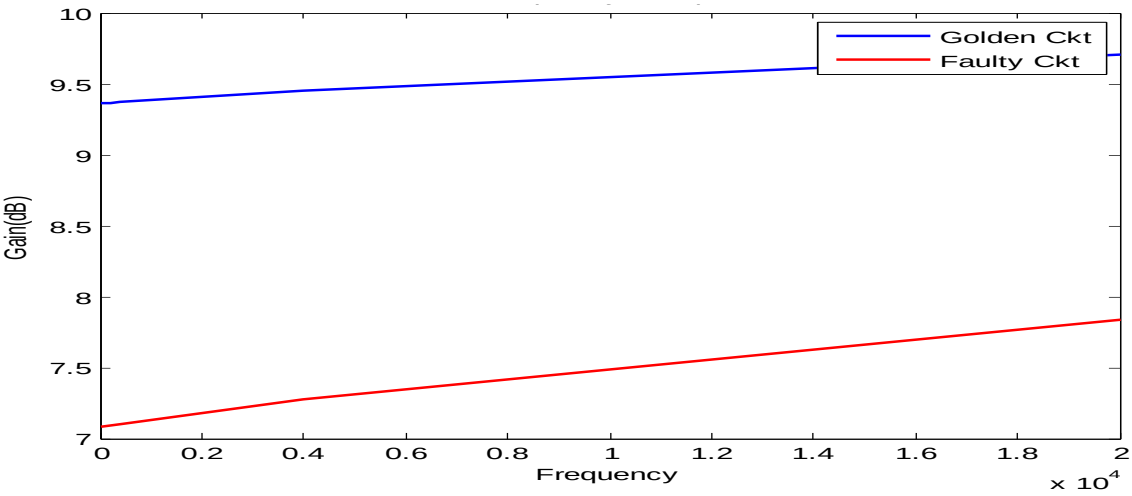


Fig 5.70: Gain Vs Frequency comparison between golden circuit and faulty circuit for R15 open

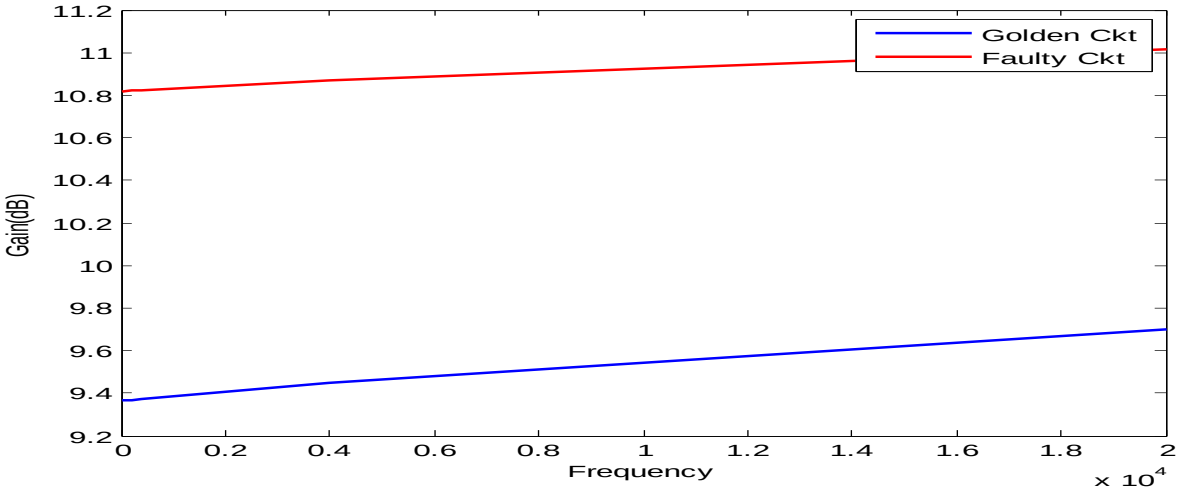


Fig 5.71: Gain Vs Frequency comparison between golden circuit and faulty circuit for R16 open

Table 5.8**:** Fault (open) in Resistance & Capacitance across op-amp

Fault Name	RMS error, Gain(dB)
r open	33.0374
C2 open	0.19233

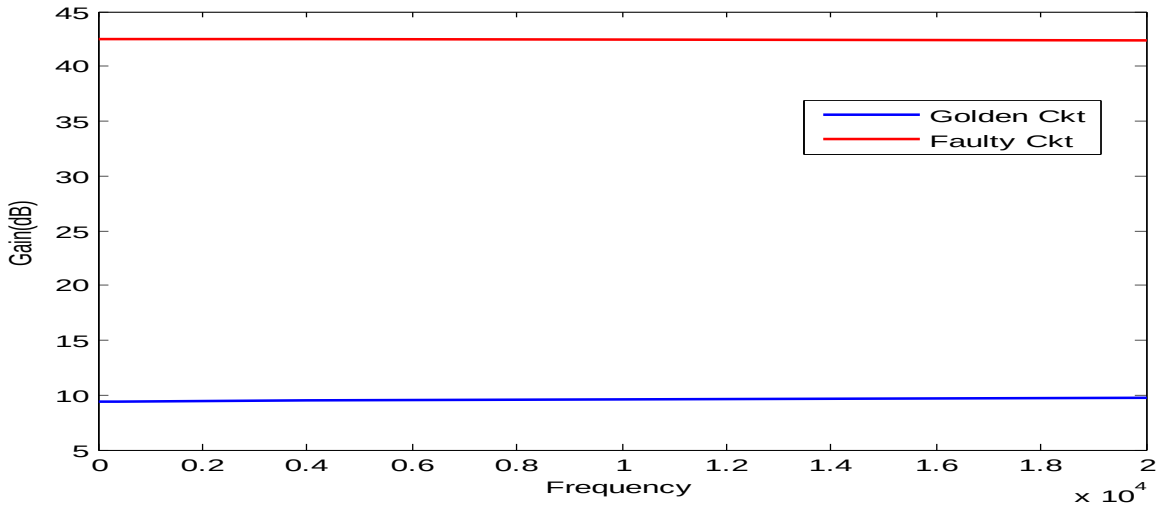


Fig 5.72: Gain Vs Frequency comparison between golden circuit and faulty circuit for r open

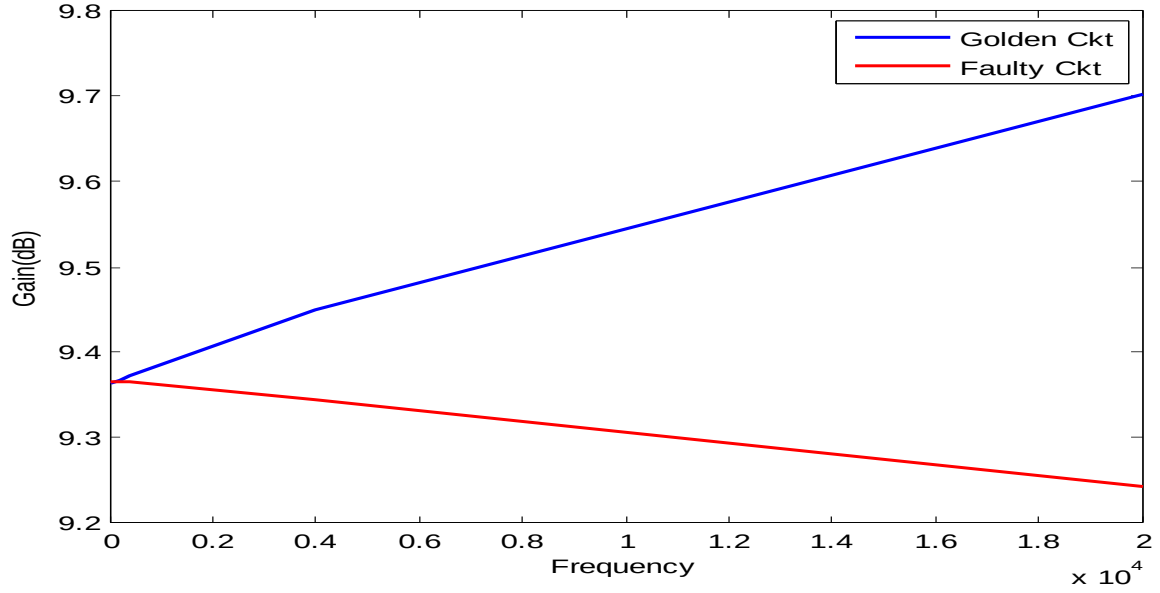


Fig 5.73: Gain Vs Frequency comparison between golden circuit and faulty circuit for C2 open

5.2 Op Amp Faults

Table 5.9: Stuck on Fault of MOSFETs in op-amp

Fault name	RMS Gain Error (DB)
M1 stuck on	4.1858
M2 stuck on	3.9068
M3 stuck on	4.5163
M4 stuck on	4.4768
M5 stuck on	4.1823
M6 stuck on	5.7191
M7 stuck on	34.5434
M8 stuck on	31.5732
M9 stuck on	22.3704
M10 stuck on	23.138
M11 stuck on	31.5732
M12 stuck on	4.4969
M13 stuck on	31.2138
M14 stuck on	31.214
M15 stuck on	51.3027
M16 stuck on	51.3027

For above Faults, Graphs are given bellow,

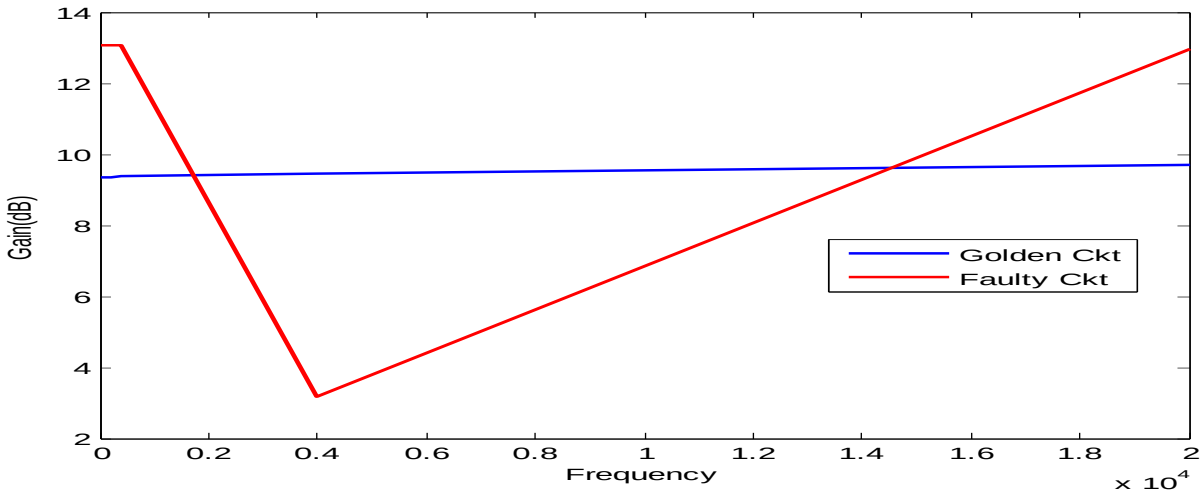


Fig 5.74: Gain Vs Frequency comparison between golden circuit and faulty circuit for M1 stuck on(op-amp)

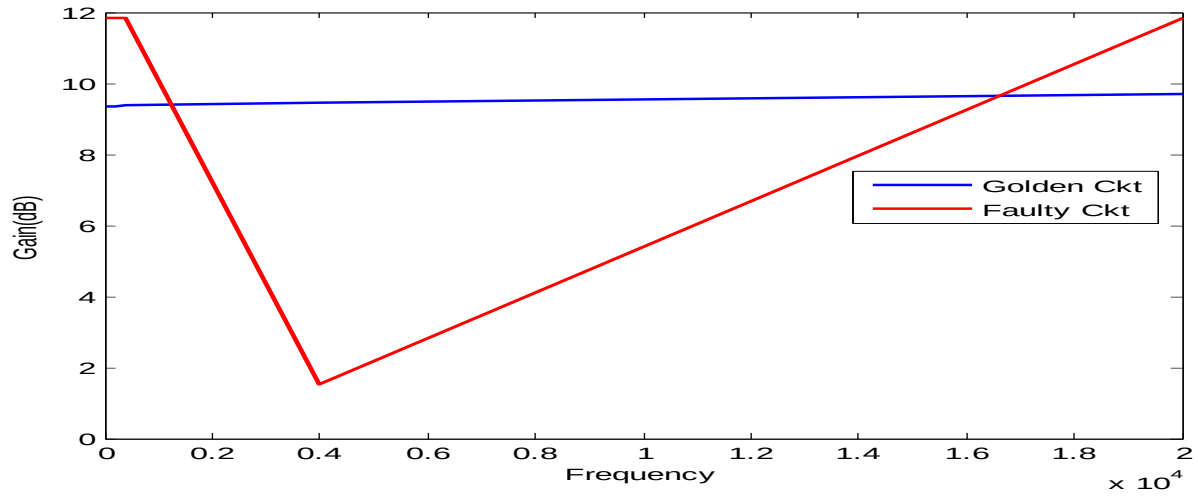


Fig 5.75: Gain Vs Frequency comparison between golden circuit and faulty circuit for M2 stuck on(op-amp)

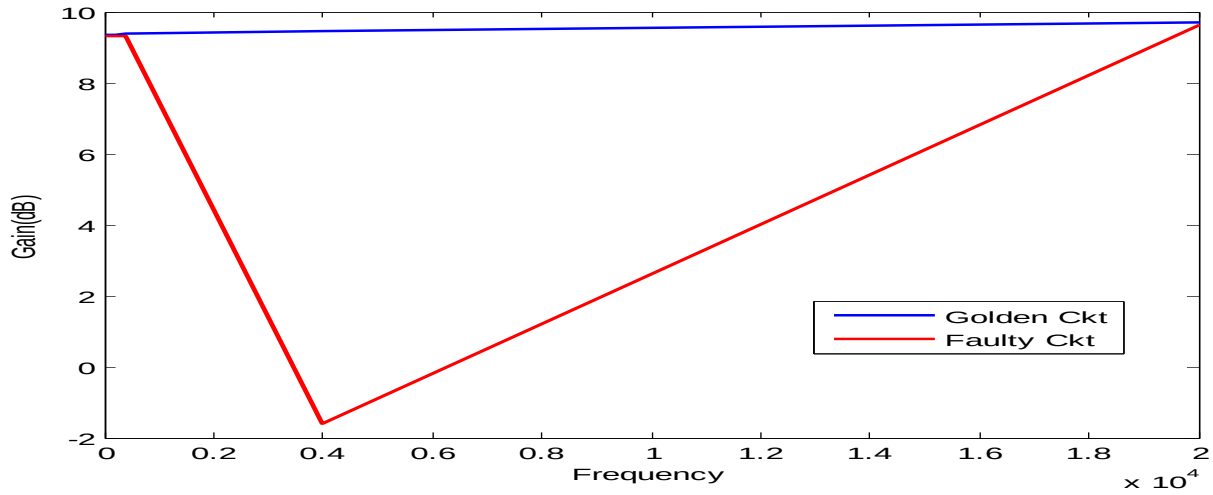


Fig 5.76: Gain Vs Frequency comparison between golden circuit and faulty circuit for M3 stuck on(op-amp)

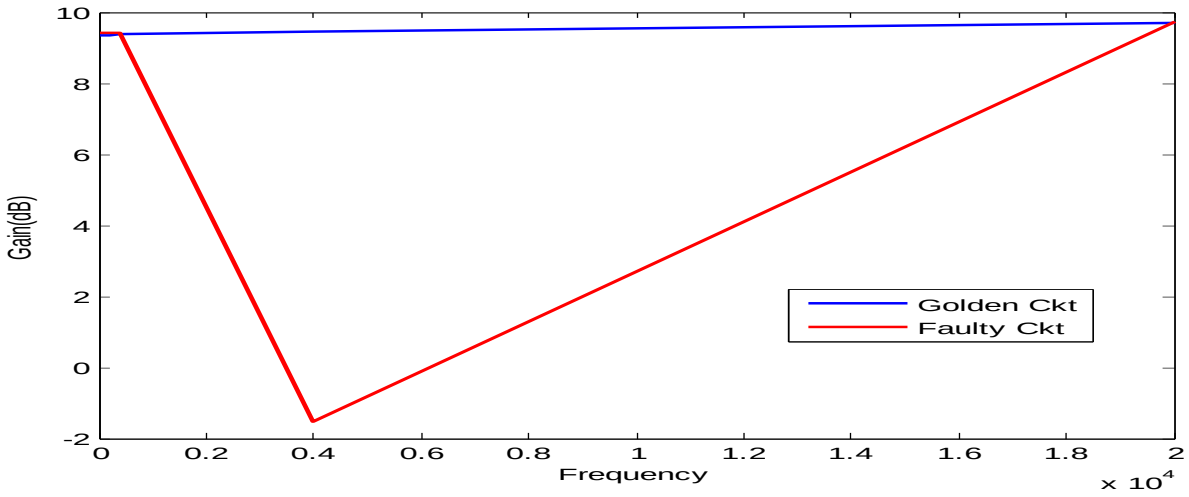


Fig 5.77: Gain Vs Frequency comparison between golden circuit and faulty circuit for M4 stuck on(op-amp)

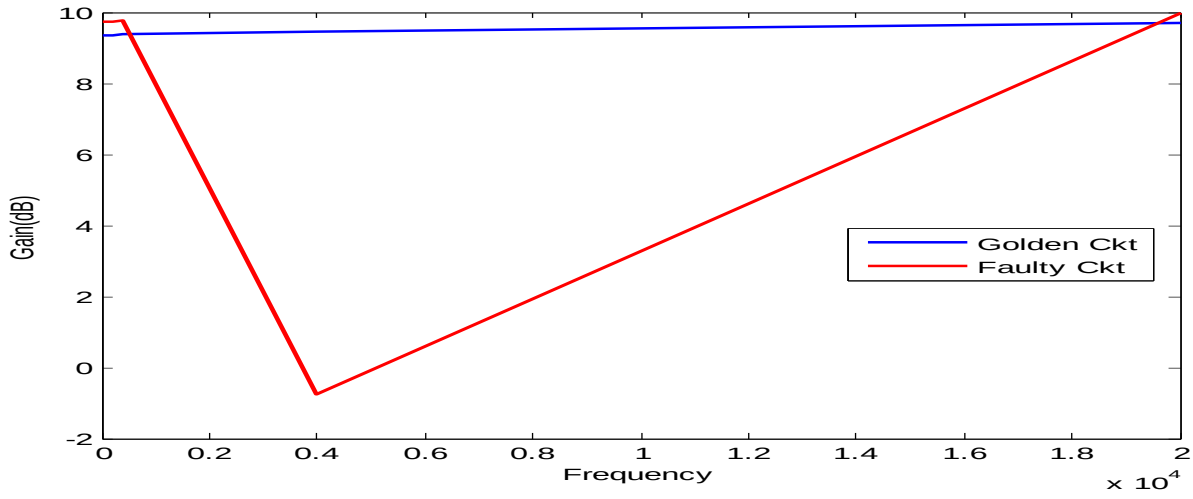


Fig 5.78: Gain Vs Frequency comparison between golden circuit and faulty circuit for M5 stuck on(op-amp)

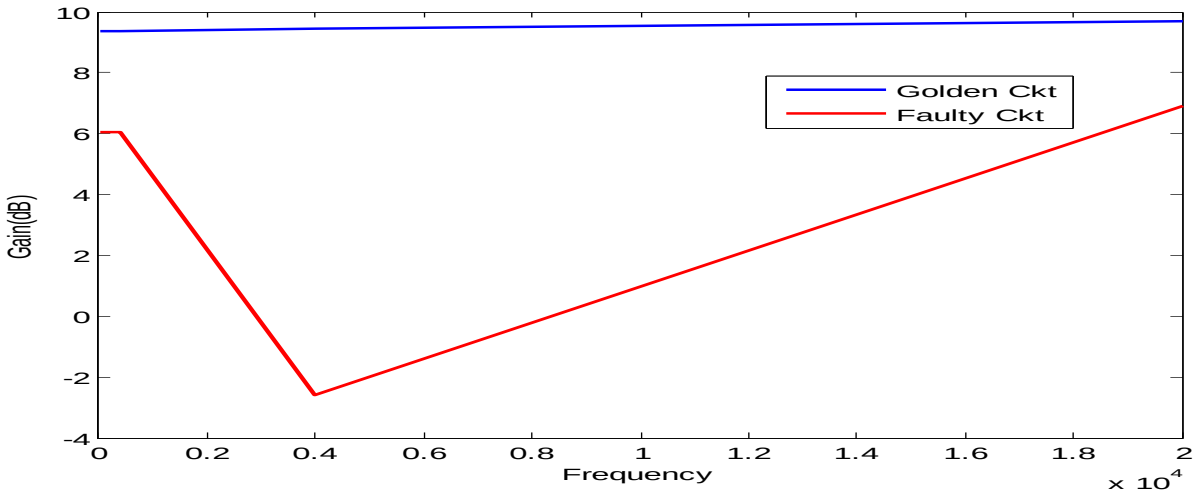


Fig 5.79: Gain Vs Frequency comparison between golden circuit and faulty circuit for M6 stuck on(op-amp)

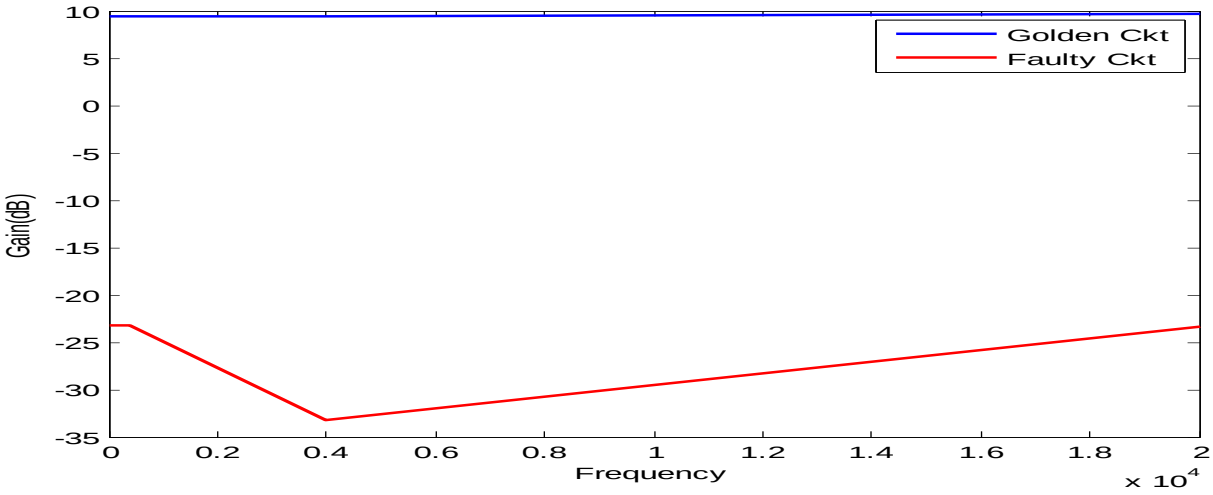


Fig 5.80: Gain Vs Frequency comparison between golden circuit and faulty circuit for M7 stuck on(op-amp)

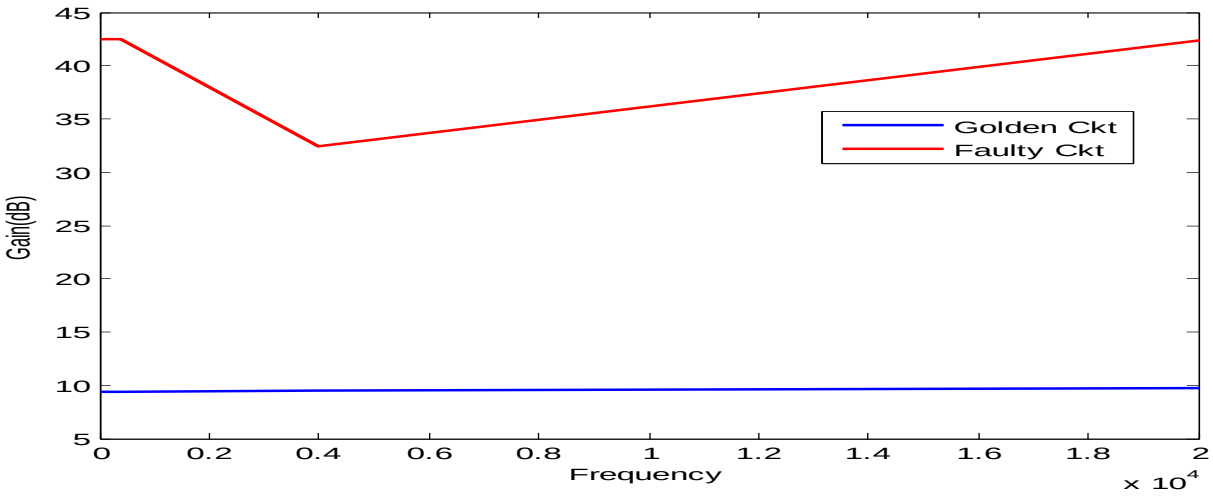


Fig 5.81: Gain Vs Frequency comparison between golden circuit and faulty circuit for M8 stuck on(op-amp)

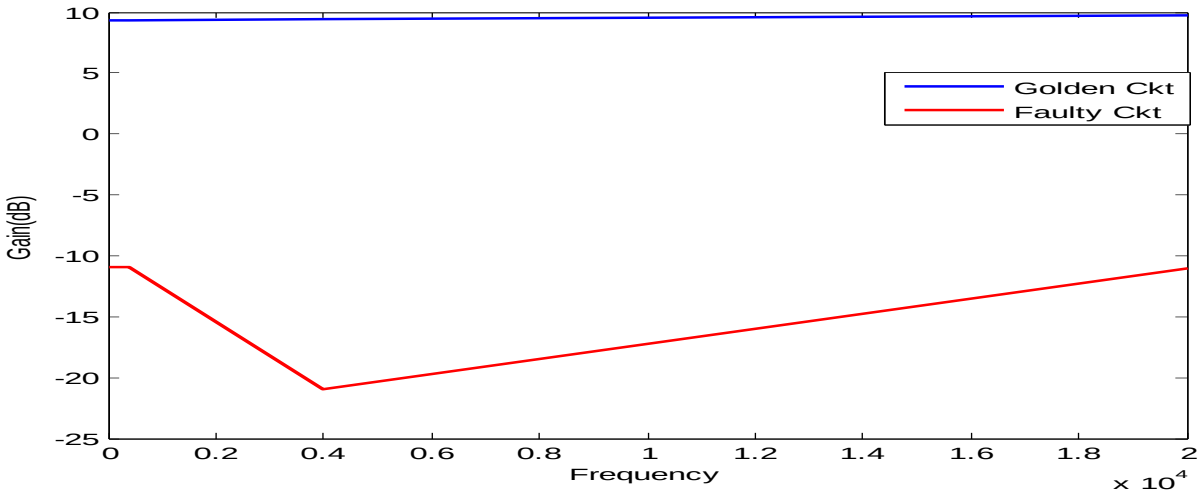


Fig 5.82: Gain Vs Frequency comparison between golden circuit and faulty circuit for M9 stuck on(op-amp)

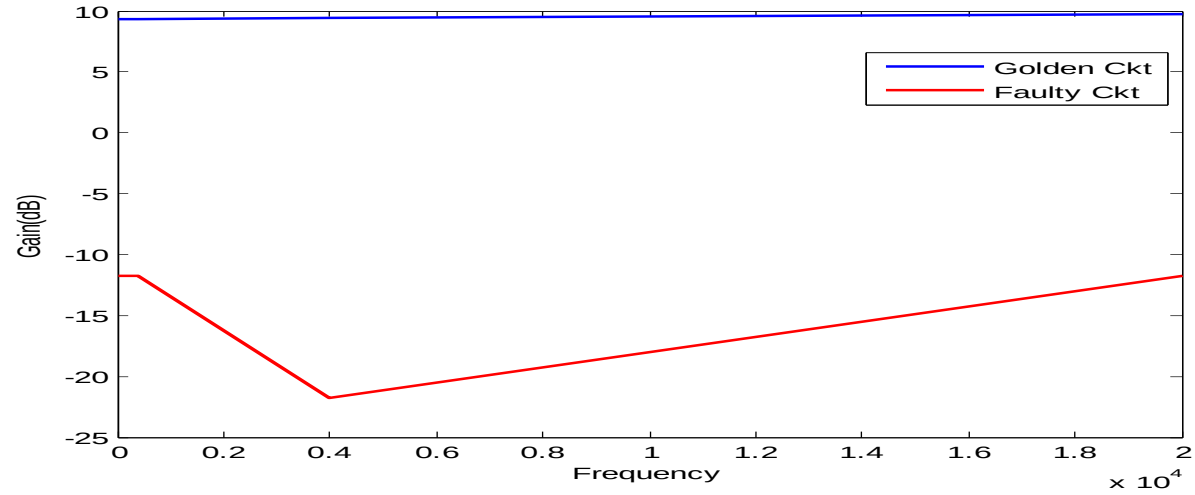


Fig 5.83: Gain Vs Frequency comparison between golden circuit and faulty circuit for M10 stuck on(op-amp)

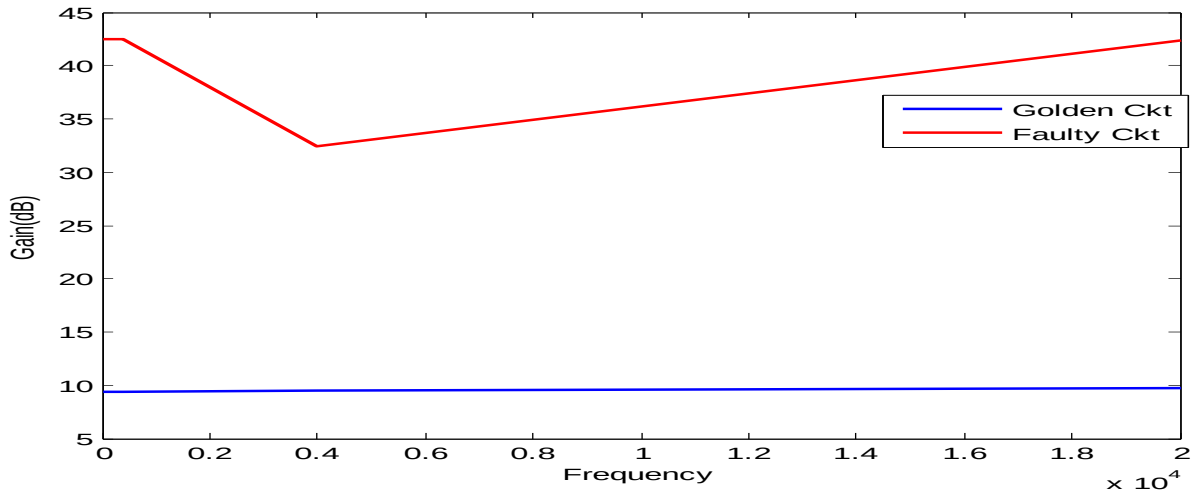


Fig 5.84: Gain Vs Frequency comparison between golden circuit and faulty circuit for M11 stuck on(op-amp)

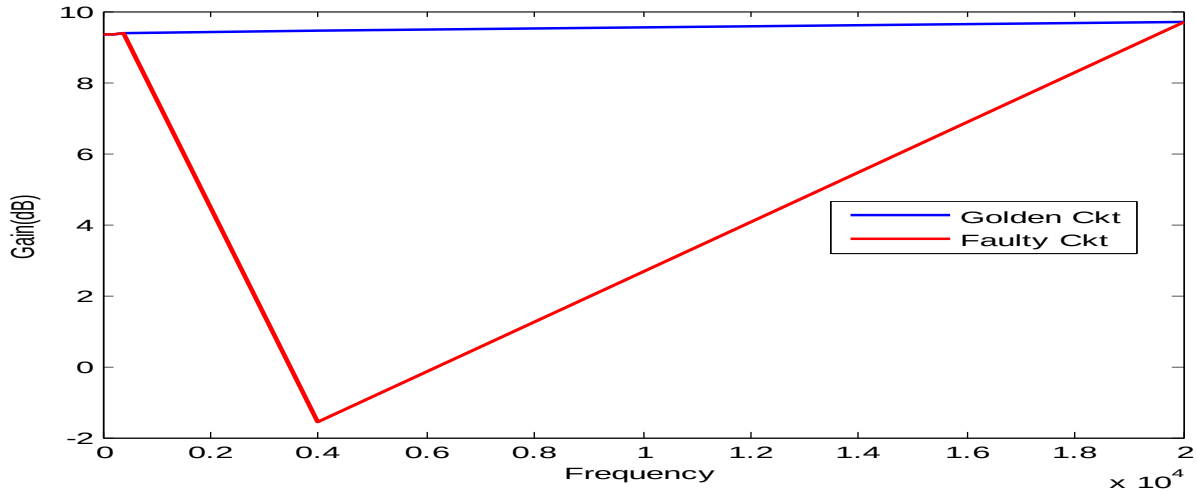


Fig 5.85: Gain Vs Frequency comparison between golden circuit and faulty circuit for M12 stuck on(op-amp)

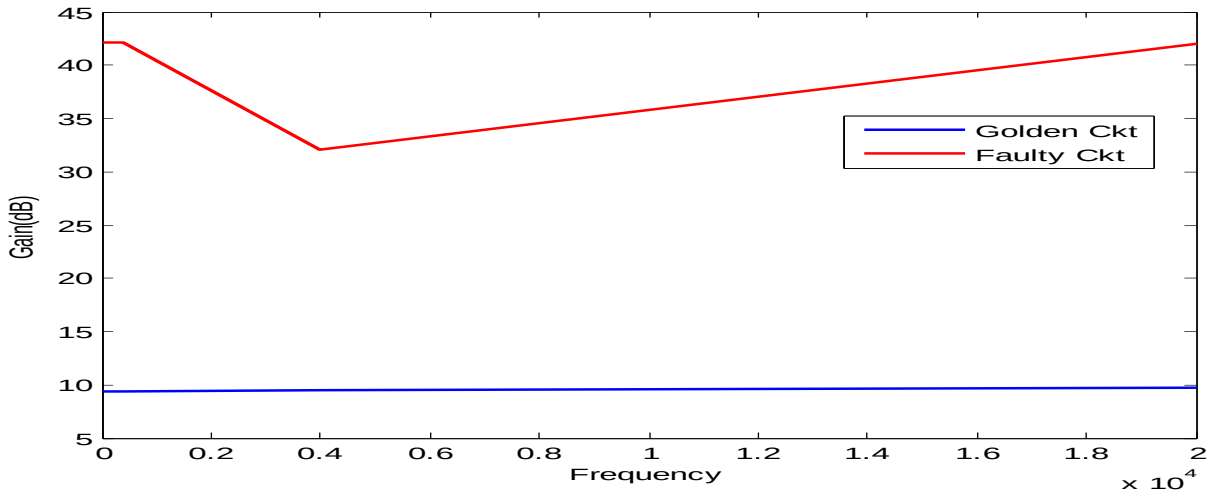


Fig 5.86: Gain Vs Frequency comparison between golden circuit and faulty circuit for M13 stuck on(op-amp)

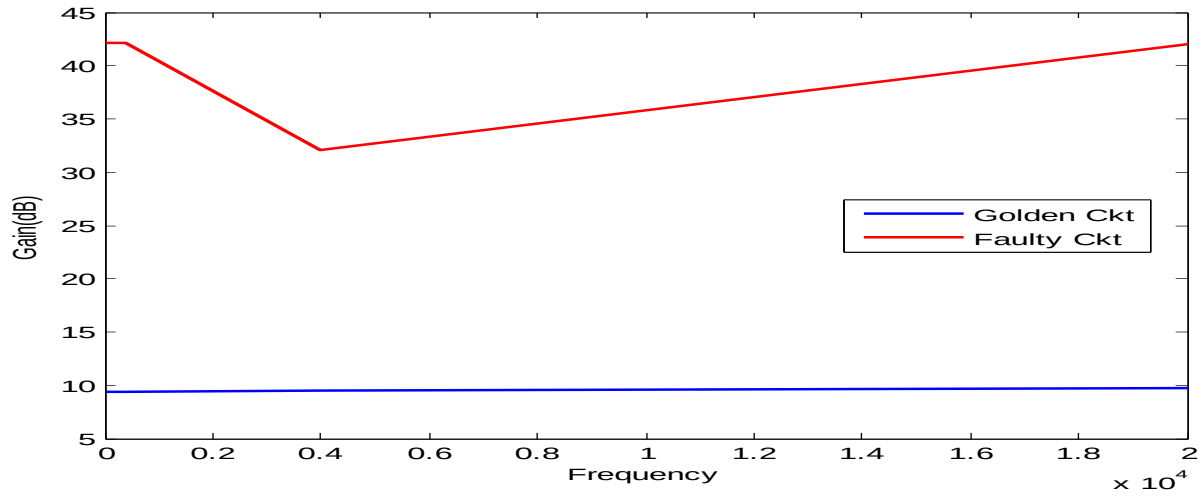


Fig 5.87: Gain Vs Frequency comparison between golden circuit and faulty circuit for M14 stuck on(op-amp)

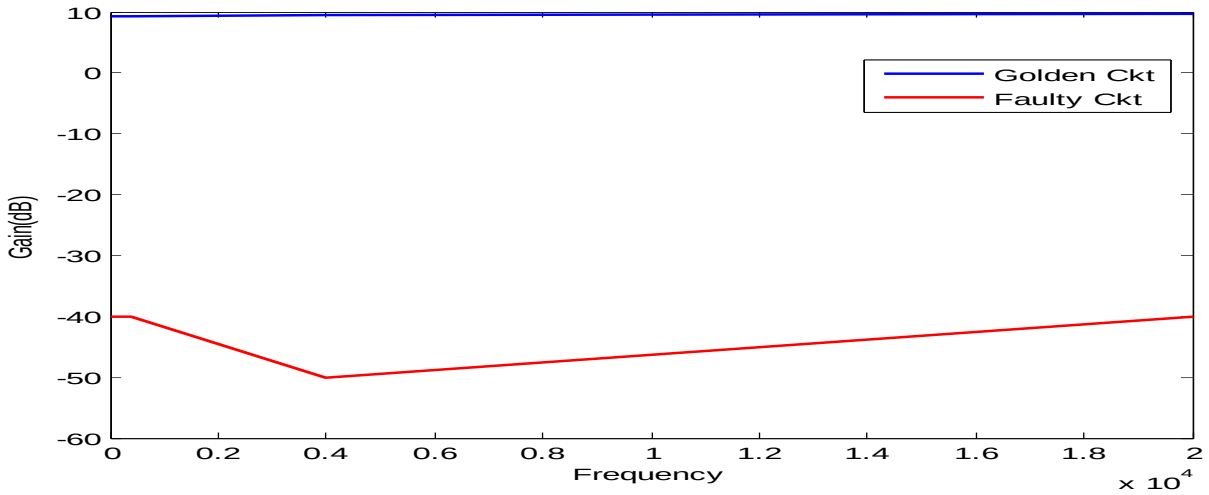


Fig 5.88: Gain Vs Frequency comparison between golden circuit and faulty circuit for M15 stuck on(op-amp)

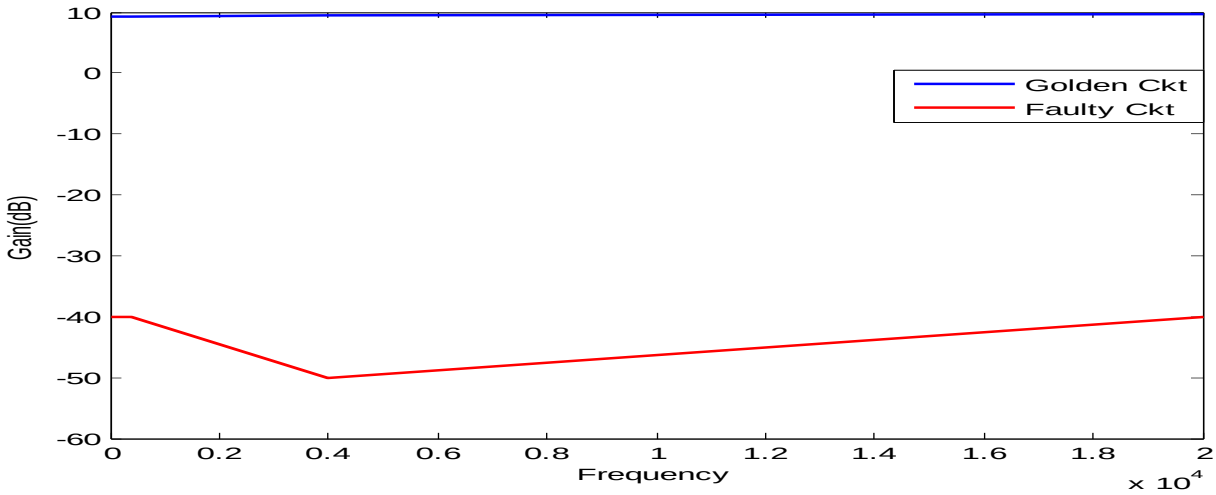


Fig 5.89: Gain Vs Frequency comparison between golden circuit and faulty circuit for M16 stuck on(op-amp)

Table 5.10: Stuck open Fault of MOSFETs in op-amp

Fault name	RMS Gain Error (dB)
M1 stuck open	19.9047
M2 stuck open	0.0064042
M3 stuck open	2.0681
M4 stuck open	2.7052e-007
M5 stuck open	3.2045
M6 stuck open	4.7391
M7 stuck open	4.2585
M8 stuck open	35.2043
M9 stuck open	33.016
M10 stuck open	30.6398
M11 stuck open	21.2983
M12 stuck open	0.0016596
M13 stuck open	3.5357
M14 stuck open	0.00041471
M15 stuck open	0.14423
M16 stuck open	0.38029

For above Faults, Graphs are given bellow,

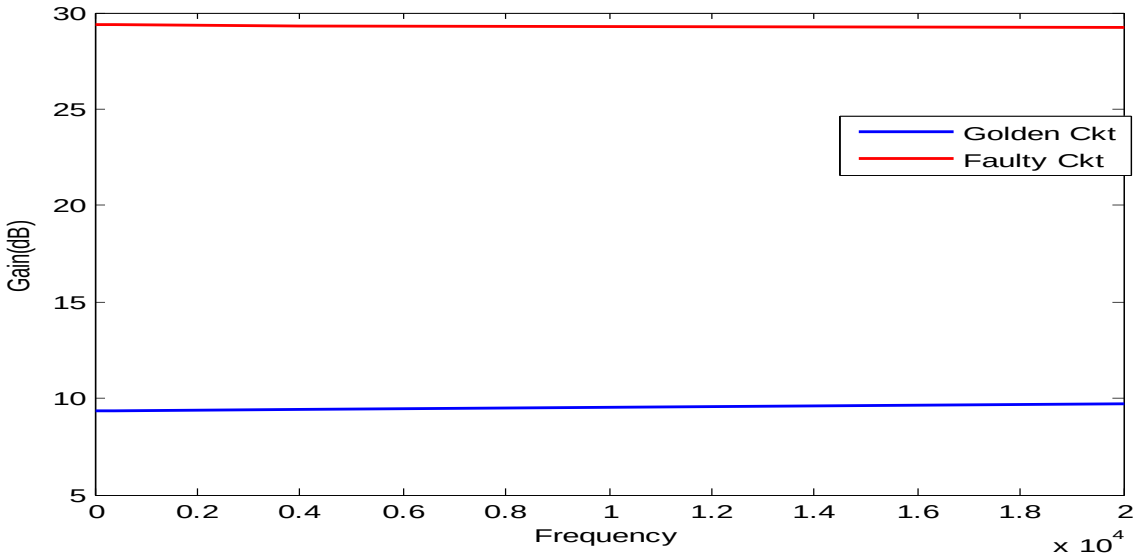


Fig 5.90: Gain Vs Frequency comparison between golden circuit and faulty circuit for M1 stuck open(op-amp)

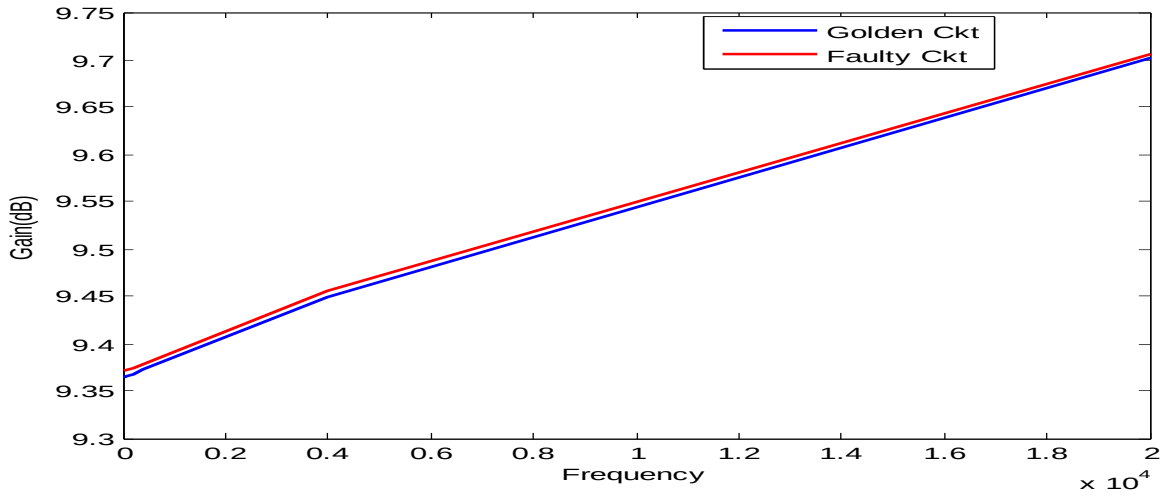


Fig 5.91: Gain Vs Frequency comparison between golden circuit and faulty circuit for M2 stuck open(op-amp)

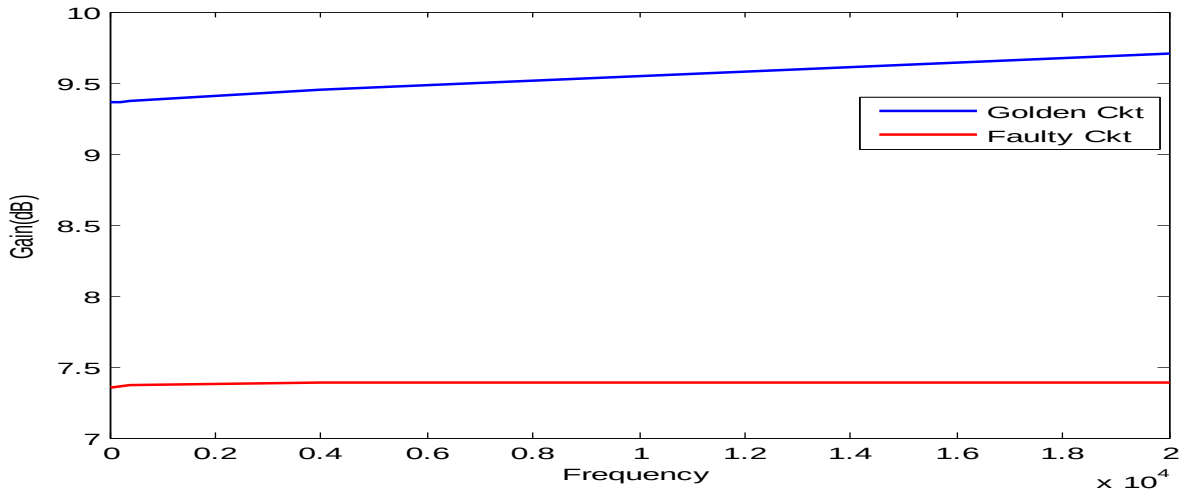


Fig 5.92: Gain Vs Frequency comparison between golden circuit and faulty circuit for M3 stuck open (op-amp)

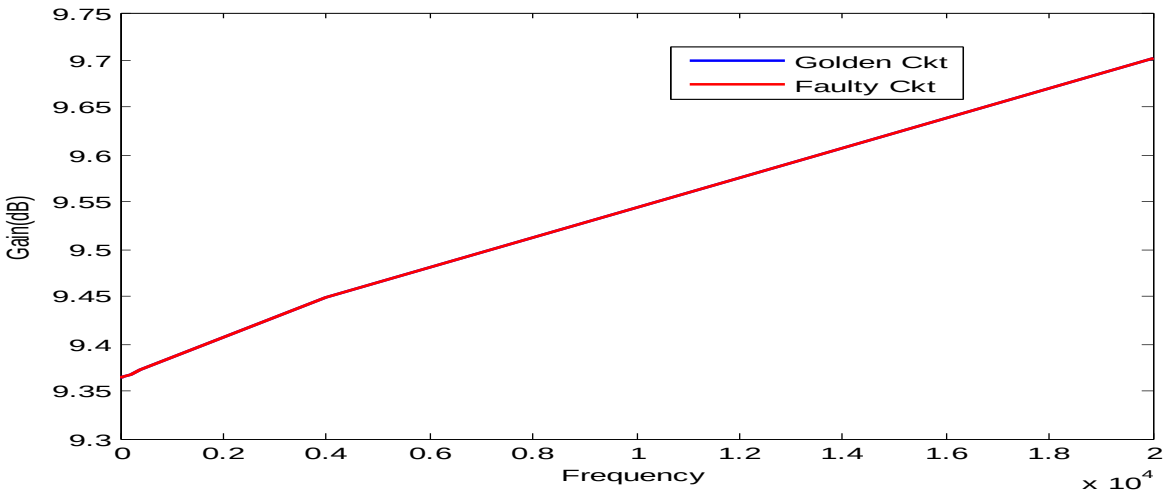


Fig 5.93: Gain Vs Frequency comparison between golden circuit and faulty circuit for M4 stuck open (op-amp)

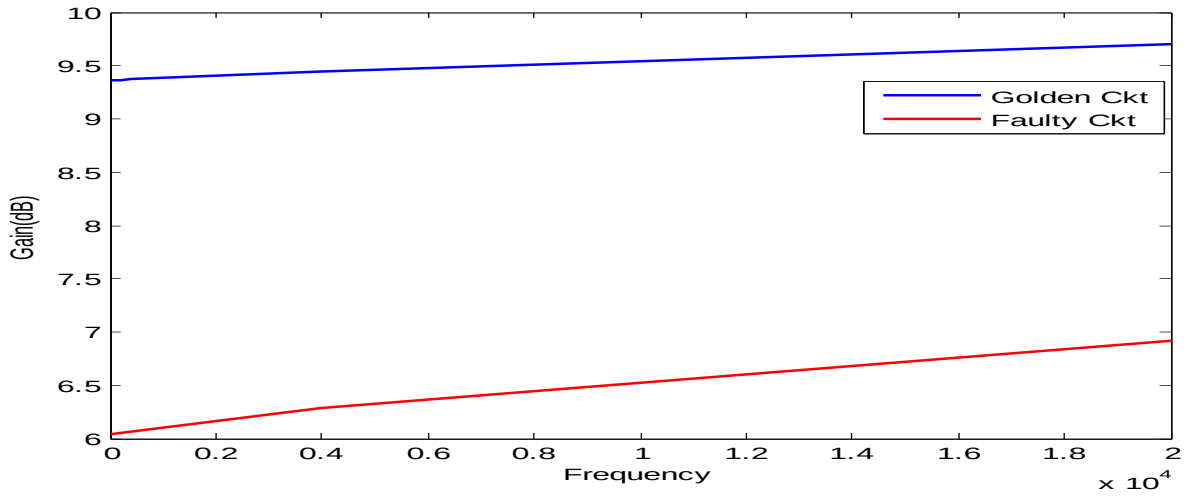


Fig 5.94: Gain Vs Frequency comparison between golden circuit and faulty circuit for M5 stuck open (op-amp)

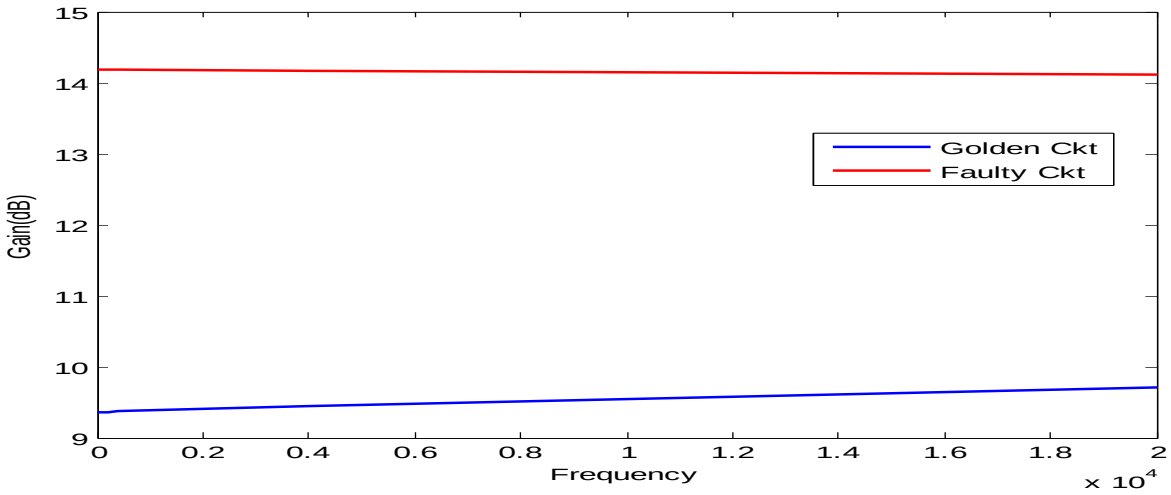


Fig 5.95: Gain Vs Frequency comparison between golden circuit and faulty circuit for M6 stuck open (op-amp)

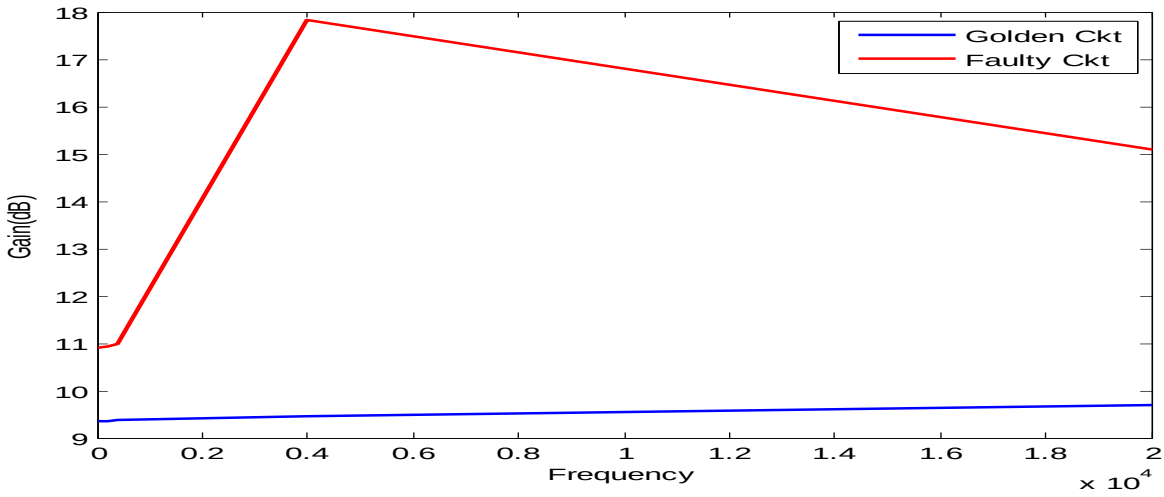


Fig 5.96: Gain Vs Frequency comparison between golden circuit and faulty circuit for M7 stuck open (op-amp)

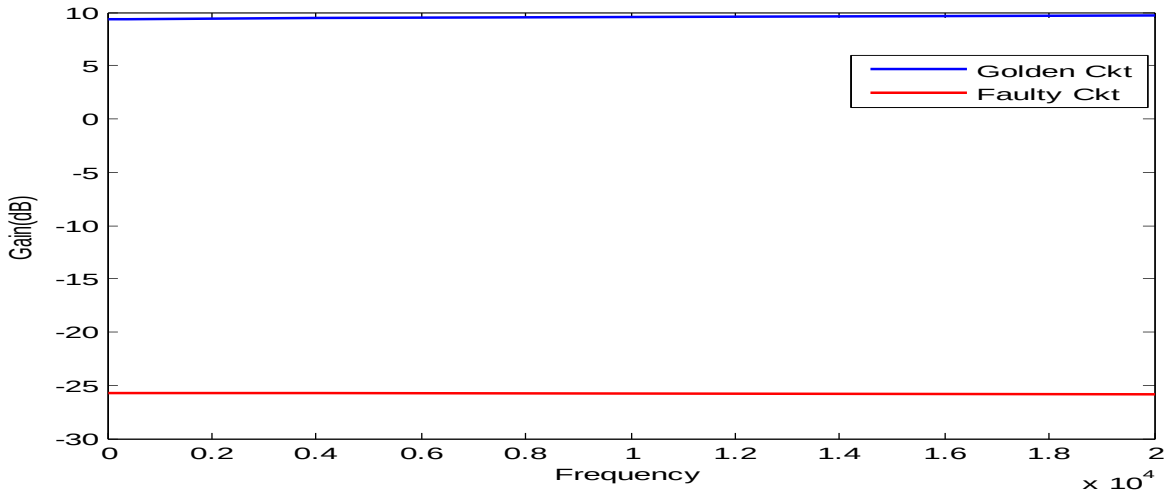


Fig 5.97: Gain Vs Frequency comparison between golden circuit and faulty circuit for M8 stuck open (op-amp)

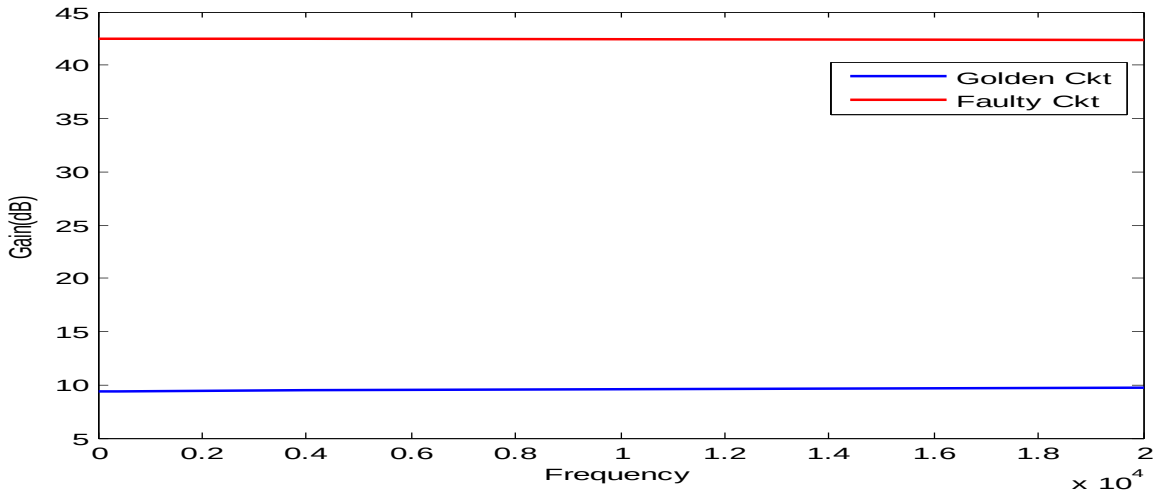


Fig 5.98: Gain Vs Frequency comparison between golden circuit and faulty circuit for M9 stuck open (op-amp)

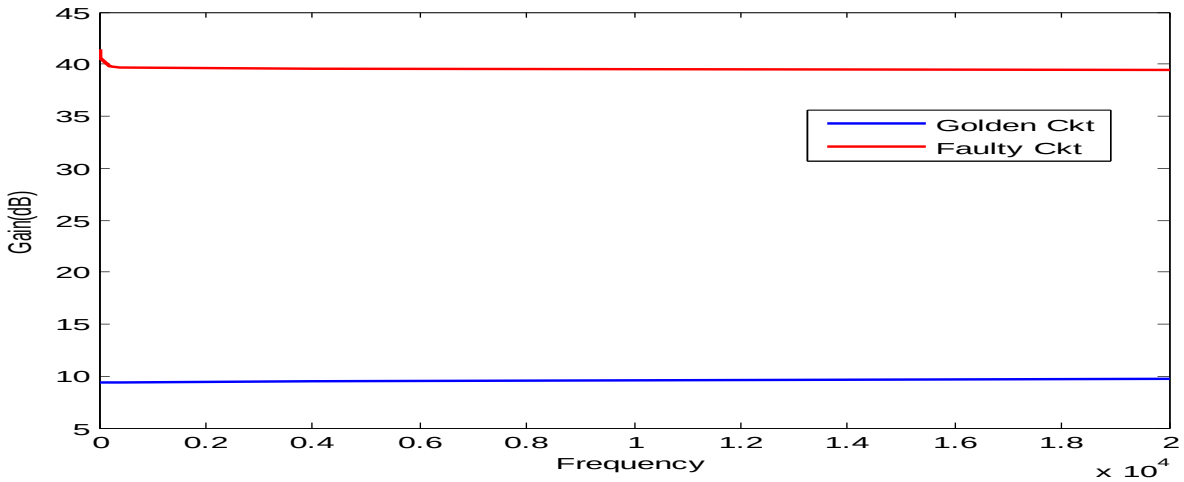


Fig 5.99: Gain Vs Frequency comparison between golden circuit and faulty circuit for M10 stuck open (op-amp)

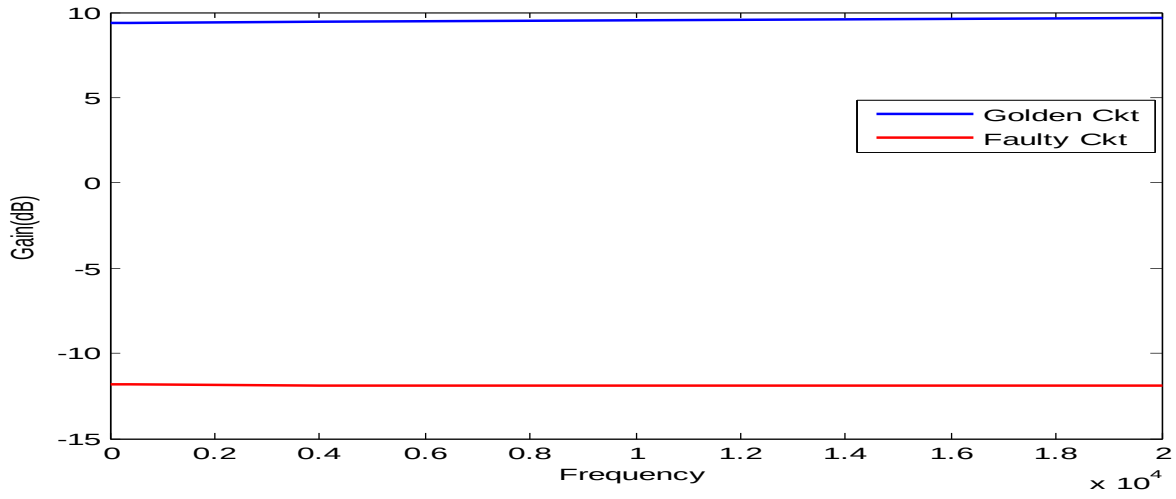


Fig 5.100: Gain Vs Frequency comparison between golden circuit and faulty circuit for M11 stuck open (op-amp)

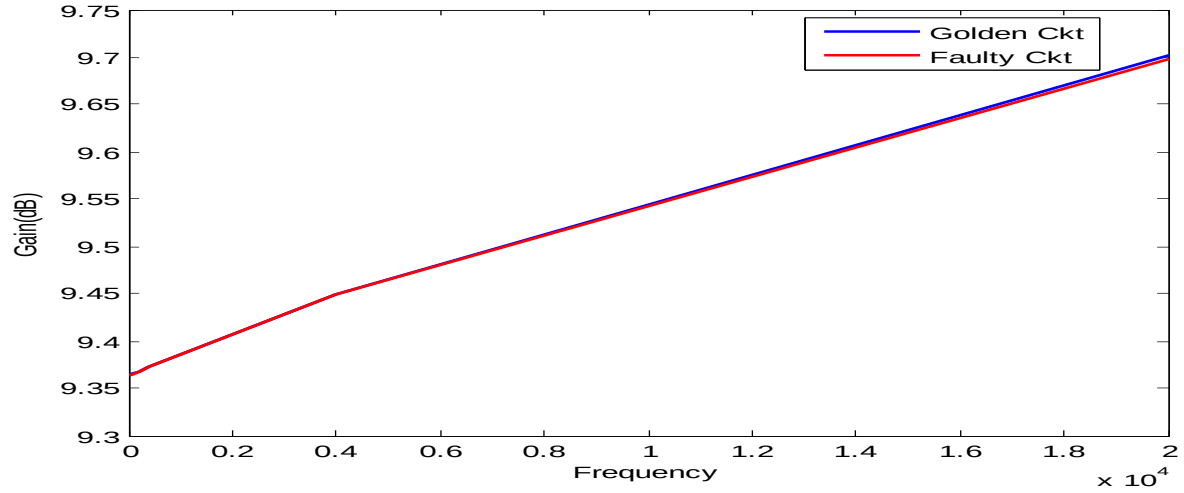


Fig 5.101: Gain Vs Frequency comparison between golden circuit and faulty circuit for M12 stuck open (op-amp)

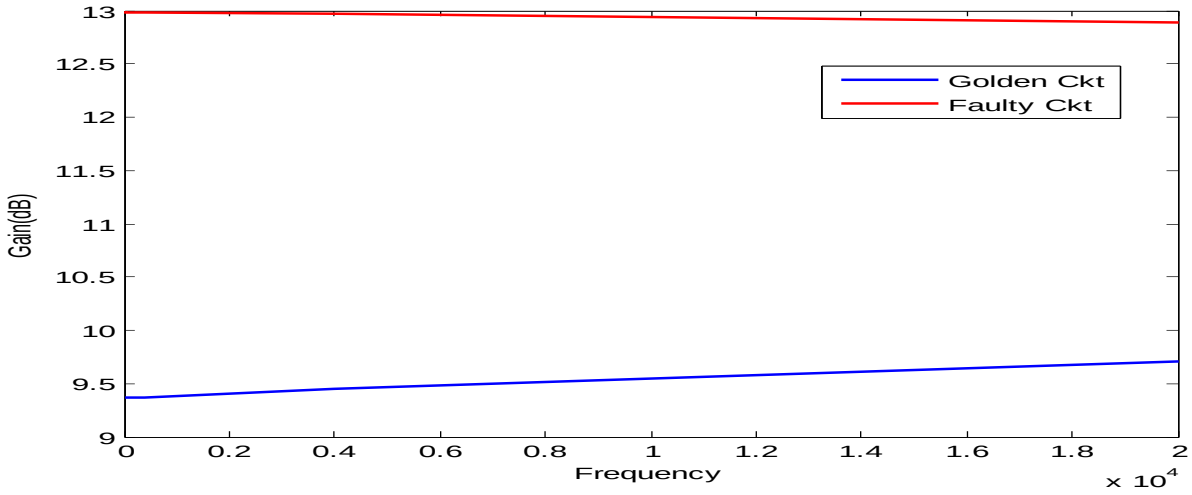


Fig 5.102: Gain Vs Frequency comparison between golden circuit and faulty circuit for M13 stuck open (op-amp)

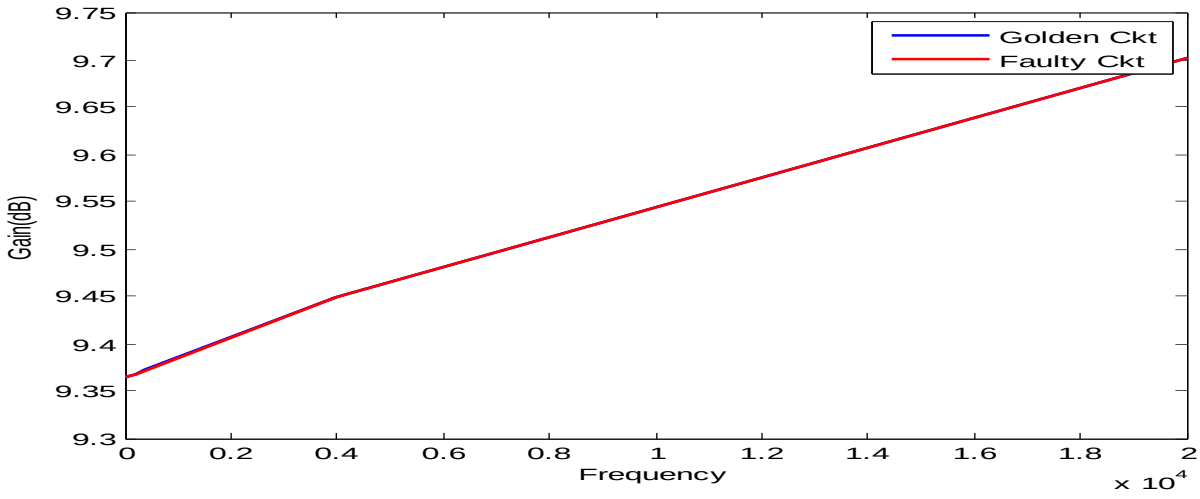


Fig 5.103: Gain Vs Frequency comparison between golden circuit and faulty circuit for M14 stuck open (op-amp)

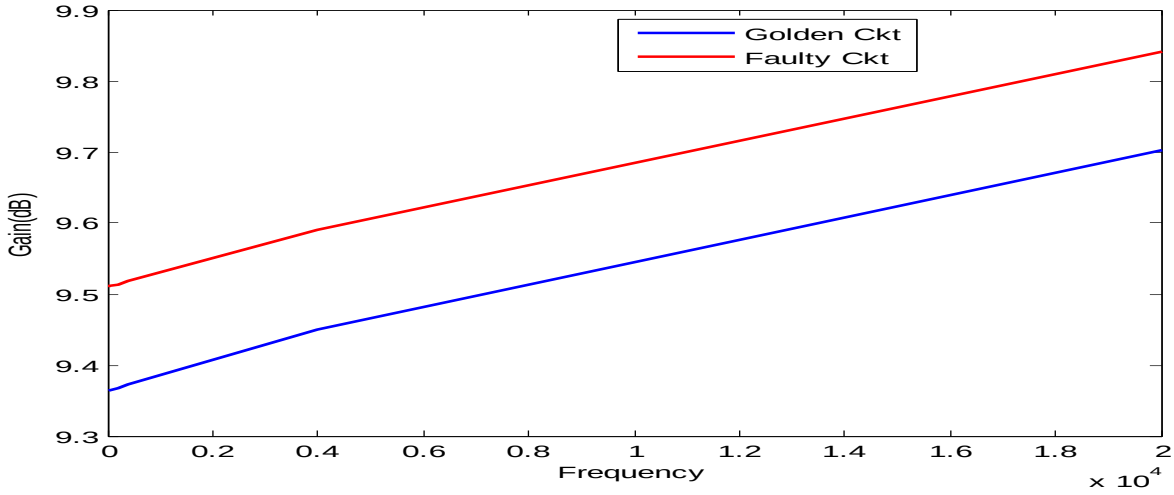


Fig 5.104: Gain Vs Frequency comparison between golden circuit and faulty circuit for M15 stuck open (op-amp)

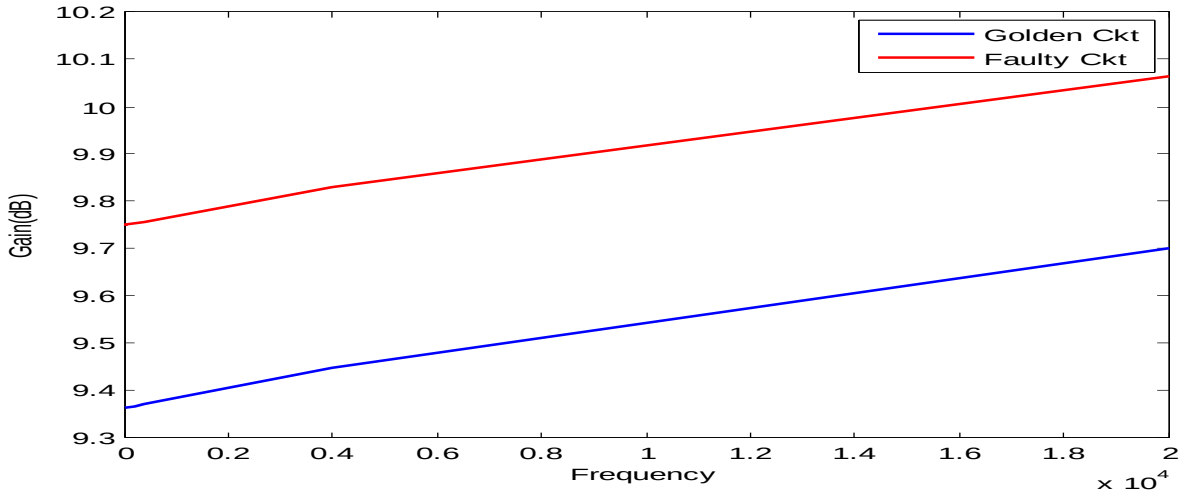


Fig 5.105: Gain Vs Frequency comparison between golden circuit and faulty circuit for M16 stuck open (op-amp)

Table 5.11: Open & short fault for Rb in op-amp

Fault name	RMS Gain(DB)
Rb open	1.1259
Rb short	13.0266

For above Faults, Graphs are given bellow,

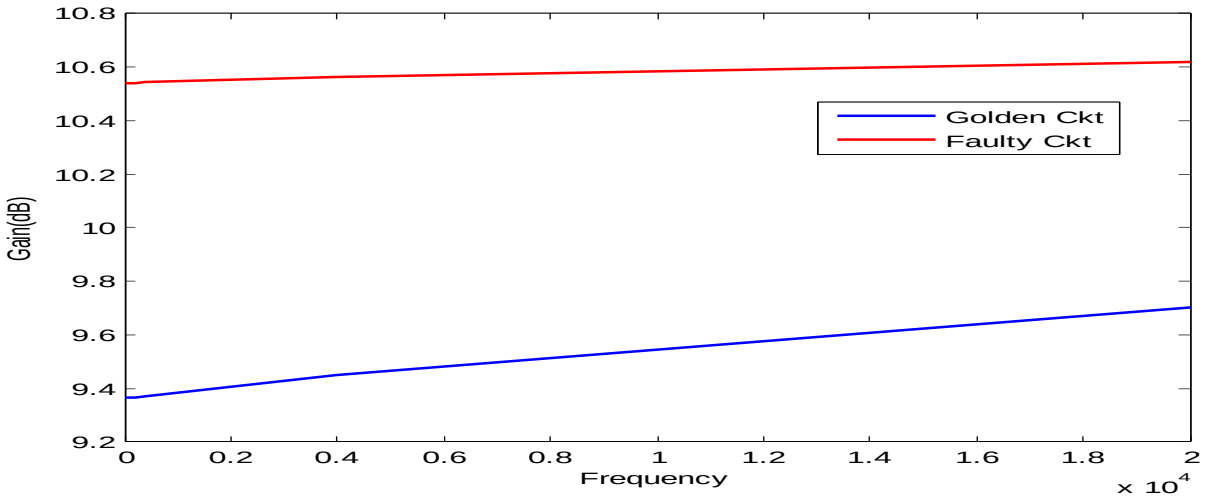


Fig 5.106: Gain Vs Frequency comparison between golden circuit and faulty circuit for Rb open (op-amp)

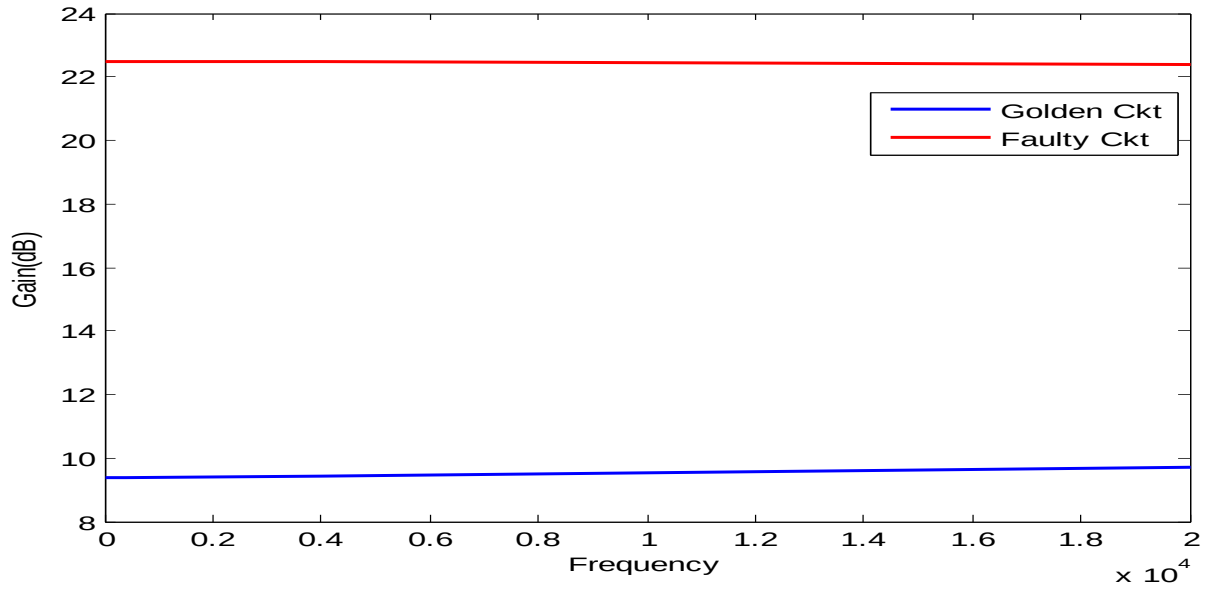


Fig 5.107: Gain Vs Frequency comparison between golden circuit and faulty circuit for Rb short (op-amp)

Table 5.12: Open & short fault for Cc in op-amp

Fault name	RMS Gain Error (DB)
Cc Short	9.3189
Cc open	0.0019633

For above Faults, Graphs are given bellow,

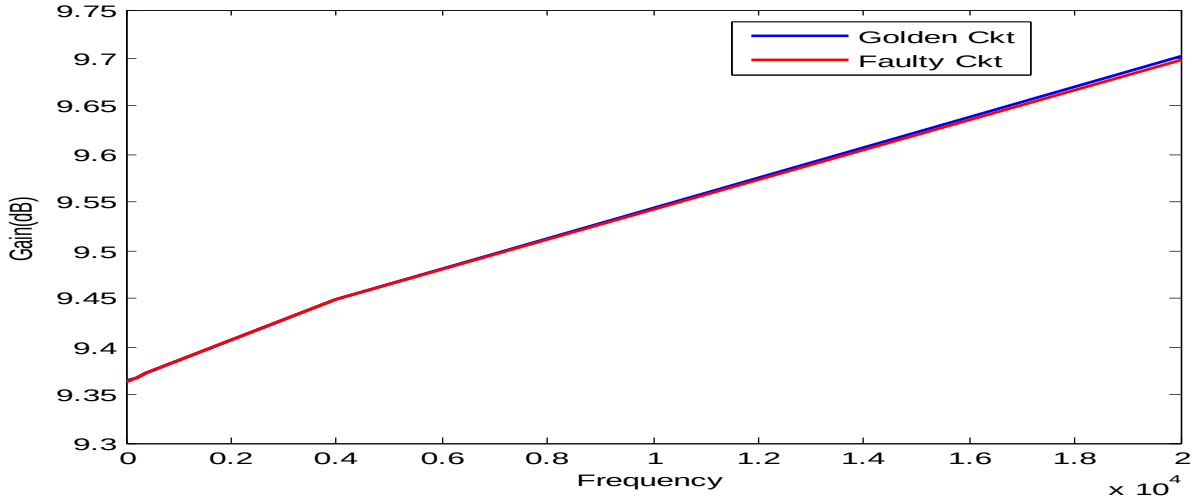


Fig 5.108: Gain Vs Frequency comparison between golden circuit and faulty circuit for Cc stuck open (op-amp)

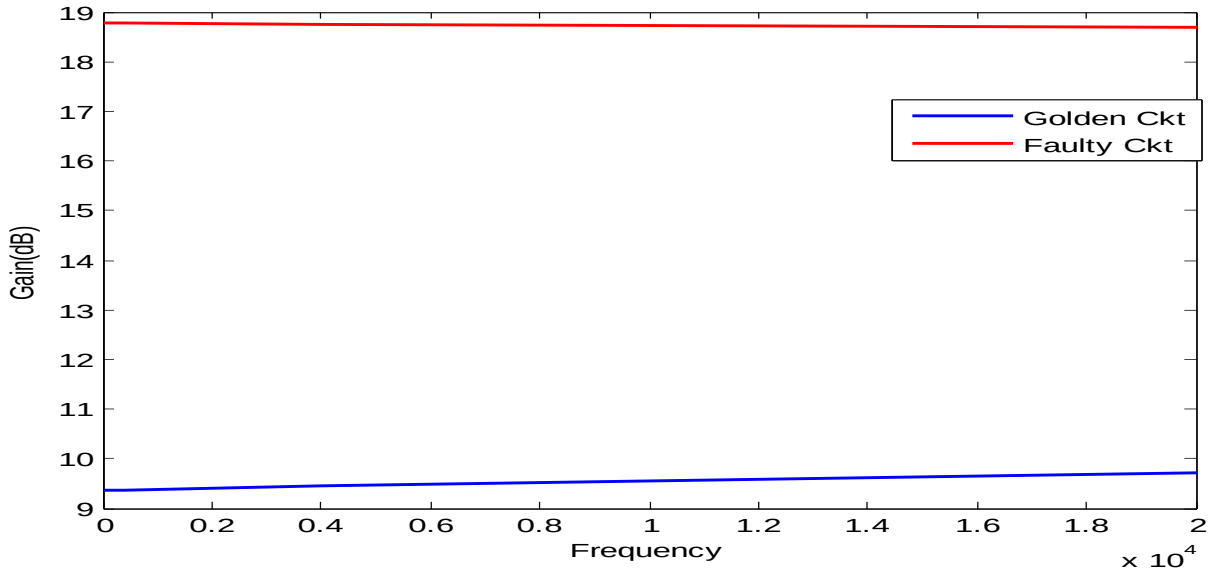


Fig 5.109: Gain Vs Frequency comparison between golden circuit and faulty circuit for Cc stuck on (op-amp)

5.3 Localization & Percentage of detectable faults:

In DAC, total 104 stuck on & stuck open fault will occur. In which,13 of them are negligible.

Table 5.13: for negligible faults

Negligible fault	Fault name
For stuck open	M1, M3, M5,M7,M9, M11,M13,M15, M2(op-amp), M4(op-amp), M12(op-amp), M14(op-amp), Cc(op-amp)

So, the no of detectable faults are (104-13) or 91

Delectability of fault in DAC =(91/104)*100%

=87.5%

So, 87.5% of faults are detectable in DAC.

From table 3.2, it is seen that except opamp1 (100% fault detectable), all benchmark circuit fault detection (in percentage) is less than our observed fault detection percentage of digital to analog converter. Our analysis represent that, we have 87.5 % fault detectability, which is very high for a circuit fault detection. So hopefully it is a satisfied value for a simulation analysis.

Localization means tracing the fault to a defective part responsible for the abnormal conditions. The stuck at faults are localized by checking voltage gain in DAC.

from the graph and simulation result, we have different rms voltage gain error for different range. For a certain range, we can also specify the nature of rms voltage gain error respective to fault free circuit. That is, whether it is greater or smaller than fault free circuit in a definite range.

Using rms voltage gain, it could be localized for accuracy. The percentage of localization is smaller, the localization is more accurate.

So we can define,

$$Percentage\ of\ Localization = \frac{No.\ of\ faults\ \ in\ range\ \ x}{Total\ \ n\ faults\ \ \ in\ DAC} * 100\%$$

Table 5.14: Localization of total stuck at faults in DAC

Range for RMS error Gain (dB),x	Fault nature	Fault name	Percentage of localization
0<x<1	Gain Golden> Gain Faulty	M4 Stuck open	(7/104)*100% =6.7307%
		R9 short	
		C2 open	
		R3 open	
		R11 open	
		R13 open	
		M12 stuck open	
	Gain Golden< Gain Faulty	M14 Stuck open	(16/104)*100% =15.3846%
		M6 Stuck open	
		M8 Stuck open	
		M10 Stuck open	
		M16 stuck on	
		R3 short	
		R8 short	
		R10 short	
		R11 short	
		R12 short	
		R14 short	
		R5 open	
		R7 open	
		R9 open	
		M15 stuck open (opamp)	
		M16 stuck open (opamp)	
1<x<2	Gain Golden> Gain Faulty	M3 stuck on	(7/104)*100% =6.7307%
		M5 Stuck on	
		M7 Stuck on	
		M9 Stuck on	
		R5 short	
		R7 short	
		R14 open	

	Gain Golden< Gain Faulty	M14 stuck on	(6/104)*104% =5.7692%
		R4 short	
		R6 short	
		R13 short	
		R16 open	
		Rb open (opamp)	
2<x<3	Gain Golden> Gain Faulty	M2 Stuck open	(5/104)*100% =4.8076%
		M16 Stuck open	
		M1 Stuck on	
		M11 Stuck on	
		M3 stuck open (opamp)	
	Gain Golden< Gain Faulty	R1 open	(2/104)*100% =1.9230%
		R15 open	
3<x<4	Gain Golden> Gain Faulty	M13 Stuck on	(4/104)*100% =3.8461%
		R16 short	
		R12 open	
		M5 stuck open (opamp)	
	Gain Golden< Gain Faulty	M12 Stuck on	(5/104)*100% =4.8076%
		R2 short	
		R15 short	
		M2 stuck on (opamp)	
		M13 stuck open(opamp)	
4<x<5	Gain Golden> Gain Faulty	M1 stuck on(opamp)	(2/104)*100% =1.9230%
		M5 stuck on(opamp)	
	Gain Golden< Gain Faulty	R8 open	(7/104)*104% =6.7307%
		R10 open	
		M3 stuck on(opamp)	
		M4 stuck on(opamp)	
		M12 stuck on(opamp)	
		M6stuck open(opamp)	
		M7 stuck open(opamp)	
5<x<6	Gain Golden> Gain Faulty	M6 stuck on (opamp)	(2/104)*100% =1.9230%
		R6 open	
	Gain Golden< Gain Faulty	M10 Stuck on	(1/104)*100% =0.9615%
x=6.631	Gain Golden> Gain Faulty	R4 open	(1/104)*100% =0.9615%
x=7.8275	Gain Golden< Gain Faulty	M8 Stuck on	(1/104)*100% =0.9615%
x=8.1128	Gain Golden> Gain Faulty	M15 Stuck on	(1/104)*100% =0.9615%
x=9.3189	Gain Golden< Gain Faulty	Cc short (opamp)	(1/104)*100% =0.9615%
x=10.5566	Gain Golden> Gain	R2 open	(1/104)*100%

	Faulty		=0.9615%
x=11.0337	Gain Golden< Gain Faulty	M6 Stuck on	(1/104)*100% =0.9615%
x=13.0266	Gain Golden< Gain Faulty	Rb short (opamp)	(1/104)*100% =0.9615%
x=15.0909	Gain Golden< Gain Faulty	M4 Stuck on	(1/104)*100% =0.9615%
x=18.553	Gain Golden> Gain Faulty	r short	(2/104)*100% =1.9230%
		C2 short	
19<x<20	Gain Golden> Gain Faulty	M2 Stuck on	(1/104)*100% =0.9615%
	Gain Golden< Gain Faulty	M1stuck open(opamp)	(1/104)*100% =0.9615%
x=21.2983	Gain Golden> Gain Faulty	M11 stuck open(opamp)	(1/104)*100% =0.9615%
x=22.3704	Gain Golden> Gain Faulty	M9 stuck on (opamp)	(1/104)*100% =0.9615%
23<x<24	Gain Golden< Gain Faulty	R1 short	(2/104)*100% =1.9230%
		M10 stuck on (opamp)	
x=30.6398	Gain Golden< Gain Faulty	M10 stuck open(opamp)	(1/104)*100% =0.9615%
31<x<32	Gain Golden< Gain Faulty	M8 stuck on(opamp)	(4/104)*100% =3.8461%
		M11 stuck on(opamp)	
		M13 stuck on(opamp)	
		M14 stuck on(opamp)	
33<x<34	Gain Golden< Gain Faulty	R open	(2/104)*100% =1.9230%
		M9 stuck open(opamp)	
x=34.5434	Gain Golden> Gain Faulty	M7stuck on(opamp)	(1/104)*100% =0.9615%
x=35.2043	Gain Golden> Gain Faulty	M8 stuck open(opamp)	(1/104)*100% =0.9615%
51<x<52	Gain Golden> Gain Faulty	M15 stuck on(opamp)	(2/104)*100% =1.9230%
		M16 stuck on(opamp)	

From the above Table, we can finally specify the fault nature and location clearly.

Here, x is the definite range for definite no of faults with definite nature. If we have one fault for a definite range x, percentage of localization will be 0.9615% which is our desired value. The no of faults in range x is smaller, the percentage of localization will be smaller that makes our fault detection more accurate.

So, it is clear that, the Percentage of Localization increase with respect to the number of faults.

Chapter 6

Conclusion

As the demand for electronic circuits and systems in modern technology increases, both their scale and complexity grow rapidly. The phenomenal development of electronic systems would not have been possible without the advances in large scale and very large scale integration (LSI/VLSI) in semiconductor circuit technologies. Therefore, in order to achieve the desired quality, fault testing is of the utmost importance.

In view of this, we have proposed on the single stuck-at fault technique of basic 8 bit DA converter, which not only localizes but also aims for identification of the fault. Such identification helps correcting any faulty in the circuit. This thesis reports simulation results that have information & nature of deviation of the gain waveform in between fault free circuit & faulty circuit.

As we saw previous work, it has been published about another benchmark circuits with both gain voltage and phase. It for Digital to analog converter we have faced some problems for finding out the gain voltage because of digital input and analog output. Because of different input and output property, it was so much difficult to find out the gain voltage of digital to analog converter.

There an another important part of Digital to analog converter is two stage CMOS operational amplifier, which has a different and complicated current flow for each Nmos and Pmos for their structure. It also makes our thesis a bit complicated for us.

In our thesis work, we see that, every stuck at fault is changing the input voltage with respect to output voltage. It makes the voltage gain error variable. Every digital input is changing for a definite stuck at fault and that impact is on the analog output voltage. It is tough to analyze these variable digital input and analog output for classify the voltage gain.

In this thesis, we use two computer programs,

1. Hspice
2. Matlab

Hspise is used for attaining the value of digital to analog converter voltage gain for different frequencies. There are six frequencies are used for accurate voltage gain. For different frequencies and different transient analysis, we obtained different output voltage and voltage gain. The simulation results from Hspice analysis are use in matlab for the root mean square

voltage gain of faulty digital to analog converter and fault free digital to analog converter. From the graph and matlab simulation we get the root mean square voltage gain error between faulty and fault free circuit of digital to analog converter.

It is a Nobel work that hasn't done before. From this analysis, it is 87.5% faults can be detected in digital to analog circuit. Furthermore it can be helpful work for detecting the phase error of digital to analog converter and more.

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APPENDIX

Circuit configuration of two stage CMOS operation amplifier used in 8 bit digital to analog converter:

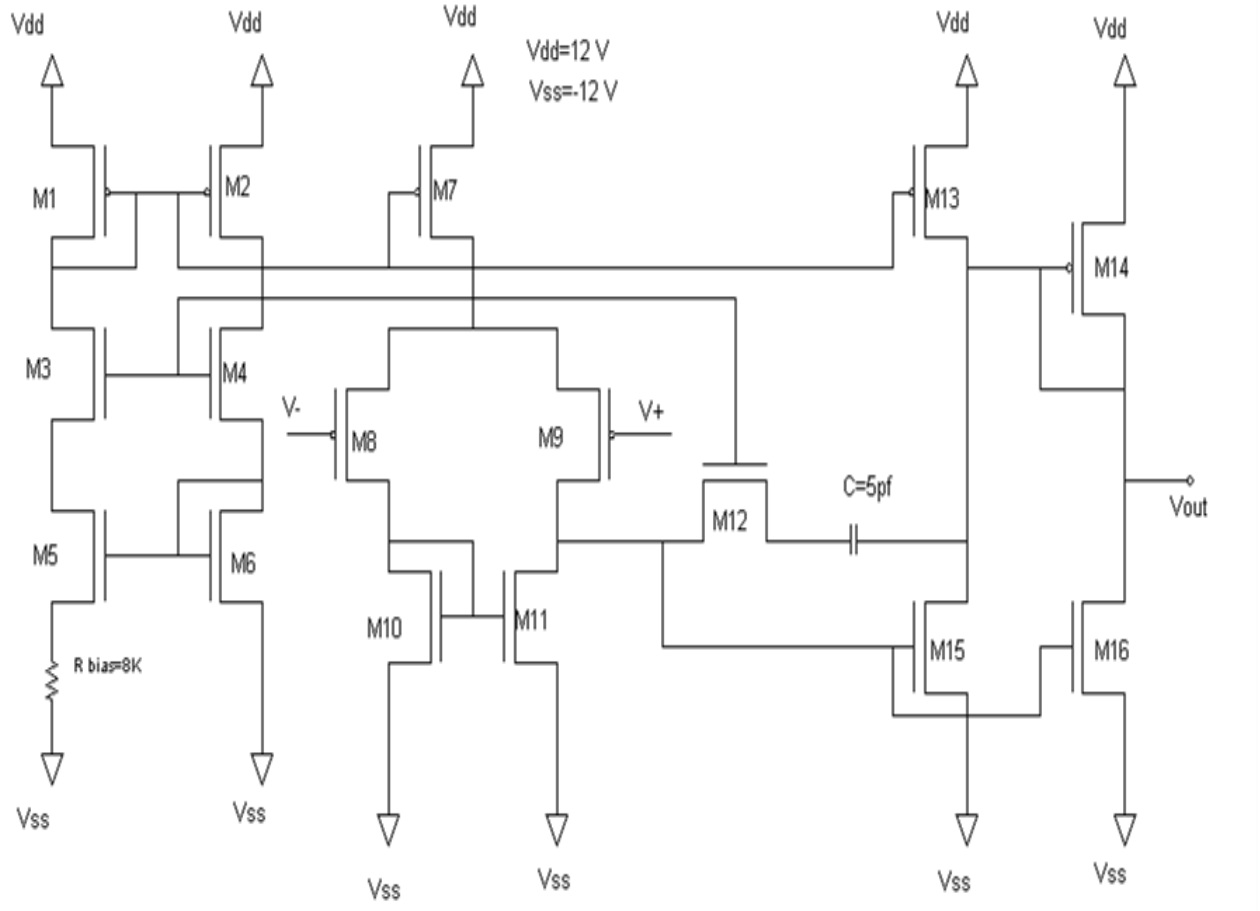

Fig: Two stage CMOS operational amplifier

Netlist of 8-bit Digital-to-Analog Converter:

```
.SUBCKT opamp5 10 9 14
Rse1 2 200 1
Rpl1 200 1 100meg
M1 200 200 1 1 pfet l=2.0u w=25.0u
Rse2 3 300 1
Rpl2 300 1 100meg
M2 300 2 1 1 pfet l=2.0u w=25.0u
Rse3 2 201 1
Rpl3 201 4 100meg
M3 201 3 4 7 nfet l=2.0u w=25.0u
Rse4 3 301 1
Rpl4 301 5 100meg
M4 300 300 5 7 nfet l=2.0u w=25.0u
Rse5 4 400 1
Rpl5 400 6 100meg
M5 400 5 6 7 nfet l=2.0u w=100.0u
Rse6 5 500 1
Rpl6 500 7 100meg
M6 500 500 7 7 nfet l=2.0u w=25.0u
Rse7 8 800 1
Rpl7 800 1 100meg
M7 800 2 1 1 pfet l=2.0u w=300.0u
Rse8 11 111 1
Rpl8 111 8 100meg
M8 111 9 8 1 pfet l=2.0u w=300.0u
Rse9 12 112 1
Rpl9 112 8 100meg
M9 112 10 8 1 pfet l=2.0u w=300.0u
Rse10 11 211 1
Rpl10 211 7 100meg
M10 211 11 7 7 nfet l=2.0u w=150.0u
Rse11 12 212 1
Rpl11 212 7 100meg
M11 212 11 7 7 nfet l=2.0u w=150.0u
Rse12 12 312 1
Rpl12 312 13 100meg
M12 312 3 13 7 nfet l=2.0u w=100.0u
Rse13 14 114 1
```

```
Rpl13 114 1 100meg
M13 114 2 1 1 pfet l=2.0u w=300.0u
Rse14 1 100 1
Rpl14 100 14 100meg
M14 100 14 14 7 nfet l=2.0u w=500.0u
Rse15 14 214 1
Rpl15 214 7 100meg
M15 214 12 7 7 nfet l=2.0u w=300.0u
Rse16 14 314 1
Rpl16 314 7 100meg
M16 314 12 7 7 nfet l=2.0u w=500.0u
Rb 6 7 8e03
rccse 13 139 1
rccpl 139 14 100meg
Cc 139 14 5pf
Vdd 1 0 12
Vss 7 0 dc 0
.MODEL nfet NMOS LEVEL=2 PHI=0.700000 TOX=3.8200E-08 XJ=0.200000U TPG=1
+ VTO=0.7745 DELTA=3.9840E+00 LD=2.0440E-07 KP=6.6776E-05
+ UO=738.7 UEXP=1.1650E-01 UCRIT=7.4320E+03 RSH=1.0230E-01
+ GAMMA=0.5269 NSUB=6.8350E+15 NFS=9.1000E+10 VMAX=5.2230E+04
+ LAMBDA=3.5390E-02 CGDO=2.7716E-10 CGSO=2.7716E-10
+ CGBO=3.4582E-10 CJ=1.25E-04 MJ=0.663 CJSW=5.63E-10
+ MJSW=0.300 PB=0.60
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.700000 TOX=3.8200E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9353 DELTA=3.0110E+00 LD=2.1590E-07 KP=1.6570E-05
+ UO=183.3 UEXP=2.9090E-01 UCRIT=1.2900E+05 RSH=9.0910E-02
+ GAMMA=0.6894 NSUB=1.1700E+16 NFS=7.1500E+11 VMAX=9.9990E+05
+ LAMBDA=4.6840E-02 CGDO=2.9275E-10 CGSO=2.9275E-10
+ CGBO=4.4235E-10 CJ=3.18E-04 MJ=0.600 CJSW=4.50E-10
+ MJSW=0.275 PB=0.90
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -5.7900E-07
.ENDS

Rmse1 16 161 1
Rmpl1 161 0 100meg
M1 161 17 0 27 pfet l=2.0u w=10.0u
Rmse2 16 162 1
```

```
Rmpl2 162 25 100meg
M2 162 17 25 0 nfet l=2.0u w=30.0u
Rmse3 15 151 1
Rmpl3 151 0 100meg
M3 151 18 0 27 pfet l=2.0u w=10.0u
Rmse4 15 152 1
Rmpl4 152 25 100meg
M4 152 18 25 0 nfet l=2.0u w=30.0u
Rmse5 14 141 1
Rmpl5 141 0 100meg
M5 141 19 0 27 pfet l=2.0u w=10.0u
Rmse6 14 142 1
Rmpl6 142 25 100meg
M6 142 19 25 0 nfet l=2.0u w=30.0u
Rmse7 13 131 1
Rmpl7 131 0 100meg
M7 131 20 0 27 pfet l=2.0u w=10.0u
Rmse8 13 132 1
Rmpl8 132 25 100meg
M8 132 20 25 0 nfet l=2.0u w=30.0u
Rmse9 12 121 1
Rmpl9 121 0 100meg
M9 121 21 0 27 pfet l=2.0u w=10.0u
Rmse10 12 122 1
Rmpl10 122 25 100meg
M10 122 21 25 0 nfet l=2.0u w=30.0u
Rmse11 11 111 1
Rmpl11 111 0 100meg
M11 111 22 0 27 pfet l=2.0u w=10.0u
Rmse12 11 112 1
Rmpl12 112 25 100meg
M12 112 22 25 0 nfet l=2.0u w=30.0u
Rmse13 10 101 1
Rmpl13 101 0 100meg
M13 101 23 0 27 pfet l=2.0u w=10.0u
Rmse14 10 102 1
Rmpl14 102 25 100meg
M14 102 23 25 0 nfet l=2.0u w=30.0u
Rmse15 9 91 1
Rmpl15 91 0 100meg
```

```
M15 91 24 0 27 pfet l=2.0u w=10.0u
Rmse16 9 92 1
Rmpl16 92 25 100meg
M16 92 24 25 0 nfet l=2.0u w=30.0u
R1 1 16 80e03
R2 1 2 40e03
R3 2 15 80e03
R4 2 3 40e03
R5 3 14 80e03
R6 3 4 40e03
R7 4 13 80e03
R8 4 5 40e03
R9 5 12 80e03
R10 5 6 40e03
R11 6 11 80e03
R12 6 7 40e03
R13 7 10 80e03
R14 7 8 40e03
R15 8 9 80e03
R16 8 0 80e03

Vdd 27 0 5
Vref 1 0 -5
v1 24 0 pwl 100us 0v, 101us 5v, 4700us 5v,  4701us 0v, 5100us 0v
v2 23 0 pwl 100us 0v, 400us 0v, 401us 5v, 4400us 5v, 4401us 0v, 5100us 0v
v3 22 0 pwl 100us 0v, 700us 0v, 701us 5v, 4100us 5v, 4101us 0v, 5100us 0v
v4 21 0 pwl 100us 0v, 1000us 0v, 1001us 5v, 3800us 5v, 3801us 0v, 5100us 0v
v5 20 0 pwl 100us 0v, 1300us 0v, 1301us 5v, 3500us 5v, 3501us 0v, 5100us 0v
v6 19 0 pwl 100us 0v, 1600us 0v, 1601us 5v, 3200us 5v, 3201us 0v, 5100us 0v
v7 18 0 pwl 100us 0v, 1900us 0v, 1901us 5v, 2900us 5v, 2901us 0v, 5100us 0v
v8 17 0 pwl 100us 0v, 2200us 0v, 2201us 5v, 2600us 5v, 2601us 0v, 5100us 0v
X1 0 25 26 opamp5
R 25 26 40e03
rcse 25 255 1
rcpl 255 26 100meg
C2 255 26 15pf
.MODEL nfet NMOS LEVEL=2 PHI=0.700000 TOX=3.8200E-08 XJ=0.200000U TPG=1
+ VTO=0.7745 DELTA=3.9840E+00 LD=2.0440E-07 KP=6.6776E-05
+ UO=738.7 UEXP=1.1650E-01 UCRIT=7.4320E+03 RSH=1.0230E-01
+ GAMMA=0.5269 NSUB=6.8350E+15 NFS=9.1000E+10 VMAX=5.2230E+04
+ LAMBDA=3.5390E-02 CGDO=2.7716E-10 CGSO=2.7716E-10
```

+ CGBO=3.4582E-10 CJ=1.25E-04 MJ=0.663 CJSW=5.63E-10
+ MJSW=0.300 PB=0.60
.MODEL pfet PMOS LEVEL=2 PHI=0.700000 TOX=3.8200E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9353 DELTA=3.0110E+00 LD=2.1590E-07 KP=1.6570E-05
+ UO=183.3 UEXP=2.9090E-01 UCRIT=1.2900E+05 RSH=9.0910E-02
+ GAMMA=0.6894 NSUB=1.1700E+16 NFS=7.1500E+11 VMAX=9.9990E+05
+ LAMBDA=4.6840E-02 CGDO=2.9275E-10 CGSO=2.9275E-10
+ CGBO=4.4235E-10 CJ=3.18E-04 MJ=0.600 CJSW=4.50E-10
+ MJSW=0.275 PB=0.90
.options post=2
.tran 1us 0.550ms
.print v(26)
.end

For different frequency, v1 to v8 time period has been changed. The above code is for 200 HZ frequency.

For 20 HZ frequency the netlist of time period will be,

v1 24 0 pwl 1000us 0v, 1001us 5v, 47000us 5v, 47001us 0v, 51000us 0v
v2 23 0 pwl 1000us 0v, 4000us 0v, 4001us 5v, 44000us 5v, 44001us 0v, 51000us 0v
v3 22 0 pwl 1000us 0v, 7000us 0v, 7001us 5v, 41000us 5v, 41001us 0v, 51000us 0v
v4 21 0 pwl 1000us 0v, 10000us 0v, 10001us 5v, 38000us 5v, 38001us 0v, 51000us 0v
v5 20 0 pwl 1000us 0v, 13000us 0v, 13001us 5v, 35000us 5v, 35001us 0v, 51000us 0v
v6 19 0 pwl 1000us 0v, 16000us 0v, 16001us 5v, 32000us 5v, 32001us 0v, 51000us 0v
v7 18 0 pwl 1000us 0v, 19000us 0v, 19001us 5v, 29000us 5v, 29001us 0v, 51000us 0v
v8 17 0 pwl 1000us 0v, 22000us 0v, 22001us 5v, 26000us 5v, 26001us 0v, 51000us 0v

For 40 HZ frequency the netlist of time period will be,

v1 24 0 pwl 500us 0v, 501us 5v, 23500us 5v, 23501us 0v, 25500us 0v
v2 23 0 pwl 500us 0v, 2000us 0v, 2001us 5v, 22000us 5v, 22001us 0v, 25500us 0v
v3 22 0 pwl 500us 0v, 3500us 0v, 3501us 5v, 20500us 5v, 20501us 0v, 25500us 0v
v4 21 0 pwl 500us 0v, 5000us 0v, 5001us 5v, 19000us 5v, 19001us 0v, 25500us 0v
v5 20 0 pwl 500us 0v, 6500us 0v, 6501us 5v, 17500us 5v, 17501us 0v, 25500us 0v
v6 19 0 pwl 500us 0v, 8000us 0v, 8001us 5v, 16000us 5v, 16001us 0v, 25500us 0v
v7 18 0 pwl 500us 0v, 9500us 0v, 9501us 5v, 14500us 5v, 14501us 0v, 25500us 0v
v8 17 0 pwl 500us 0v, 11000us 0v, 11001us 5v, 13000us 5v, 13001us 0v, 25500us 0v

For 400 HZ frequency the netlist of time period will be,

v1 24 0 pwl 50us 0v, 51us 5v, 2350us 5v, 2351us 0v, 2550us 0v
v2 23 0 pwl 50us 0v, 200us 0v, 201us 5v, 2200us 5v, 2201us 0v, 2550us 0v
v3 22 0 pwl 50us 0v, 350us 0v, 351us 5v, 2050us 5v, 2051us 0v, 2550us 0v
v4 21 0 pwl 50us 0v, 500us 0v, 501us 5v, 1900us 5v, 1901us 0v, 2550us 0v
v5 20 0 pwl 50us 0v, 650us 0v, 651us 5v, 1750us 5v, 1751us 0v, 2550us 0v
v6 19 0 pwl 50us 0v, 800us 0v, 801us 5v, 1600us 5v, 1601us 0v, 2550us 0v
v7 18 0 pwl 50us 0v, 950us 0v, 951us 5v, 1450us 5v, 1451us 0v, 2550us 0v
v8 17 0 pwl 50us 0v, 1100us 0v, 1101us 5v, 1300us 5v, 1301us 0v, 2550us 0v

For 4000 HZ frequency the netlist of time period will be,

v1 24 0 pwl 5us 0v, 6us 5v, 235us 5v, 236us 0v, 255us 0v
v2 23 0 pwl 5us 0v, 20us 0v, 21us 5v, 220us 5v, 221us 0v, 255us 0v
v3 22 0 pwl 5us 0v, 35us 0v, 36us 5v, 205us 5v, 206us 0v, 255us 0v
v4 21 0 pwl 5us 0v, 50us 0v, 51us 5v, 190us 5v, 191us 0v, 255us 0v
v5 20 0 pwl 5us 0v, 65us 0v, 66us 5v, 175us 5v, 176us 0v, 255us 0v
v6 19 0 pwl 5us 0v, 80us 0v, 81us 5v, 160us 5v, 161us 0v, 255us 0v
v7 18 0 pwl 5us 0v, 95us 0v, 96us 5v, 145us 5v, 146us 0v, 255us 0v
v8 17 0 pwl 5us 0v, 110us 0v, 111us 5v, 130us 5v, 131us 0v, 255us 0v

For 20000 HZ frequency the netlist of time period will be,

v1 24 0 pwl 1us 0v, 2us 5v, 47us 5v, 48us 0v, 51us 0v
v2 23 0 pwl 1us 0v, 4us 0v, 5us 5v, 44us 5v, 45us 0v, 51us 0v
v3 22 0 pwl 1us 0v, 7us 0v, 8us 5v, 41us 5v, 42us 0v, 51us 0v
v4 21 0 pwl 1us 0v, 10us 0v, 11us 5v, 38us 5v, 39us 0v, 51us 0v
v5 20 0 pwl 1us 0v, 13us 0v, 14us 5v, 35us 5v, 36us 0v, 51us 0v
v6 19 0 pwl 1us 0v, 16us 0v, 17us 5v, 32us 5v, 33us 0v, 51us 0v
v7 18 0 pwl 1us 0v, 19us 0v, 20us 5v, 29us 5v, 30us 0v, 51us 0v
v8 17 0 pwl 1us 0v, 22us 0v, 23us 5v, 26us 5v, 27us 0v, 51us 0v