OPTIMAL DESIGN OF SUBTHRESHOLD MOSFET

A Thesis submitted to the Department of Electrical, Electronic and Communication Engineering (EECE) of Military Institute of Science and Technology (MIST) for partial fulfillment of the course "EECE-400" for the degree of Bachelor of Science in Electrical, Electronic and Communication Engineering.

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CERTIFICATION

This thesis paper entitled **"Optimal Design of Subthreshold MOSFET**" submitted by the group under mention, has been accepted as satisfactory in partial fulfillment of the requirements for the degree of Bachelor of Science in Electrical, Electronic and Communication Engineering on December, 2017.

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DECLARATION

We hereby declare that the thesis titled "**Optimal Design of Subthreshold MOSFET"** is submitted to the Department of Electrical, Electronic and Communication Engineering for the partial fulfillment of the requirement for Bachelor of Science Degree on Electrical, Electronic and Communication Engineering (Course Number 400).

This is our original work under the supervision of **Dr. Md. Forkan Uddin** and was not submitted elsewhere for the award of any other degree or any other publication.

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ABSTRACT

As data storage devices, MOSFETs have been used for a long time. However, the data storage mainly involves the digital characteristics and so the analog especially high frequency appliances have been neglected for long and BJT have been the analog designer's choice. With the miniaturization and low power devices on demand, the analog designers have been tiled towards MOSFET and more models are being developed in subthreshold regime as subthreshold is the region below the threshold voltage that can operate with a current less than the subthreshold current, thus achieving low energy with a performance penalty in terms of frequency. However, in this era of technology where everyone is aiming to achieve the greatest speed possible, frequency penalty is unacceptable. So, in this paper, we explore the performance parameters and find optimum solutions for which frequency will not be forsaken to operate low voltage devices. In this regard, we explore high performance speed and power degradation parameters, transition frequency, F_t and gate capacitance, C_g and analyze their graphical relationships with device design parameters, i.e., channel length L, channel width, W and applied gate to source voltage, V_{gs}. We formulate an optimization problem to find the optimal design of a subthreshold MOSFET device. The optimization problem is found to be a convex problem. We solve the optimization problem using an optimization tool. The numerical results show that the proposed optimization based design approach is able to minimize the gate capacitance, C_g and maximize the transition frequency, F_t.

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CHAPTER 1

INTRODUCTION

Metal-oxide-semiconductor (MOS) integrated circuits (ICs) have met the world's growing needs for electronic devices for computing, communication, entertainment, automotive, and other applications with continual improvements in cost, speed and power consumption. These improvements in turn stimulated and enabled new applications and greatly improved the quality of life and productivity worldwide. The primary engine that powered the proliferation of electronics is "miniaturization." By making the transistors and interconnects smaller, more circuits can be fabricated on each silicon wafer and therefore each circuit becomes cheaper. Miniaturization has also been instrumental to the improvements in speed and power consumption of ICs. Gordon Moore made an empirical observation in 1965 that the number of devices on a chip doubles every 18 to 24 months or so.

The line width, some other parameters are also reduced with scaling such as the MOSFET gate oxide thickness and the power supply voltage. The reductions are chosen such that the transistor current density increases with each new node. Also, the smaller transistors and shorter interconnects lead to smaller capacitances. Together, these changes cause the circuit delays to drop.

Historically, IC speed has increased roughly 30% at each new technology node. Higher speed enables new applications such as wide-band data transmission via RF mobile phones [1], [2].

As one of the method to potentially solve the power consumption issue and increase the speed of the devices, this paper explores the subthreshold operation region. Although subthreshold operation design reduces power consumption according to past studies, its performance degradation and susceptibility to noise and variations of temperature have prevented its application. In this paper, an optimization model is explored with an attempt to analyze and numerically calculate the optimum points which will help to increase the speed of the subthreshold MOSFET device and also reduce the power consumption by reducing gate capacitance.

1.1 MOSFET Structure:

The MOSFET is by far the most prevalent semiconductor device in ICs. It is the basic building block of digital, analog, and memory circuits. Its small size allows the making of inexpensive and dense circuits such as Giga-bit (GB) memory chips. Its low power and high speed make possible chips for gigahertz (GHz) computer processors and radio-frequency (RF) cellular phones.

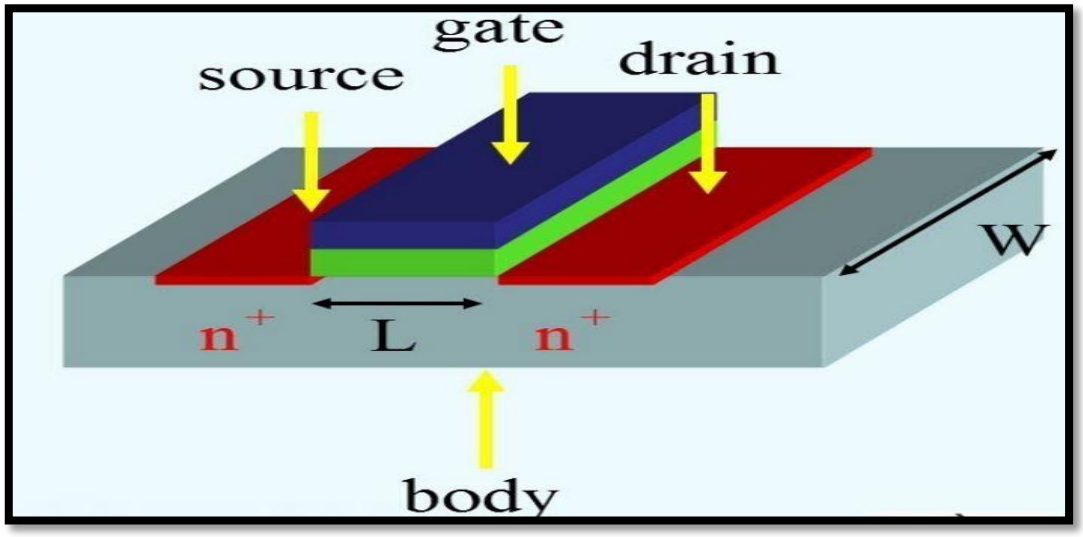

Figure 1.1: Basic MOSFET Structure [3].

Figure 1.1 shows the basic structure of a MOSFET. The two PN junctions are the source and the drain that supplies the electrons or holes to the transistor and drains them away respectively. This device is symmetric, so either of the n+ regions can be source or drain. The name field-effect transistor or FET refers to the fact that the gate turns the transistor (inversion layer) on and off with an electric field through the oxide. A transistor is a device that presents a high input resistance to the signal source, drawing little input power, and a low resistance to the output circuit, capable of supplying a large current to drive the circuit load. Modern Si MOSFETs are all enhancement-mode transistors where a (forward) gate voltage is needed to turn the transistor on as N-channel is thinner than the depletion-layer width at $V_g = 0$. This make circuit design much easier [4].

1.2 Operating Principle of MOSFET:

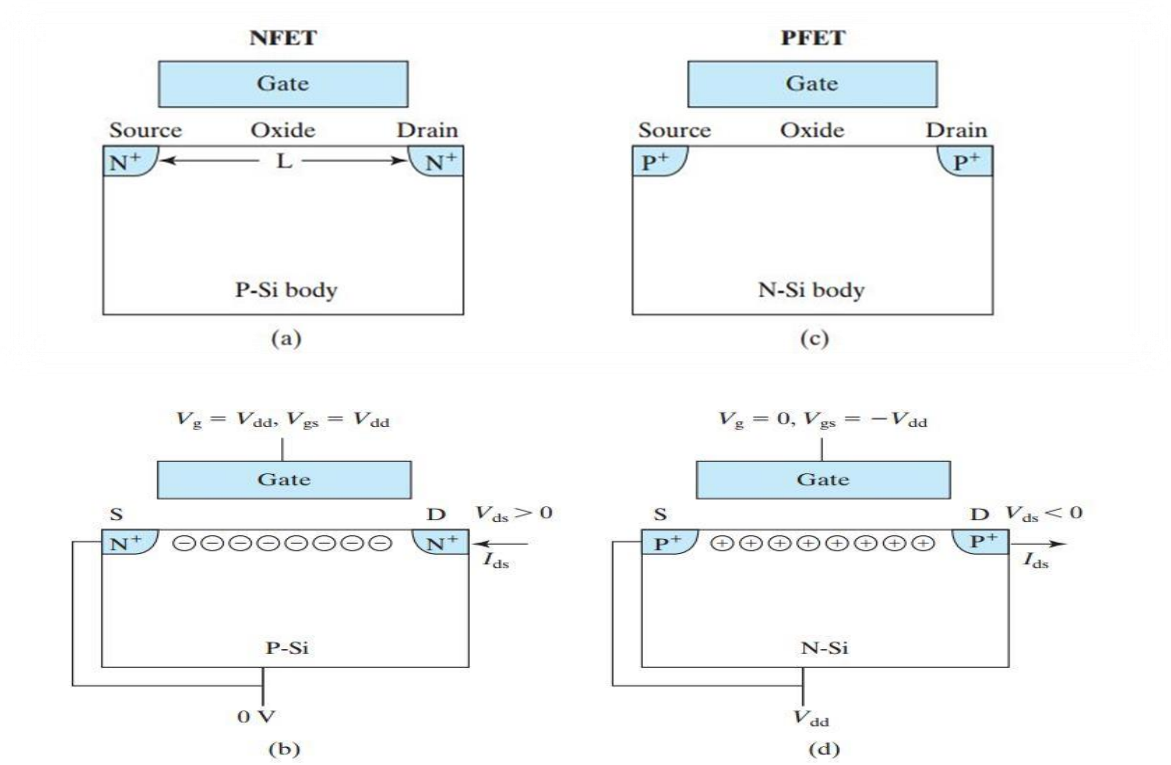

Figure 1.2: Schematic Drawing of N-channel and P-channel MOSFET Off State (a), (c) and On State (b), (d) [4].

Figure 1.2 also shows Schematic drawing of N-channel and P-channel MOSFET. Depending on the gate voltage, the MOSFET can be off (conducting only a very small off-state leakage current, (I_{off}) or on (conducting a large on-state current, I_{on}). It is called N-channel because the conduction channel (i.e., the inversion layer) is electron rich or N-type. Figure 1.2 (c) and d illustrate a P-channel MOSFET, or P-MOSFET, or PFET. In both cases, V_{gs} and V_{dd} swing between 0 V and V_{dd}, the power-supply voltage. The body of an NFET is connected to the lowest voltage in the circuit, 0 V, as shown in 1.2 (b). Consequently, the PN junctions are always reverse-biased or unbiased and do not conduct forward diode current. When V_{gs} is equal to V_{dd} as shown in 1.2(b), an inversion layer is present and the NFET is turned on. With its body and source connected to V_{dd}, the PFET shown in 1.2(d) responds to V_g in exactly the opposite manner. When $V_{gs} = V_{dd}$, the NFET is on and the PFET is off. When $V_{gs} = 0$, the PFET is on and the NFET is off. The complementary nature of NFETs and PFETs makes it possible to design low-power circuits called CMOS or complementary MOS circuits [4].

1.3 MOSFET I-V Characteristics Curve:

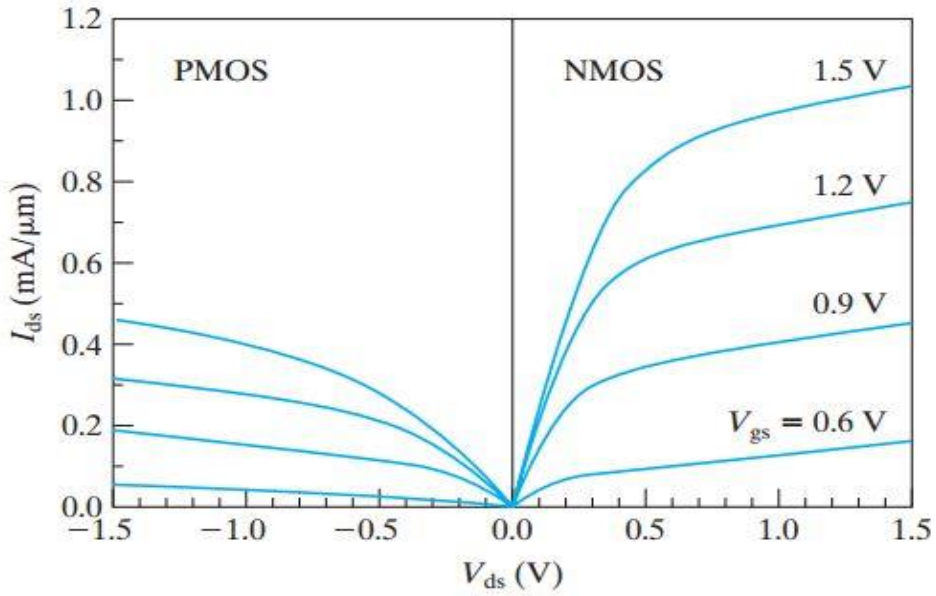

Figure 1.3: I-V characteristics of PFET and NFET with T_{ox} = 3 nm and $L \approx 100$ nm [4].

In figure 1.3, PFET and NFET have similar I-V characteristics, e.g., both exhibit a linear $I_{dsat} - V_{gs}$ relationship. I_P is about half of I_N. The holes mobility is three times smaller and their saturation velocity is 30% smaller than that of the electrons [5].

So MOSFET exhibit three basic regions of operation viz., cut-off, linear or ohmic and saturation. When they are used in amplifiers they are required to operate in ohmic region. On the other hand when MOSFETs are required to function as switch they are biased in such a way that they alter between cut-off and saturation states. They also used in chopper circuits, linear voltage regulators. MOSFETs require no gate input current other than a pulse to charge or discharge the input capacitance. They can operate at higher switching speeds and lower currents than bipolar transistors. The main advantage of a MOSFET is that it requires almost no input current to control the load current, when compared with bipolar transistors. In an "enhancement mode" MOSFET, voltage applied to the gate terminal increases the conductivity of the device. In "depletion mode" transistors, voltage applied at the gate reduces the conductivity [5], [6].

1.4 Subthreshold MOSFET:

Subthreshold operation is one of the low power design approaches known to designers as subthreshold occurs for ultra-low power applications. We know that circuit speed improves with increasing I_{on} and for lower use of energy, small threshold voltage, V_{th} is also desirable but V_{th} can't be set arbitrarily small.

Subthreshold region is the region where a MOSFET is being operated below the threshold voltage. Threshold voltage is the minimum gate to source voltage that is needed to create a conducting path between the sources and drain terminals. There are three operating region for MOS: Subthreshold region, linear region, Saturation region. Working at the subthreshold region is useful for systems that should work at low voltages around 1V. The main benefit of working at this region is that the output current is related exponentially with the input voltage rather than the quadratic relationship to the input voltage in saturation region. This increases the transconductance of the MOSFET and so getting higher gain. It is hard to say where this region start for sure but a 50mV less than the threshold voltage is good. In the past, the subthreshold conduction of transistors have usually been very small in the off state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, subthreshold conduction has become a bigger factor.

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low.

Subthreshold is the region below the threshold voltage that can operate with a current less than the subthreshold current, thus achieving low energy with a performance penalty in terms of frequency to maintain device reliability. The amount of subthreshold conduction is set by threshold voltage, which sits between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device off and as subthreshold conduction varies

exponentially with gate voltage. It becomes more and more significant as MOSFETs shrink in size [4].

1.5 Transition Frequency:

This is the frequency at which the gain of the transistor's grounded emitter becomes 1. This value indicates how high a frequency signal can be amplified. This limit of frequency is generally known as the gain bandwidth product (F_t). It is defined as a short circuit current gain of transistor.

So to increase Transition frequency:

- Semiconductors are used with higher charge mobility (hard to implement). From this it is obtained that n-MOS has higher F_t than p-MOS due to higher electron mobility than holes.
- To boost g_m higher overdrive voltage is used.
- Use of minimum Gate length [1], [4].

1.6 Gate Capacitance:

Gate to drain capacitance is a non-linear function of the voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. It is also called Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. Gate capacitance is very important as it creates channel charge necessary for operation [1].

1.7 Motivation:

Combining hundreds of interconnected transistors on a small chip, the integrated circuit (IC) was created in the early 1960.Transistors have been shrinking exponential in size and therefore the number of transistors in a single microelectronic chip exponentially. Such an increase in packing density was made possible by continually shrinking the metal-oxide-semiconductor field-effect transistor MOSFET. In the current generation of transistors, the transistor dimensions have shrunk to such an extent that the exponential decrease in transistor size can continue. Recently, however, a new generation of MOSFETs, called multi gate transistors, has emerged and this multi gate geometry will allow the continuing enhancement of computer performance into the next decade [4]. To better estimate the circuit delay and understand the effect of variations in the subthreshold region, a variations-aware analytical model is proposed and verified through simulations [5].

There are also some research paper that investigate about the threshold voltage of MOSFET. Kyungseok Kim [6] propose a method for minimum energy digital CMOS (Complementary Metal Oxide Semiconductor) circuit design using dual subthreshold supply. Fabrication process utilizing 3-D bias is reliable and inexpensive, exhibit low impedance characteristics [7]. The ITRS have played a significant role in the advancement of the CMOS technology [8]. The objective of these are to optimize the subthreshold MOSFET.

However, in previous work there are some lackings. Objective function was not considered earlier, which is important for designing subthreshold MOSFET. Because using objective function, the required important parameters can be obtained. It is important to know the required parameters to design a subthreshold MOSFET. So, we try to make our optimization problem using an objective function. And considering more realistic, we designed a subthreshold MOSFET to solve those problems.

1.8 Contribution:

- We study the effect of different parameters on the transition frequency (F_t) and gate capacitance (C_g) of subthreshold MOSFET.
- We formulate an optimization problem to optimally design a subthreshold MOSFET.
- We numerically solve the optimization by using an optimization tool MATLAB.
- We present different characteristic curves for different parameters.

1.9 Outline:

- Chapter 1 contains primary introduction of the thesis. Also, there is study about MOSFET structure, its operating principle, its I-V characteristics curve, subthreshold MOSFET, transition frequency (F_t) and gate capacitance (C_g) of subthreshold MOSFET. It also contains motivation behind this research and contribution of this research.
- Chapter 2 contains related work about the design of MOSFET.
- Chapter 3 contains performance analysis of subthreshold MOSFET. It also contains, the modeling of (F_t) and (C_g) and the performance analysis of subthreshold MOSFET based on models.
- Chapter 4 contains problem formulation and solution to design the subthreshold MOSFET.
- Chapter 5 contains the conclusion and future work.

CHAPTER 2

RELATED WORK

In [1], it informs that Intel's Itanium microprocessor contained more than 2 billion transistors and a 16 GB Flash memory contained more than 4 billion transistors. This corresponds to a compound annual growth rate of 53% over 50 years. No other technology in history has sustained such a high growth rate lasting for so long. And all this is possible due to the continuous improvement of MOSFETS in various applications. In [2], it shows that MOSFETs have been used as switches in digital application where they remain outside the switching or transition region most of the time. On the other side, the analog circuit's linearity response is depended upon the MOSFET**'**s switching region. In the forty-five years since 1965, the price of one bit of semiconductor memory has dropped 100 million times. The cost of a logic gate has undergone a similarly dramatic drop.
According to [4], the primary engine that powered the proliferation of electronics is "miniaturization" which journey begins with the introduction to Moore's law. Gordon Moore made an observation in 1965 that the number of devices on a chip doubles every 18 to 24 months. This Moore's law is succinct description of the rapid and persistent trend of miniaturization. Each time the minimum line width is reduced, a new technology generation or technology node is introduced.

In [4], [9] and [10], it informs that miniaturization has also been instrumental to the improvements in speed and power consumption of Ics as with the introduction of miniaturization and its continuous development depending on the Moore**'**s law, MOSFETs are continuously being used in analog circuits. In [11] and [12], improvement of speed, power consumption and high performance of MOSFETs have been discussed which give MOSFETS extra advantage to analog designers over their choice of BJT. An important goal of device design is to minimize circuit power consumption. In [13] and [14], it shows that it is desirable for a transistor to provide a large I_{on} (to reduce circuit switching delay) at a low V_{dd} (to reduce circuit power consumption). In [13] and [14], it's also shown that reducing the transistor L and W, other parameters being equal, would lower capacitance through reduction in the gate capacitance and the source–drain junction capacitance. In [15], it confirms that smaller transistors make the chip smaller and

therefore reduce the interconnect capacitance too. Both device size reduction and V_{dd} reduction have been powerful means of lowering the power consumption per circuit function. So, this concludes that it is highly desirable to have large I_{on} , without using a large power supply voltage, V_{dd}. It is also desirable to reduce the total load capacitance, C (including the junction capacitance of the driver devices, the gate capacitance of the driven devices, and the interconnect capacitance). Both capacitance and cost reductions provide strong motivations for reducing the size of the transistors and therefore the size of the chip. In addition, speed has benefited from the relentless push for smaller L, thinner T_{ox}, and lower V_t; and power consumption has benefited greatly from the lowering of $V_{dd.}$

In [16] and [17], it is stated that subthreshold operation is one of the low power design approaches known to designers as subthreshold occurs for utra low power applications. MOSFET current observed at $V_{gs} < V_{th}$ is called the subthreshold current. It is the main contributor to the MOSFET off-state current, I_{off} .To minimize the static power, it is important to keep I_{off} very small. Although subthreshold I_{off} isn't a problem if V_{th} is very high but high V_{th} isn't desirable as it would reduce I_{on} and therefore reduce circuit speed. For continual scaling of both V_{dd} and V_{th} ; this offset leakage current has spurred. The exponential relation between V_{th} and I_{off} is central to this problem. So V_{th} needs to be reduced to maintain good device switching speeds at low supply voltage. In [18], a square law device term is used which is a device where either current or voltage depends on the square of the other. For a threshold operated MOSFET, $I_d \propto (V_{gs} - V_{th})^2$. But with the introduction of subthreshold regime, this conventional square laws has become invalid and there's been need of derivation of new models for subthreshold region. In [19], [20] and [21], such important models for nano sclae subthreshold MOSFETs are introduced which concludes some very important informations regarding low voltage designs. In [19] it comes to a conclusion that the subthreshold region will cause the MOSFET to heat up more than other regions due to having the most 'on' resistance. It derives that,

$$\sigma^2 \Delta C_g \propto T^{-2}$$

$$\sigma^2 \Delta f_t \propto T^{-6}$$

Here σ, Δ, T, Cg, f_t indicates variance, change of the parameters, room temperature, gate capacitance, transient frequency respectively. It means that Δf_t is low and ΔC_g is high if the temperature is low and vice versa for high temperature. However, the rate of change

in Δf_t to the temperature is greater than that of ΔC_g. Another important derivation from [20] is the Subthreshold MOSFET's High Frequency Characteristics model which says,

$$\sigma^2 \Delta C_g \propto L$$
$$\sigma^2 \Delta f_t \propto L^{-7}$$

Here σ, Δ, L, Cg, f_t indicates variance, change of the parameters, channel length respectively.

This explains that the shrinking of gate length can reduce ΔC_g, but higher degree of increasing in Δf_t is considered a penalty. So, this trade-off issue must be taken into account in the designing of subthreshold region operated MOSFET based high frequency applications for any transistor type.

These subthreshold model concepts can help to design self-sufficient power devices with effective cooling process and get us closer towards the era of battery less devices. In [22], it also shows how these models and derivations can be used in explaining process variables (i.e. PVT, process, voltage, temperature) in the subthreshold region.

Various Subthreshold MOSFETs dc applications are also explored which are included below:

- Subthreshold CMOS active inductor [23], [24], [25].
- Subthreshold Leakage Current for VLSI circuits [26], [27], [28].
- Subthreshold mismatch principles [29], [30], [31].
- Subthreshold scaling [32], [33], [34].

CHAPTER 3

PERFORMANCE ANALYSIS OF SUBTHRESHOLD MOSFET

In this chapter, the performance analysis of subthreshold MOSFET based on Gate Capacitance (C_g) model and Transition Frequency (F_t) model is presented.

3.1 Gate Capacitance (C_g) Model:

It is necessary to give some detailed information about the basic idea of modeling subthreshold region operated MOSFET.

At the most basic level, a MOSFET may be thought of as an on-off switch as shown in the Figure 3.1.

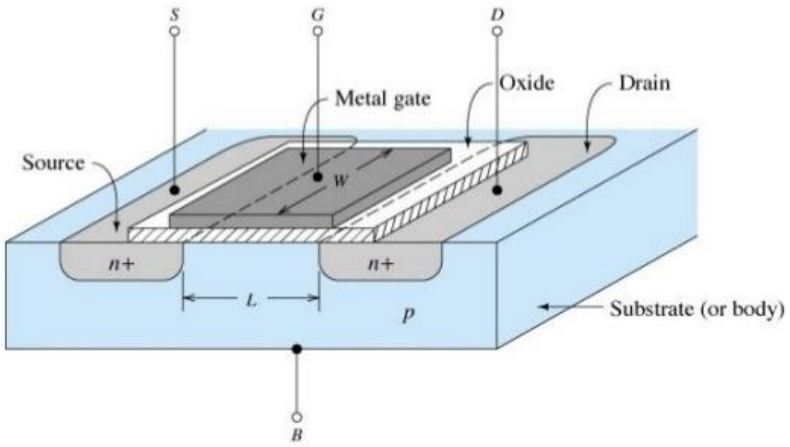

Figure 3.1: n-Channel enhancement MOSFET showing channel length L and width W [35].

Here, S, G, D, B denotes source, gate, drain and body terminals respectively. Also W, L denotes channel width and channel length respectively. Oxide material (SiO2) is used to make isolation between channel and gate terminal. Hence there forms an oxide capacitance which is denoted by Cox.

When a voltage signal is applied below the threshold voltage at the gate terminal, then a weak inversion region is formed that allows a current conduction path which is known as drain current, I_d.

The drain current [36], I_d of subthreshold MOSFET is given by,

$$I_d = \mu C_{dep} \frac{W}{L} \left(\frac{kT}{q}\right)^2 exp\left[\frac{Vgs - Vt}{nkT/q}\right] \left[1 - exp\left[-\frac{Vds}{nkT/q}\right]\right] \quad \text{.....(3.1)}$$

Here, C_{dep}, n, μ, k, T, q, V_{gs}, V_t, V_{ds} denote the capacitance of the depletion region under the gate area , the subthreshold slope factor which lies between 1 and 1.5, carrier mobility, Boltzmann constant which is 1.38×10^{-23}, temperature which is 298 k, charge which is 1.6×10^{-19}, gate to source voltage, threshold voltage and drain to source voltage.

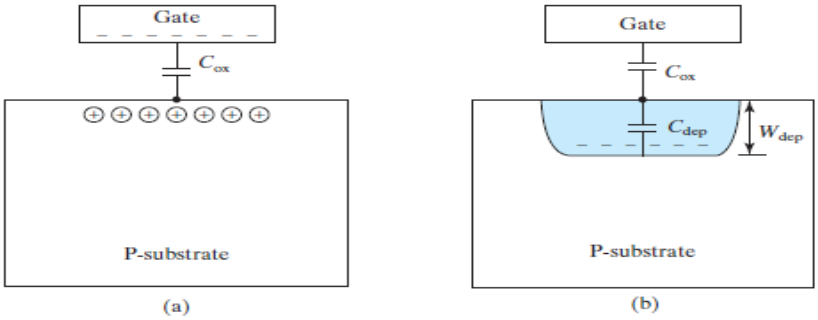

Figure 3.2: Illustration of the MOS capacitor in all bias regions with the depletion layers shaded. (a) Accumulation region; (b) Depletion region.

It is mentioned here that the necessary condition for operating in the subthreshold region of any MOSFET is $V_{gs} < V_t$ which can be simply given as follows [37].

V_t = VFB + ϕs + $\epsilon_{ox}{}^{-1} q$ tinv Nsub Wdep .....(3.2)

Here, V_t , Nsub, tinv, Wdep, VFB and ϕs stand for the threshold voltage of subthreshold MOSFET, substrate doping concentration, electrical gate dielectric thickness, depletion width, flat band voltage and surface potential respectively.

By using Eq. (1), the transconductance, gm of subthreshold MOSFET can be given as [36],

$$g_m = \frac{\mu}{n} C_{dep} \frac{W}{L} \left(\frac{kT}{q}\right)^2 exp\left[\frac{Vgs - Vt}{nkT/q}\right]\left[1 - exp\left[-\frac{Vds}{nkT/q}\right]\right] \quad \text{.....(3.3)}$$

At this point, it is ready to present the proposed analysis and modeling. Here, the mathematical description of MOSFET's gate capacitance, *Cg* which is the capacitive part of the total admittance seen by looking in to the gate terminal of the MOSFET, *Yg* conceptually defined in **Fig.3.3**, can be given as in (3.4) [38].

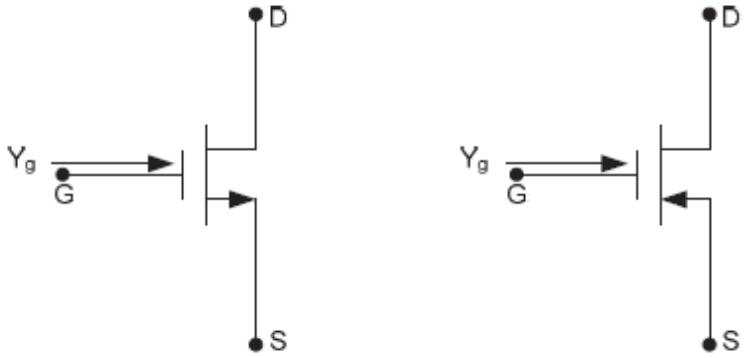

Figure 3.3: Conceptual definition of *Yg* of N-type MOSFET (left) and P-type MOSFET (right) [36].

$$Cg \triangleq \frac{dQg}{dVgs} \quad \text{..... (3.4)}$$

Here, Qg denotes the gate charge [38] which can be given by [39],

$$Qg = \frac{\mu W^2 L C_{ox}^2}{I_d} \int_0^{Vgs - Vt} (Vgs - Vc - Vt)^2 \, dVc - Q_{B,max} \quad \text{.....(3.5)}$$

It should be mentioned here that $Q_{B,max}$ denotes the maximum bulk charge [39]. By applying Eq. (1) for I_d in Eq. (5), Qg of the subthreshold region operated MOSFET can be given by,

$$Qg = \frac{\left[\frac{WL^2C_{ox}^2}{C_{dep}\left(\frac{kT}{q}\right)^2}\right](Vgs - Vt)^3}{3\left[1-exp\left[-\frac{Vds}{nkT/q}\right]\right]exp\left[\frac{Vgs - Vt}{nkT/q}\right](Vgs - Vt)} - Q_{B,max} \quad \text{.....(3.6)}$$

So, C_g of the subthreshold MOSFET can be given as follows [36],

$$C_g = \frac{1}{3}\left[\frac{WL^2C_{ox}^2}{C_{dep}\left(\frac{kT}{q}\right)^2}\right]\left[3(V_{gs} - V_t)^2 - \frac{q}{nkT}(V_{gs} - V_t)^3\right] exp\left[-\frac{q}{nkT}(V_{gs} - V_t)\right] \text{..... (3.7)}$$

3.2 Model for Transition Frequency (F_t):

The maximum operating frequency, ω_T, is the frequency at which the FET no longer amplifies the input signal: that is, the dependent current source g_mVgs is equal to the input current.

$$\omega_T = \frac{g_m}{(C_g + C_{ds})} \text{..... (3.8)}$$

We know that, $\omega_T = 2\pi F_t$, and g_m, C_g from the above equation and taking drain to gate capacitance C_{ds} from (8) we get the transition frequency (F_t) which is the unity gain frequency, that gives by [36],

$$F_t = \frac{3}{2}\left[\frac{\mu C_{dep}^2\left(\frac{kT}{q}\right)^3}{2n\Pi L^3C_{ox}^2}\right]\left[1 - exp\left[-\frac{V_{ds}}{kT/q}\right]\right]^2\left[\frac{exp\left[\frac{2q}{nkT}(V_{gs} - V_t)\right]}{3(V_{gs} - V_t)^2 - \frac{q}{nkT}(V_{gs} - V_t)^3}\right] \text{.....(3.9)}$$

Now, based on these two model for C_g and Ft, the characteristics of a subthreshold region operated MOSFET can be illustrated by taking the variable parameters such as channel length (L), channel width (W), and gate voltage (V_{gs}). In these illustration all other constant values are taken as standard values.

3.3 Performance Analysis Based on Models:

In this section, we illustrate the graphical representation of the above stated models by taking each of the three variables separately and at the same time rest of them will be considered as constant.

We want to see the response of our desired MOSFET by changing only one variable along X-axis and output characteristics such as C_g and F_t in the Y-axis respectively, while keeping all the other variables as constant with standard values.

3.3.1 Output Characteristics of C_g with Respect to L:

The output characteristics of C_g with respect to L is obtained here. In order to see the output characteristics of C_g with respect to channel length (L), putting C_g in the Y-axis and channel length (L) along X-axis was varied from the lower bound to the upper bound. We used 45nm process for our design purposes, so we had to vary channel length (L) from 45nm to a particular length say 250 nm and taking all others as constants such as n, C_{ox}, C_{dep}, q, k, T in kelvin, V_t, $V_{gs,}$ and channel width (W). All the characteristics analysis are done in MATLAB 2017a.

As stated in the gate capacitance (C_g) model, MOSFET gate capacitance (C_g) is proportional to the square of the channel length (L). So when we increased channel length from 50nm to 250nm, MOSFET gate capacitance (C_g) increase non-linearly.

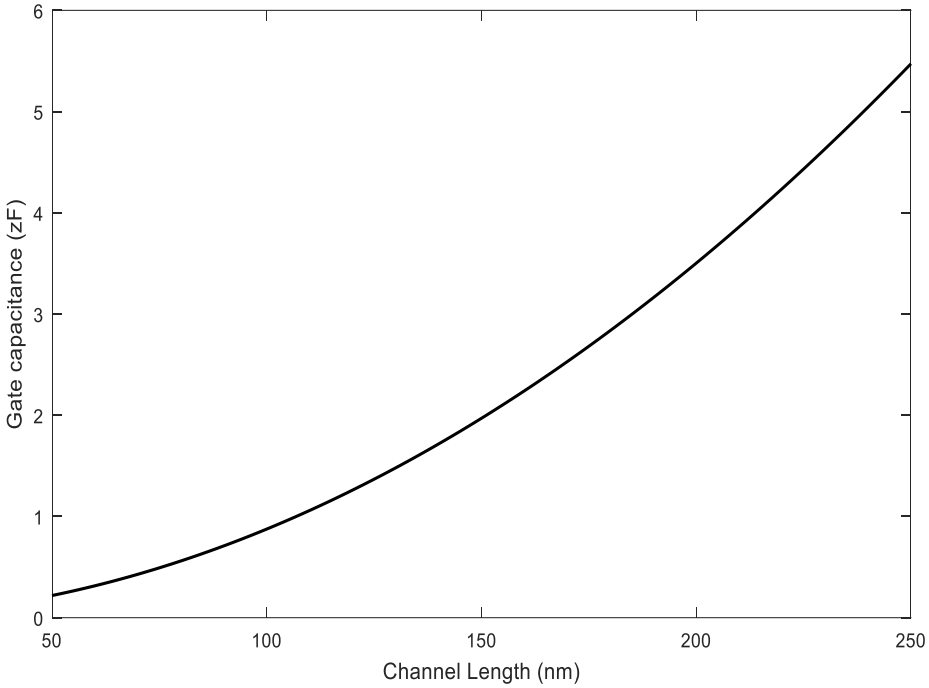

Figure 3.4: Illustration of channel length (L) vs gate capacitance (C_g).

We know, parallel plate capacitance C= $\frac{\epsilon A}{d}$ [40]. Here ϵ, A, d denotes the permittivity of dielectric, area of the capacitor plate and distance between two plates and A is proportional to the channel length (L). So as far as channel length (L) increases, the area of the MOS-capacitor plate increases hence the capacitance C also increases, which we can see in the above figure 3.4.

3.3.2 Output Characteristics of C_g with Respect to W:

The output characteristics of C_g with respect to W is obtained here. The characteristics of C_g is shown by varying channel width (W) as follows,

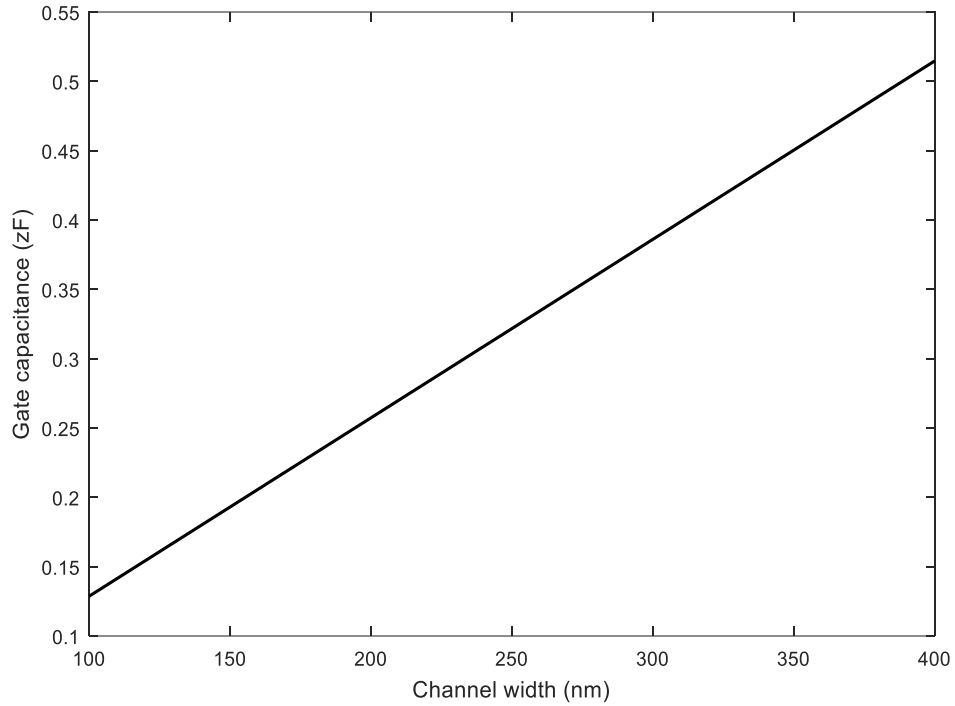

Figure 3.5: Illustration of channel width (W) vs gate capacitance (C_g).

From the gate capacitance (C_g) model, we can see that, MOSFET gate capacitance (C_g) is directly proportional to the channel width (W). It is necessary to take a larger width for a MOSFET which results a smaller drain to source resistance (Rds) or internal resistance of a MOSFET that cause a better current conduction path with low noise. So when we increase channel width (W) from 100nm to 400nm, MOSFET gate capacitance (C_g) increase linearly that appear in the MATLAB graph.

From figure 3.5 we can see that, if W increase, then area of the MOS-capacitor also increases as well as capacitance increase as discussed above.

3.3.3 Output Characteristics of C_g with Respect to V_{gs}:

The output characteristics of C_g with respect to V_{gs} is obtained here. The characteristics of C_g by varying gate voltage (V_{gs}) as follows,

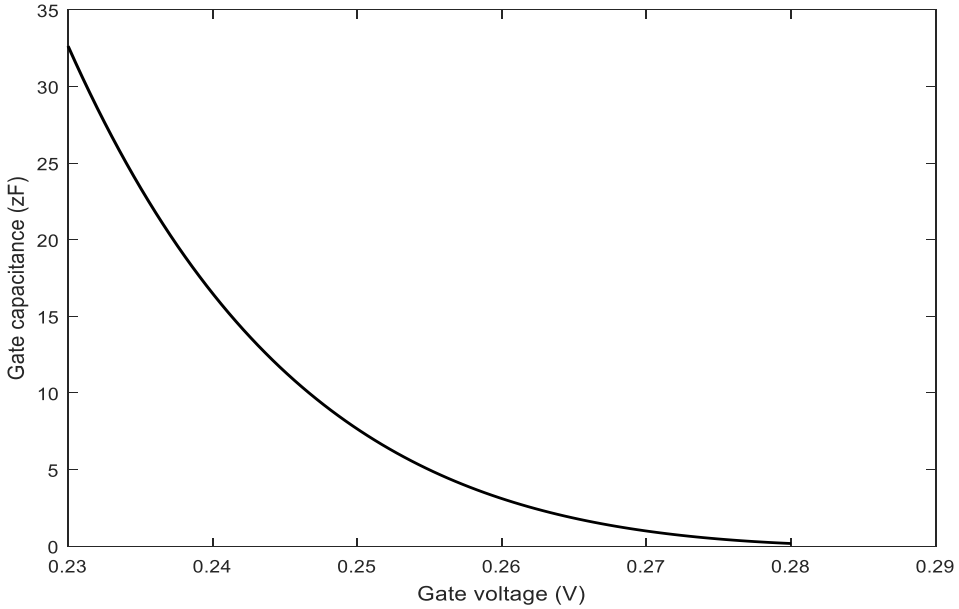

Figure 3.6: Illustration of gate voltage (V_{gs}) vs gate capacitance (C_g).

Here is the characteristics plot from MATLAB in which, gate voltage (V_{gs}) is varied from 0.23v to 0.28v that is below the threshold voltage (V_t). It is necessary to limited V_{gs} below V_t which is prerequisite for a weak inversion region of a subthreshold region operated MOSFET. Increase of V_{gs} results an exponential decrease of gate capacitance (C_g). From, C= $\frac{Q}{V}$ [40]. Here Q and V denotes charge and applied voltage respectively. We get capacitance is inversely proportional to V. For that reason when applied gate voltage increases, capacitance (C_g) decreases exponentially in the above figure.

3.3.4 Output Characteristics of F_t with Respect to L:

The Output Characteristics of F_t with Respect to L is obtained here. We analyzed the transition frequency (F_t) which is the unity gain frequency by varying channel length (L) along the X-axis which gives us follows,

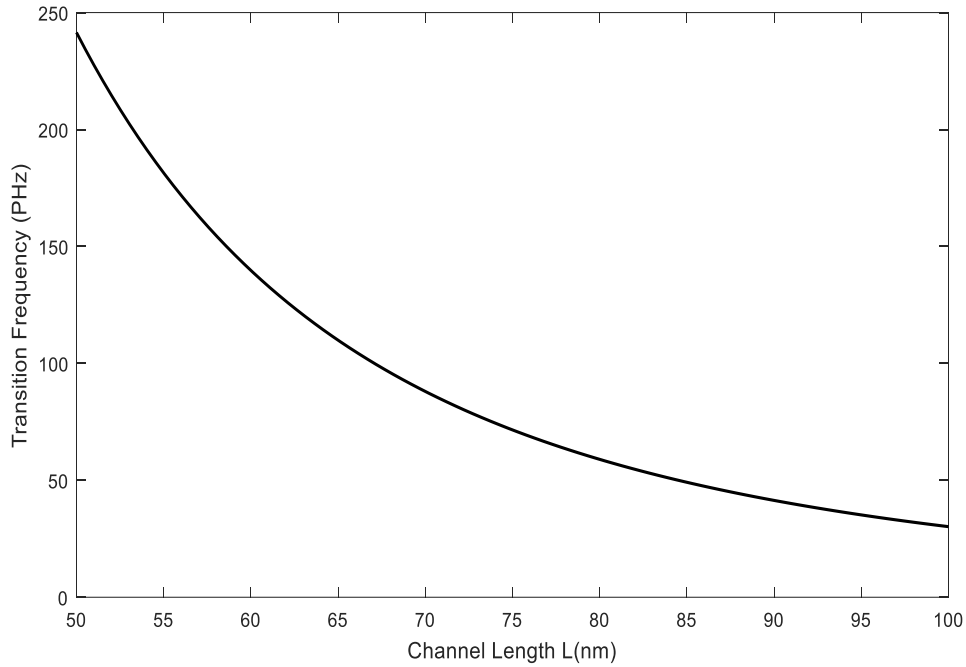

Figure 3.7: Illustration of channel length (L) vs transition frequency (F_t).

MOSFET transition frequency is inversely proportional to the cube of the channel length (L), So when we change the length from 50nm to 100nm, the transition frequency is decreased non-linearly as we can see in the MATLAB plot.

Here, when channel length (L) is increasing gate capacitance (C_g) is also increased. And if C_g increase, charging-discharging time is also increase. We know frequency is inversely proportional to time. So that F_t decreases when C_g increase.

3.3.5 Output Characteristics of F_t with Respect to V_{gs}:

The output characteristics of F_t with respect to V_{gs} is obtained here. The characteristics of F_t is shown by varying gate voltage (V_{gs}) as follows,

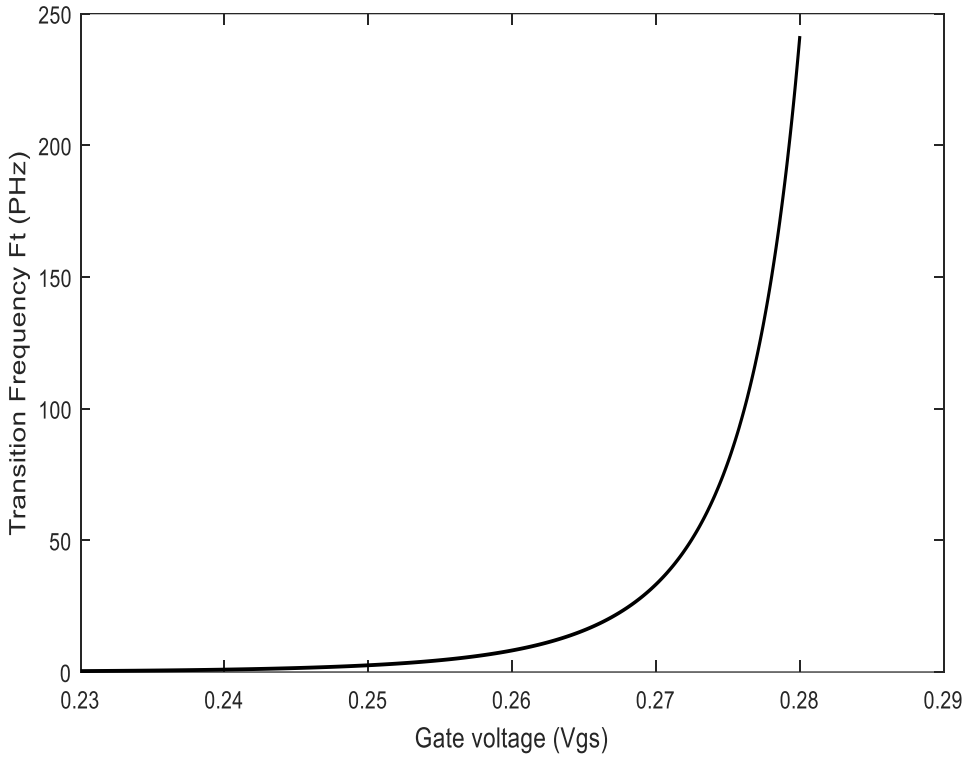

Figure 3.8: Gate voltage (V_{gs}) vs transition frequency (F_t)

Characteristics plot from MATLAB in which, gate voltage (V_{gs}) is varied from 0.23v to 0.28v that is below the threshold voltage (Vt). It is necessary to limited V_{gs} below Vt which is prerequisite for a weak inversion region of a subthreshold region operated MOSFET. Increase of V_{gs} results an exponential increase of transition frequency (F_t). Here, V_{gs} increase when C_g decrease and switching time also decrease. So F_t increase while increasing V_{gs}.

3.4 Summary:

High frequency performance of MOSFET can be defined by two major parameters, entitled gate capacitance, C_g and transition frequency, Ft which depends on MOSFETs channel length (L), channel width (W) and applied gate voltage (V_{gs}). For high frequency performance of subthreshold MOSFET, it has found that When channel length (L) increases, its gate capacitance (C_g) increase and transition frequency (F_t) decrease, When channel width (W) increases, its gate capacitance (C_g) increase. When gate voltage (V_{gs}) increases, its gate capacitance (C_g) decrease at the same time transition frequency (F_t) increase.

CHAPTER 4

OPTIMAL DESIGN OF SUBTHRESHOLD MOSFET

In this chapter, the optimization problem formulation for subthreshold MOSFET is given. Then we approached for the solution. And we numerically solved the optimization problem using MATLAB.

4.1 Problem Formulation:

Here, 45 nanometer process technology is used for optimal subthreshold MOSFET design. From chapter 3, it is found that, F_t and C_g are inversely proportional to each other and F_t is in PHz (10^{15}) and C_g is in ZF (10^{-23}). Here C_g is very small compared to F_t. So to make the value of C_g near to F_t, the values of channel length (L) and channel width (W) are considered in millimeter range instead to nanometer range. To make the transition frequency (F_t) high, objective function need to be maximized.
So, an objective function is formulated as $Z = \alpha F_t - (1-\alpha) C_g$.

Subject to: $L_{min} \leq L \leq L_{max}$

$W_{min} \leq W \leq W_{max}$

$0 \leq V_{gs} \leq V_t$

α is varied from 0 to 1 to find L(length), W(width), V_{gs}(applied gate voltage) such that the function Z is maximized. The values of the parameters are considered as, L_{min} = 45 nm, L_{max} = 250 nm, W_{min} = 135 nm, W_{max} = 450 nm, V_t = 0.32 V.
The efficiency of the optimization technique depends on the nature of the objective function. If the objective function is non-convex in nature, global optimal is achieved. To check convexity, 1st and 2nd order derivatives of the objective function with respect to the variables need to be derived.
So first of all, it had to found out whether the above objective function is convex or not.

4.1.1 Convexity Test:

If $f_{(X1,X2,\ldots\ldots Xn)}$ has continuous second order partial derivatives, then $f_{(X1,X2,\ldots\ldots Xn)}$ is convex if its n×n Hessian matrix is positive semidefinite for all positive values of $f_{(X1,X2,\ldots\ldots Xn)}$. And $f_{(X1,X2,\ldots\ldots Xn)}$ is concave if its n×n Hessian matrix is negative semidefinite for all possible values of $f_{(X1,X2,\ldots\ldots Xn)}$.

- n×n Hessian matrix is positive semidefinite if the scalar Z^T×H×Z is non negative for every non zero column vector of Z of n real numbers.
- n×n Hessian matrix is negative semidefinite if the scalar Z^T×H×Z is non positive for every non zero column vector of Z of n real numbers.

Here, Gate capacitance, (C_g) and transition frequency, (f_t) is as follows,

$$C_g = \frac{1}{3}\left\{\frac{WL^2cox^2}{C_{dep}(\frac{KT}{q})^2}\right\}\times\{3(V_{gs}-V_t)^2-\{\frac{q}{nKT}(V_{gs}-V_t)^3\}\times\exp\{-\frac{q}{nKT}(V_{gs}-V_t)\}. \quad (4.1)$$

$$F_t=\frac{3}{2}\{\frac{\mu C_{dep}(\frac{KT}{q})^3}{2n\pi L^3(cox)^2}\}\times\{1-exp(-\frac{V_{ds}}{\frac{KT}{q}})\}^2\times\{\frac{\exp\{\frac{2q}{nKT}(V_{gs}-V_t)\}}{3(V_{gs}-V_t)^2-\frac{q}{nKT}(V_{gs}-V_t)^3}\}\ldots\ldots(4.2)$$

Here, cox =17.265e^{-3}, C_{dep} = e^{-3}, V_t =.35, n =1.5, μ = 0.14, V_{gs} = .22 ≈ .29, $\frac{KT}{q}$ = .0265

Suppose for equation (4.1),

$$a = \frac{1}{3}\left\{\frac{cox^2}{C_{dep}(\frac{KT}{q})^2}\right\} = \frac{(17.265\,e^{-3})^2}{3\,e^{-3}\times(.026)^2}=53.97$$

$$b = \frac{q}{nKT} = \frac{1}{1.5\times.026} = 25.64$$

Substituting a and b in equation (4.1) it found as,

$$C_g=aWL^2\times\{3(V_{gs}-V_t)^2-\{b(V_{gs}-V_t)^3\}\times\exp\{-b\,(V_{gs}-V_t)\}\ldots\ldots\ldots\ldots\ldots\ldots(4.3)$$

Then, second order partial derivative of equation (4.3) with respect to W, L and V_{gs} followed by,

1. $\frac{\partial^2 C_g}{\partial W^2} = 0$

2. $\frac{\partial^2 C_g}{\partial W \partial L}$ = 2a L K_1

   Here,

   $K_1 = \{3(V_{gs} - V_t)^2 - b(V_{gs} - V_t)^3\} \times e^{-b(V_{gs} - V_t)}\}$ = 2.98

3. $\frac{\partial^2 C_g}{\partial W \partial V_{gs}}$ = a $L^2 K_2$

   Here,

   $K_2 = \{6(V_{gs} - V_t) - 3\,b(V_{gs} - V_t)^2\} \times \{-be^{-b(V_{gs} - V_t)}\}$ = 1482.8031

4. Similar to 2. $\frac{\partial^2 C_g}{\partial W \partial L}$ = 2a L K_1

5. $\frac{\partial^2 C_g}{\partial L^2}$ = 2a W K_1

6. $\frac{\partial^2 C_g}{\partial L \partial V_{gs}}$ = 2a WL K_2

7. Similar to 3. $\frac{\partial^2 C_g}{\partial W \partial V_{gs}}$ = a $L^2 K_2$

8. Similar to 6. $\frac{\partial^2 C_g}{\partial L \partial V_{gs}}$ = 2a WL K_2

9. $\frac{\partial^2 C_g}{\partial {V_{gs}}^2}$ = aW$L^2 K_3$

   Here,

   $K_3 = [\{3(V_{gs} - V_t)^2 - b(V_{gs} - V_t)^3\} \times b^2 e^{-b(V_{gs} - V_t)}] + [-be^{-b(V_{gs} - V_t)} \times \{6(V_{gs} - V_t) - 3\,b(V_{gs} - V_t)^2\}] + [e^{-b(V_{gs} - V_t)}\ \{6 - 6\mathrm{b}(V_{gs} - V_t)\}] + [\{6(V_{gs} - V_t) - 3\,b(V_{gs} - V_t)^2\}\ \{-be^{-b(V_{gs} - V_t)}\}]$

   = 5671.39007

Then, the Hessian matrix for C_g as follows,

$$\mathrm{H} = \begin{vmatrix} \frac{\partial^2 C_g}{\partial W^2} & \frac{\partial^2 C_g}{\partial W \partial L} & \frac{\partial^2 C_g}{\partial W \partial V_{gs}} \\ \frac{\partial^2 C_g}{\partial L \partial W} & \frac{\partial^2 C_g}{\partial L^2} & \frac{\partial^2 C_g}{\partial L \partial V_{gs}} \\ \frac{\partial^2 C_g}{\partial V_{gs} \partial W} & \frac{\partial^2 C_g}{\partial V_{gs} \partial L} & \frac{\partial^2 C_g}{\partial {V_{gs}}^2} \end{vmatrix} = \begin{vmatrix} 0 & 2\mathrm{a\ L}\ K_1 & \mathrm{a}\ L^2 K_2 \\ 2\mathrm{a\ L}\ K_1 & 2\mathrm{a\ W}\ K_1 & 2\mathrm{a\ WL}\ K_2 \\ \mathrm{a}\ L^2 K_2 & 2\mathrm{a\ WL}\ K_2 & 2\mathrm{a\ WL}\ K_2 \end{vmatrix}$$

Assume, another matrix as, Z= $\begin{vmatrix} Z_1 \\ Z_2 \\ Z_3 \end{vmatrix}$

Then, the multiplication of transpose matrix of Z, hessian matrix of C_g and Z, followed by,

$$Z^T H\,Z = |Z_1 \quad Z_2 \quad Z_3| \begin{vmatrix} 0 & 2a\,L\,K_1 & a\,L^2K_2 \\ 2a\,L\,K_1 & 2a\,W\,K_1 & 2a\,WL\,K_2 \\ a\,L^2K_2 & 2a\,WL\,K_2 & a\,WL^2\,K_3 \end{vmatrix} \begin{vmatrix} Z_1 \\ Z_2 \\ Z_3 \end{vmatrix}$$

$= Z_1(2aLK_1Z_2 + a\,L^2K_2Z_3) + 2aZ_2{}^2(L\,K_1 + W\,K_1 + WL\,K_2) + a\,LZ_3{}^2(L\,K_2 + 2WK_2 + WLK_3)$

The above equation is greater than or equal to 0 for every non zero value of Z column vector. And the above expression is positive semidefinite for all positive values of Z. So, C_g is convex.

Suppose for equation (4.2)

$c = \frac{3}{2}\{\frac{\mu C_{dep}(\frac{KT}{q})^3}{2n\pi(cox)^2}\} = \frac{3 \times \cdot 14 \times (e^{-3})^2 \times (\cdot 026)^3}{2 \times 2n\pi\,(cox)^2} = 1\cdot 31 \times 10^{-9}$

$d = \{1 - exp(-\frac{V_{ds}}{\frac{KT}{q}})\}^2 = \cdot 95$

$j = \frac{q}{nKT} = 25.64$

Substituting c, d, j in equation (4.2) it found as,

$F_t = \frac{c}{L^3} \times d \times \{\frac{\exp\{2j(V_{gs} - V_t)\}}{3(V_{gs} - V_t)^2 - j(V_{gs} - V_t)^3}\}$ ……………………………………………………(4.4)

Then, second order partial derivative of equation (4.4) with respect to W, L and V_{gs} followed by,

1. $\frac{\partial^2 \mathrm{Ft}}{\partial W^2} = 0$
2. $\frac{\partial^2 \mathrm{Ft}}{\partial W \partial L} = 0$
3. $\frac{\partial^2 \mathrm{Ft}}{\partial W \partial V_{gs}} = 0$
4. Same as $\frac{\partial^2 \mathrm{Ft}}{\partial W \partial L} = 0$
5. $\frac{\partial^2 \mathrm{Ft}}{\partial L^2} = \frac{12c}{L^5} \times d \times \frac{e^{2j(V_{gs} - V_t)}}{3(V_{gs} - V_t)^2 - j(V_{gs} - V_t)^3}$

   Here $K_4 = \frac{e^{2j(V_{gs} - V_t)}}{3(V_{gs} - V_t)^2 - j(V_{gs} - V_t)^3}$ = .0114 [taking $V_{gs} = \cdot 22$]
6. $\frac{\partial^2 \mathrm{Ft}}{\partial L \partial V_{gs}} = \frac{-3cd \times K_5}{L^4}$

Here $K_5 =$

$$\frac{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3\times 2j\times e^{2j(V_{gs}-V_t)}-e^{2j(V_{gs}-V_t)}\times\{6(V_{gs}-V_t)-3j(V_{gs}-V_t)^2\}}{\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3\}^2}$$

$= \cdot 78$

7. Same as $\frac{\partial^2 \mathrm{Ft}}{\partial W \partial V_{gs}} = 0$
8. Same as $\frac{\partial^2 \mathrm{Ft}}{\partial L \partial V_{gs}} = \frac{-3cd\times K_5}{L^4}$
9. $\frac{\partial^2 \mathrm{Ft}}{\partial {V_{gs}}^2} = \frac{c\ d\ K_6}{L^3}$

Here, K_6

$$= \left[\frac{[\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3\times(2j)^2\times e^{2j(V_{gs}-V_t)}+2j\times e^{2j(V_{gs}-V_t)}\times\{6(V_{gs}-V_t)-3j(V_{gs}-V_t)^2\}}{[\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3]^4} - \frac{\{e^{2j(V_{gs}-V_t)}\{6-6j(V_{gs}-V_t)^2\}+\{2j\times e^{2j(V_{gs}-V_t)}\times\{6(V_{gs}-V_t)-3j(V_{gs}-V_t)^2\}}{[\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3]^4}\right]$$

$$\times \{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3\}^2 - \frac{\left[\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3\times 2j\times e^{2j(V_{gs}-V_t)}\right]-\left[e^{2j(V_{gs}-V_t)}\times\{6(V_{gs}-V_t)-3j(V_{gs}-V_t)^2\}\right]}{[\{3(V_{gs}-V_t)^2-j(V_{gs}-V_t)^3]^4}\times$$

$$\{6(V_{gs}-V_t)^2-2j(V_{gs}-V_t)^3\}$$

= 8883.30

Then, the Hessian matrix for F_t as follows,

$$\mathrm{H} = \begin{vmatrix} \frac{\partial^2 f_t}{\partial W^2} & \frac{\partial^2 f_t}{\partial W \partial L} & \frac{\partial^2 f_t}{\partial W \partial V_{gs}} \\ \frac{\partial^2 f_t}{\partial L \partial W} & \frac{\partial^2 f_t}{\partial L^2} & \frac{\partial^2 f_t}{\partial L \partial V_{gs}} \\ \frac{\partial^2 f_t}{\partial V_{gs} \partial W} & \frac{\partial^2 f_t}{\partial V_{gs} \partial L} & \frac{\partial^2 f_t}{\partial {V_{gs}}^2} \end{vmatrix} = \begin{vmatrix} 0 & 0 & 0 \\ 0 & \frac{12\mathrm{cdK_4}}{\mathrm{L^5}} & \frac{-3cd\times K_5}{L^4} \\ 0 & \frac{-3cd\times K_5}{L^4} & \frac{c\ d\ K_6}{L^3} \end{vmatrix}$$

Assume Z= $\begin{vmatrix} Z_1 \\ Z_2 \\ Z_3 \end{vmatrix}$

Then, the multiplication of transpose matrix of Z, hessian matrix of F_t and Z, followed by,

$$Z^T \text{H Z} = |Z_1 \quad Z_2 \quad Z_3| \begin{vmatrix} 0 & 0 & 0 \\ 0 & \frac{12cdK_4}{L^5} & \frac{-3cd \times K_5}{L^4} \\ 0 & \frac{-3cd \times K_5}{L^4} & \frac{c\ d\ K_6}{L^3} \end{vmatrix} \begin{vmatrix} Z_1 \\ Z_2 \\ Z_3 \end{vmatrix}$$

$$= \left|0 \quad \left(\frac{12cdK_4Z_2}{L^5} - \frac{3cd\ K_5Z_3}{L^4}\right) \quad \left(\frac{c\ d\ K_6Z_3}{L^3} - \frac{3cd\ K_5Z_2}{L^4}\right)\right| \begin{vmatrix} Z_1 \\ Z_2 \\ Z_3 \end{vmatrix}$$

$$= \left|0 + Z_2\left(\frac{12cdK_4Z_2}{L^5} - \frac{3cd\ K_5Z_3}{L^4}\right) + Z_3\left(\frac{c\ d\ K_6Z_3}{L^3} - \frac{3cd\ K_5Z_2}{L^4}\right)\right|$$

As, values of Z positive,

$$= \left(\frac{12cdK_4}{L^5} - \frac{3cd\ K_5}{L^4}\right) + \left(\frac{c\ d\ K_6}{L^3} - \frac{3cd\ K_5}{L^4}\right) \geq 0$$

The above expression is positive semidefinite for all positive values of Z. So, Ft is convex. That's why the desired objective function, $Z = \alpha F_t - (1- \alpha C_g)$ is convex.

4.2 Solution Approach:

MATLAB is a multi-paradigm numerical computing environment. It allows matrix manipulation for plotting of function and data. MATLAB provides different kind of optimization toolbox and optimization function for determining the optimized value. The above problem deals with non-linear equations. To perform optimization in MATLAB, MATLAB built in function "fmincon" have been used here. Here, α varied from 0 to 1. F_t maximized and C_g minimized, when α equals to 1.

So the output characteristics for Alpha (α) vs objective function (Z), Alpha (α) vs channel length (L), Alpha (α) vs channel width (W), Alpha (α) vs gate voltage (Vgs), Alpha (α) vs transition frequency (F_t) and Alpha (α) vs gate capacitance (C_g) is illustrated bellow. The curves bellow obtained varying alphas value from 0 to 1 in interval of 0.005. For observation, total 201 values of alpha were taken along x-axis and objective function, channel length, channel width, gate voltage, transition frequency and gate capacitance along y-axis.

4.2.1 Output Characteristics of Objective Function (Z) with Respect to Alpha (α):

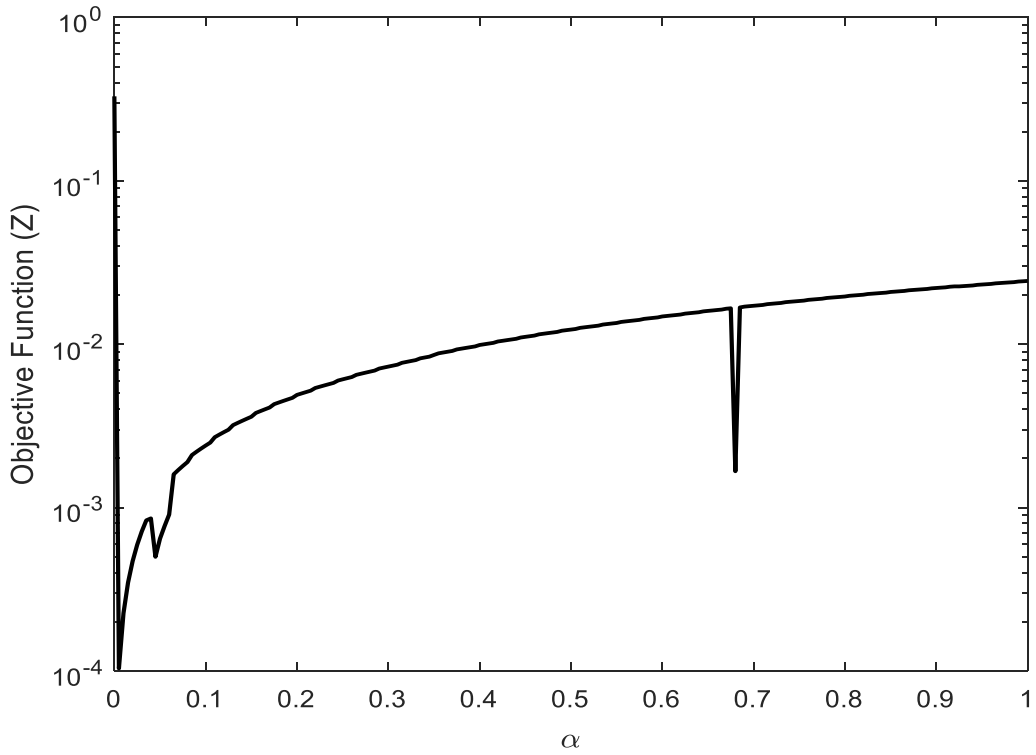

Figure 4.1: Illustration of α vs Z characteristics.

From Fig. 4.1, the change in objective function (Z) for various values of alpha (α) is observed. It is evident that with the change of alpha the objective function changes. The initial value of the objective function was higher.

4.2.2 Output Characteristics of Channel Length (L) with Respect to Alpha (α):

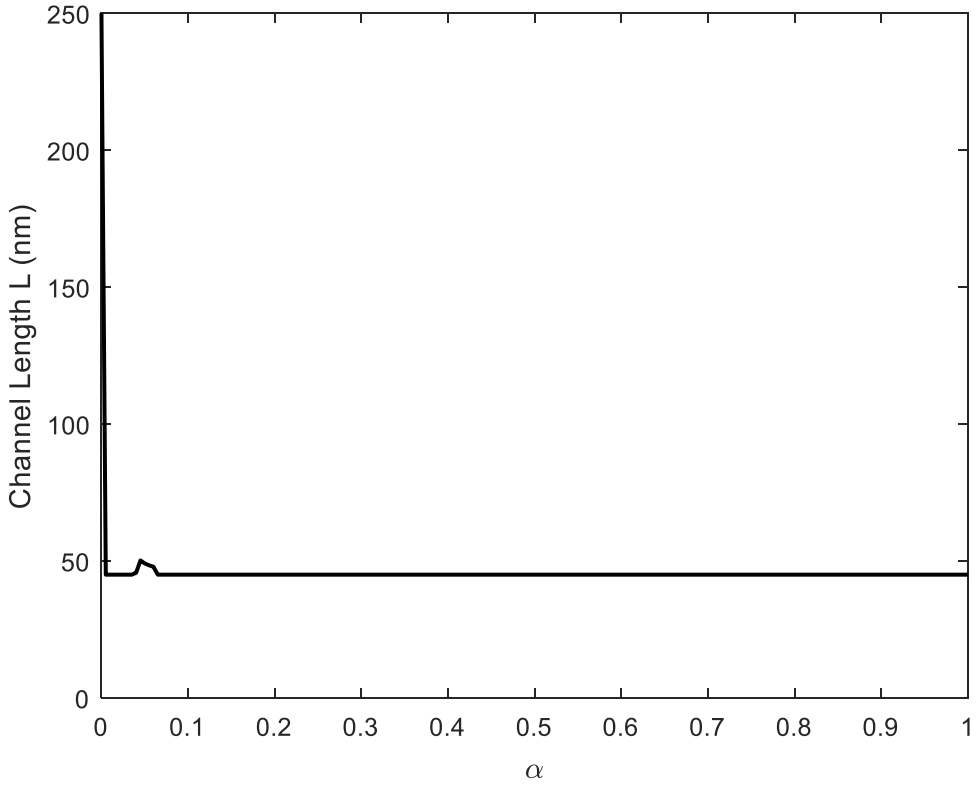

Figure 4.2: Illustration of α vs channel length (L) characteristics

From Fig. 4.2, the change in channel length (L) for various values of alpha (α) is observed. It is evident that with the change of alpha the channel length was initially changed and when alpha increased then channel length becomes constant.

4.2.3 Output Characteristics of Channel Width (W) with Respect to Alpha (α):

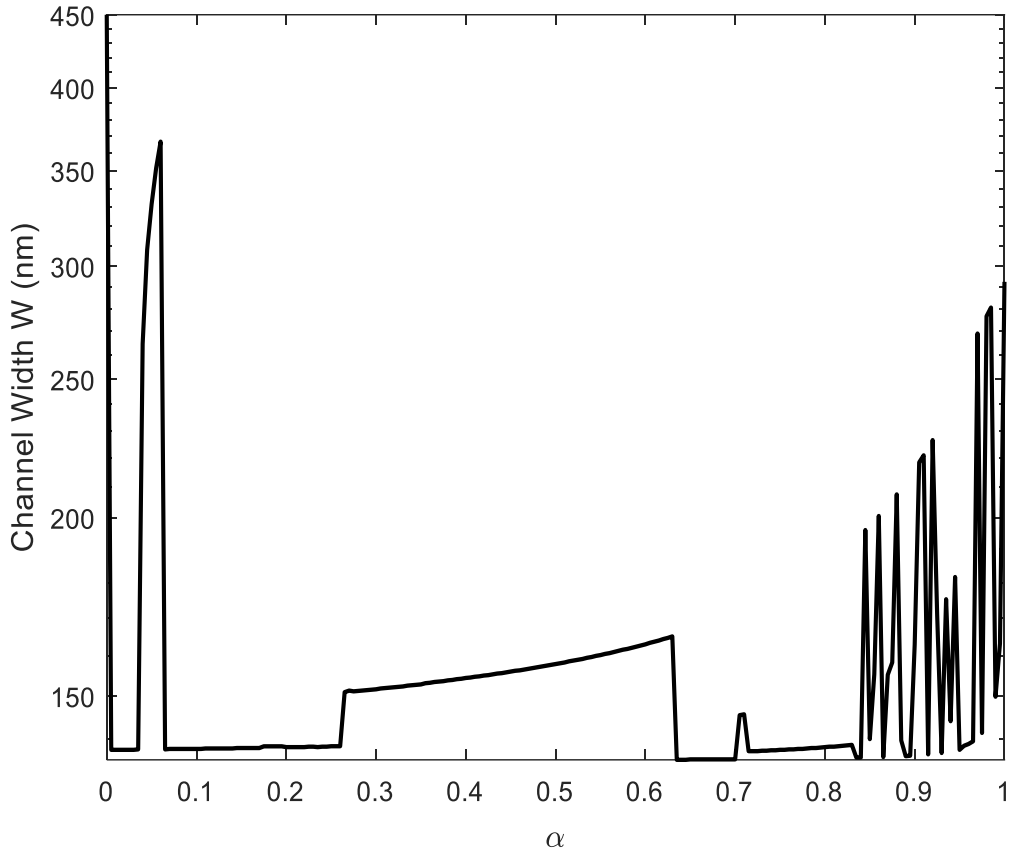

Figure 4.3: Illustration of α vs channel width (W) characteristics

From the above Fig.4.3, it is observed that with the change in alpha the channel width changes. It is clear that with the increase in alpha, the channel width randomly fluctuate above .8, alpha value.

4.2.4 Output Characteristics of Gate Voltage (V_{gs}) with Respect to Alpha (α):

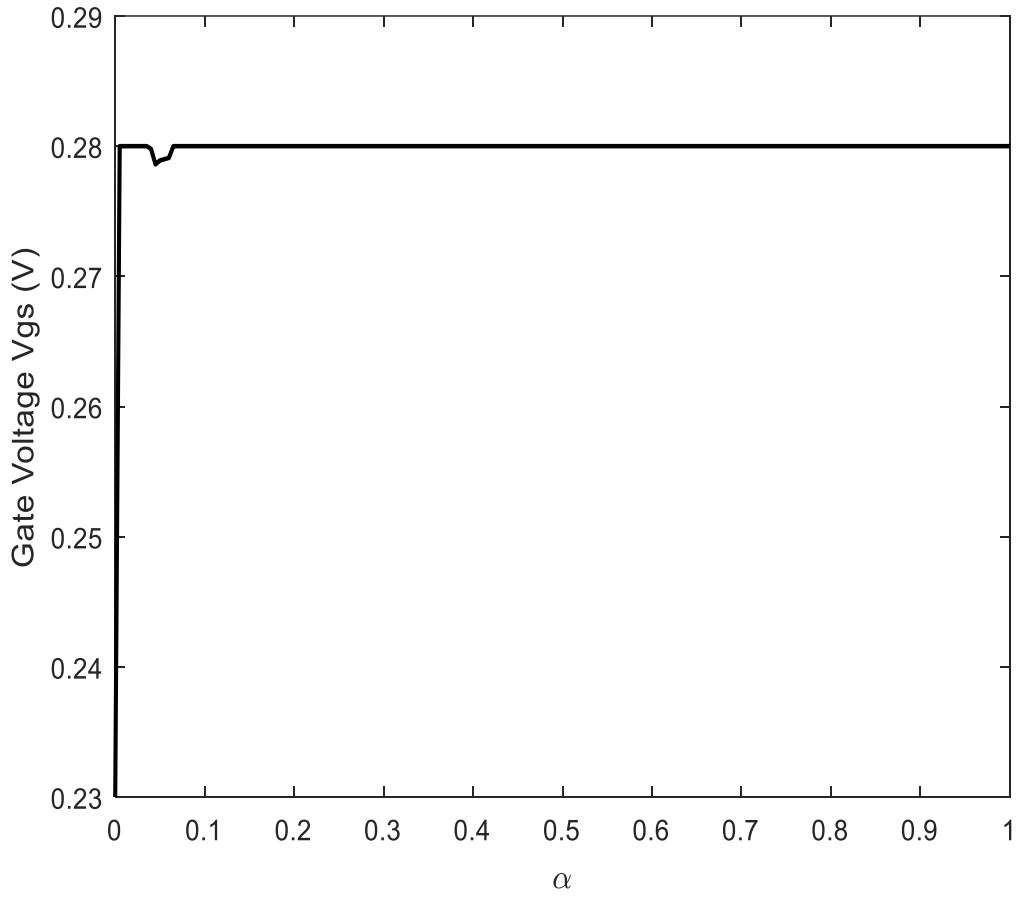

Figure 4.4: Illustration of α vs gate voltage (V_{gs}) characteristics.

From the above Fig.4.4, it is observed that the value of gate voltage initially change a little and finally it becomes constant with the increase of alpha (α).

4.2.5 Output Characteristics of Transition Frequency (F_t) with Respect to Alpha (α):

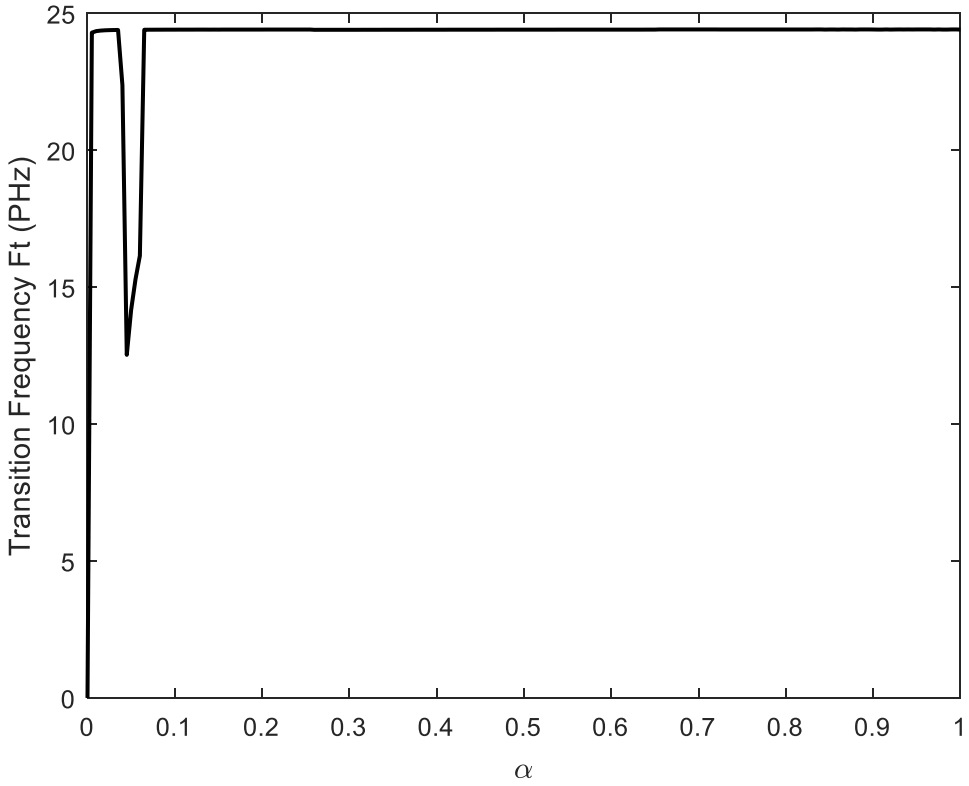

Figure 4.5: Illustration of α vs transition frequency F_t characteristics.

From the above Fig.4.5, it is observed that the value of transition frequency initially changes a little and finally it becomes constant with the increase of alpha (α).

4.2.6 Output Characteristics of Gate Capacitance (C_g) with Respect to Alpha (α):

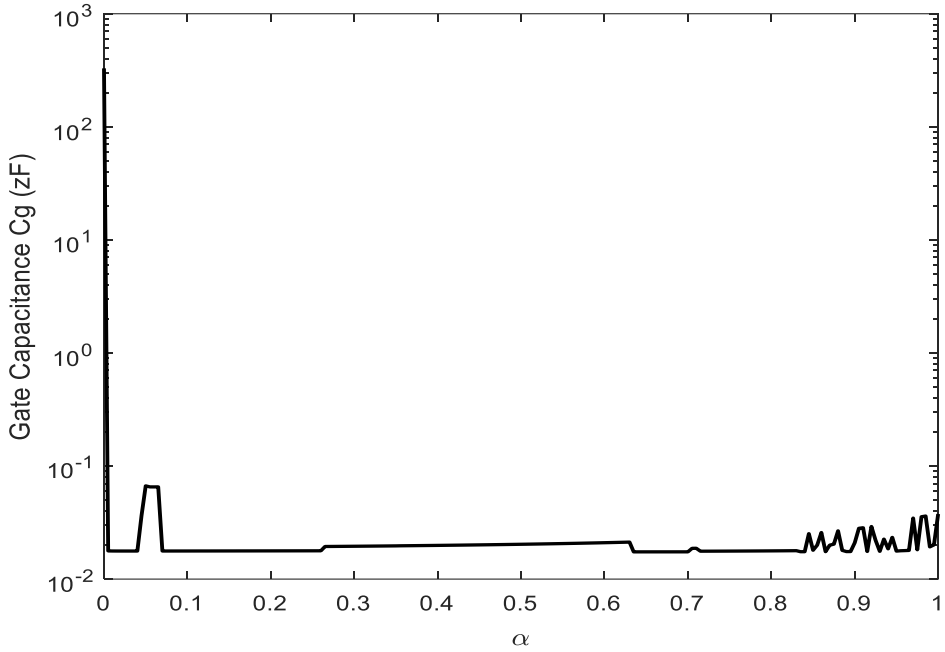

Figure 4.6: Illustration of α vs gate capacitance $C_g$characteristics.

From the above Fig.4.6, it is observed that initially, the value of gate voltage initially changes a little, then it act as constant and above .8, alpha value it randomly fluctuates with the increase of alpha (α).

For all the values of alpha (α), corresponding observed values of the objective function, channel length, channel width, gate voltage, transition frequency and gate capacitance are given bellow in the table 4.1;

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g).

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0	0.3290	250	450	0.23	2.1141×10^{11}	3.2896×10^{-19}
0.005	1.038×10^{-4}	45	137.5	0.28	2.4293×10^{16}	1.7753×10^{-23}
0.010	2.2593×10^{-4}	45	137.5	0.28	2.4348×10^{16}	1.7725×10^{-23}
0.015	3.4806×10^{-4}	45	137.5	0.28	2.4368×10^{16}	1.7715×10^{-23}
0.020	4.7019×10^{-4}	45	137.5	0.28	2.4378×10^{16}	1.7711×10^{-23}
0.025	5.9232×10^{-4}	45	137.5	0.28	2.4384×10^{16}	1.7710×10^{-23}
0.030	7.1445×10^{-4}	45	137.5	0.28	2.4388×10^{16}	1.7709×10^{-23}
0.035	8.3658×10^{-4}	45	137.6	0.28	2.4391×10^{16}	1.7709×10^{-23}
0.040	8.6001×10^{-4}	45.7	264.6	0..2798	2.2375×10^{16}	3.6450×10^{-23}
0.045	4.9995×10^{-4}	50.2	308	0.2786	1.2527×10^{16}	6.6747×10^{-23}
0.050	6.4634×10^{-4}	49.1	331.6	0.2789	1.4169×10^{16}	6.5394×10^{-23}
0.055	7.7101×10^{-4}	48.4	351.3	0.2790	1.5287×10^{16}	6.5356×10^{-23}
0.060	9.0737×10^{-4}	47.9	366.7	0.2791	1.6148×10^{16}	6.5423×10^{-23}
0.065	0.0016	45	137.6	0.28	2.4399×10^{16}	1.7715×10^{-23}
0.070	0.0017	45	137.7	0.28	2.44×10^{16}	1.7716×10^{-23}
0.075	0.0018	45	137.7	0.28	2.44×10^{16}	1.7718×10^{-23}
0.080	0.0019	45	137.7	0.28	2.4401×10^{16}	1.7719×10^{-23}
0.085	0.0021	45	137.7	0.28	2.4401×10^{16}	1.7721×10^{-23}
0.090	0.0022	45	137.7	0.28	2.4402×10^{16}	1.7723×10^{-23}
0.095	0.0023	45	137.7	0.28	2.4402×10^{16}	1.7724×10^{-23}
0.100	0.0024	45	137.7	0.28	2.4402×10^{16}	1.7726×10^{-23}
0.105	0.0025	45	137.8	0.28	2.4403×10^{16}	1.7728×10^{-23}
0.110	0.0027	45	137.8	0.28	2.4403×10^{16}	1.7730×10^{-23}
0.115	0.0028	45	137.8	0.28	2.4403×10^{16}	1.7732×10^{-23}
0.120	0.0029	45	137.8	0.28	2.4403×10^{16}	1.7733×10^{-23}
0.125	0.0030	45	137.8	0.28	2.4404×10^{16}	1.7735×10^{-23}
0.130	0.0032	45	137.8	0.28	2.4404×10^{16}	1.7737×10^{-23}
0.135	0.0033	45	137.8	0.28	2.4404×10^{16}	1.7739×10^{-23}
0.140	0.0034	45	137.9	0.28	2.4403×10^{16}	1.7741×10^{-23}
0.145	0.0035	45	137.9	0.28	2.4404×10^{16}	1.7743×10^{-23}
0.150	0.0036	45	137.9	0.28	2.4403×10^{16}	1.7745×10^{-23}
0.155	0.0038	45	137.9	0.28	2.4405×10^{16}	1.7748×10^{-23}
0.160	0.0039	45	137.9	0.28	2.4405×10^{16}	1.7750×10^{-23}
0.165	0.0040	45	137.9	0.28	2.4405×10^{16}	1.7752×10^{-23}
0.170	0.0041	45	138.28	0.28	2.4405×10^{16}	1.7754×10^{-23}

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g). (continued)

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0.175	0.0043	45	138.28	0.28	2.4405×10^{16}	1.7756×10^{-23}
0.180	0.0044	45	138.28	0.28	2.4405×10^{16}	1.7759×10^{-23}
0.185	0.0045	45	138.28	0.28	2.4405×10^{16}	1.7761×10^{-23}
0.190	0.0046	45	138.28	0.28	2.4405×10^{16}	1.7763×10^{-23}
0.195	0.0047	45	138.1	0.28	2.4405×10^{16}	1.7765×10^{-23}
0.200	0.0049	45	138.1	0.28	2.4405×10^{16}	1.7768×10^{-23}
0.205	0.0050	45	138.1	0.28	2.4406×10^{16}	1.7770×10^{-23}
0.210	0.0051	45	138.1	0.28	2.4406×10^{16}	1.7773×10^{-23}
0.215	0.0052	45	138.1	0.28	2.4406×10^{16}	1.7775×10^{-23}
0.220	0.0054	45	138.2	0.28	2.4406×10^{16}	1.7778×10^{-23}
0.225	0.0055	45	138.2	0.28	2.4406×10^{16}	1.7780×10^{-23}
0.230	0.0056	45	138.1	0.28	2.4406×10^{16}	1.7783×10^{-23}
0.235	0.0057	45	138.2	0.28	2.4406×10^{16}	1.7786×10^{-23}
0.240	0.0058	45	138.2	0.28	2.4406×10^{16}	1.7788×10^{-23}
0.245	0.0060	45	138.3	0.28	2.4406×10^{16}	1.7791×10^{-23}
0.250	0.0061	45	138.3	0.28	2.4406×10^{16}	1.7794×10^{-23}
0.255	0.0062	45	138.3	0.28	2.4406×10^{16}	1.7796×10^{-23}
0.260	0.0063	45	150.9	0.28	2.4396×10^{16}	1.9424×10^{-23}
0.265	0.0065	45	151.28	0.28	2.4397×10^{16}	1.9437×10^{-23}
0.270	0.0066	45	151.1	0.28	2.4397×10^{16}	1.9450×10^{-23}
0.275	0.0067	45	151.2	0.28	2.4397×10^{16}	1.9464×10^{-23}
0.280	0.0068	45	151.3	0.28	2.4397×10^{16}	1.9477×10^{-23}
0.285	0.0069	45	151.4	0.28	2.4397×10^{16}	1.9491×10^{-23}
0.290	0.0071	45	151.5	0.28	2.4398×10^{16}	1.9505×10^{-23}
0.295	0.0070	45	151.6	0.28	2.4398×10^{16}	1.9519×10^{-23}
0.3	0.0073	45	151.8	0.28	2.4398×10^{16}	1.9533×10^{-23}
0.305	0.0074	45	151.9	0.28	2.4398×10^{16}	1.9548×10^{-23}
0.310	0.0075	45	152.0	0.28	2.4398×10^{16}	1.9562×10^{-23}
0.315	0.0077	45	152.1	0.28	2.4399×10^{16}	1.9577×10^{-23}
0.320	0.0078	45	152.2	0.28	2.4399×10^{16}	1.9592×10^{-23}
0.325	0.0079	45	152.3	0.28	2.4399×10^{16}	1.9608×10^{-23}
0.330	0.0080	45	152.5	0.28	2.4399×10^{16}	1.9623×10^{-23}
0.335	0.0082	45	152.6	0.28	2.4399×10^{16}	1.9639×10^{-23}
0.345	0.008	45	152.7	0.28	2.4399×10^{16}	1.9655×10^{-23}

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g). (continued)

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0.350	0.0084	45	152.8	0.28	2.4399×10^{16}	1.9671×10^{-23}
0.355	0.0086	45	153.1	0.28	2.4400×10^{16}	1.9704×10^{-23}
0.360	0.0088	45	153.2	0.28	2.4400×10^{16}	1.9721×10^{-23}
0.365	0.0089	45	153.4	0.28	2.4400×10^{16}	1.9739×10^{-23}
0.370	0.0090	45	153.5	0.28	2.4400×10^{16}	1.9756×10^{-23}
0.375	0.0091	45	153.6	0.28	2.4400×10^{16}	1.9774×10^{-23}
0.380	0.0093	45	153.8	0.28	2.4400×10^{16}	1.9792×10^{-23}
0.385	0.0094	45	153.9	0.28	2.4400×10^{16}	1.9810×10^{-23}
0.390	0.0095	45	154.1	0.28	2.4400×10^{16}	1.9828×10^{-23}
0.395	0.0096	45	154.2	0.28	2.4401×10^{16}	1.9847×10^{-23}
0.400	0.0097	45	154.4	0.28	2.4401×10^{16}	1.9867×10^{-23}
0.405	0.0099	45	154.5	0.28	2.4401×10^{16}	1.9886×10^{-23}
0.410	0.0100	45	154.7	0.28	2.4401×10^{16}	1.9906×10^{-23}
0.415	0.0101	45	154.8	0.28	2.4401×10^{16}	1.9926×10^{-23}
0.420	0.0102	45	155.0	0.28	2.4401×10^{16}	1.9946×10^{-23}
0.425	0.0104	45	155.1	0.28	2.4401×10^{16}	1.9967×10^{-23}
0.430	0.0105	45	155.3	0.28	2.4401×10^{16}	1.9988×10^{-23}
0.435	0.0106	45	155.5	0.28	2.4401×10^{16}	2.0009×10^{-23}
0.440	0.0107	45	155.6	0.28	2.4401×10^{16}	2.0031×10^{-23}
0.445	0.0108	45	155.8	0.28	2.4401×10^{16}	2.0053×10^{-23}
0.450	0.0110	45	156.0	0.28	2.4402×10^{16}	2.0075×10^{-23}
0.455	0.0111	45	156.2	0.28	2.4402×10^{16}	2.0098×10^{-23}
0.460	0.0112	45	156.3	0.28	2.4402×10^{16}	2.0121×10^{-23}
0.465	0.0113	45	156.5	0.28	2.4402×10^{16}	2.0145×10^{-23}
0.470	0.0115	45	156.7	0.28	2.4402×10^{16}	2.0169×10^{-23}
0.475	0.0116	45	156.9	0.28	2.4402×10^{16}	2.0194×10^{-23}
0.480	0.0117	45	157.1	0.28	2.4402×10^{16}	2.0218×10^{-23}
0.485	0.0118	45	157.3	0.28	2.4402×10^{16}	2.0244×10^{-23}
0.490	0.0119	45	157.5	0.28	2.4402×10^{16}	2.0270×10^{-23}
0.495	0.0121	45	157.7	0.28	2.4402×10^{16}	2.0296×10^{-23}
0.500	0.0122	45	157.9	0.28	2.4402×10^{16}	2.0323×10^{-23}
0.505	0.0123	45	158.1	0.28	2.4402×10^{16}	2.0350×10^{-23}
0.510	0.0124	45	158.3	0.28	2.4402×10^{16}	2.0378×10^{-23}
0.515	0.0126	45	158.6	0.28	2.4402×10^{16}	2.0406×10^{-23}
0.520	0.0127	45	158.8	0.28	2.4403×10^{16}	2.0435×10^{-23}

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g). (continued)

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0.525	0.0128	45	159.0	0.28	2.4403×10^{16}	2.0464×10^{-23}
0.530	0.0129	45	159.2	0.28	2.4403×10^{16}	2.0494×10^{-23}
0.535	0.0130	45	159.5	0.28	2.4403×10^{16}	2.0524×10^{-23}
0.540	0.0132	45	159.7	0.28	2.4403×10^{16}	2.0555×10^{-23}
0.545	0.0133	45	160.0	0.28	2.4403×10^{16}	2.0587×10^{-23}
0.550	0.0134	45	160.2	0.28	2.4403×10^{16}	2.0619×10^{-23}
0.555	0.0135	45	160.5	0.28	2.4403×10^{16}	2.0652×10^{-23}
0.560	0.0137	45	160.7	0.28	2.4403×10^{16}	2.0686×10^{-23}
0.565	0.0138	45	161.0	0.28	2.4403×10^{16}	2.0720×10^{-23}
0.570	0.0139	45	161.3	0.28	2.4403×10^{16}	2.0755×10^{-23}
0.575	0.0140	45	161.6	0.28	2.4403×10^{16}	2.0791×10^{-23}
0.580	0.0141	45	161.8	0.28	2.4403×10^{16}	2.0828×10^{-23}
0.585	0.0143	45	162.1	0.28	2.4403×10^{16}	2.0865×10^{-23}
0.590	0.0144	45	162.4	0.28	2.4403×10^{16}	2.0903×10^{-23}
0.595	0.0145	45	162.7	0.28	2.4403×10^{16}	2.0942×10^{-23}
0.600	0.0146	45	163.0	0.28	2.4403×10^{16}	2.0982×10^{-23}
0.605	0.0148	45	163.4	0.28	2.4403×10^{16}	2.1023×10^{-23}
0.610	0.0149	45	163.7	0.28	2.4403×10^{16}	2.1065×10^{-23}
0.615	0.0150	45	164.0	0.28	2.4403×10^{16}	2.1107×10^{-23}
0.620	0.0151	45	164.4	0.28	2.4404×10^{16}	2.1151×10^{-23}
0.625	0.0152	45	164.7	0.28	2.4404×10^{16}	2.1195×10^{-23}
0.630	0.0154	45	165.1	0.28	2.4404×10^{16}	2.1241×10^{-23}
0.635	0.0155	45	135.3	0.28	2.4409×10^{16}	1.7414×10^{-23}
0.640	0.0156	45	135.3	0.28	2.4409×10^{16}	1.7414×10^{-23}
0.645	0.0157	45	135.3	0.28	2.4409×10^{16}	1.7415×10^{-23}
0.650	0.0159	45	135.4	0.28	2.4409×10^{16}	1.7416×10^{-23}
0.655	0.0160	45	135.4	0.28	2.4409×10^{16}	1.7416×10^{-23}
0.660	0.0161	45	135.4	0.28	2.4409×10^{16}	1.7417×10^{-23}
0.665	0.0162	45	135.4	0.28	2.4409×10^{16}	1.7418×10^{-23}
0.670	0.0163	45	135.4	0.28	2.4409×10^{16}	1.7419×10^{-23}
0.675	0.0165	45	135.4	0.28	2.4409×10^{16}	1.7419×10^{-23}
0.680	0.0166	45	135.4	0.28	2.4409×10^{16}	1.7420×10^{-23}
0.685	0.0167	45	135.4	0.28	2.4409×10^{16}	1.7421×10^{-23}
0.690	0.0168	45	135.4	0.28	2.4409×10^{16}	1.7422×10^{-23}
0.695	0.0170	45	135.4	0.28	2.4409×10^{16}	1.7422×10^{-23}

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g). (continued)

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0.700	0.0171	45	135.4	0.28	2.4409×10^{16}	1.7423×10^{-23}
0.705	0.0172	45	145.4	0.28	2.4408×10^{16}	1.8709×10^{-23}
0.710	0.0173	45	145.6	0.28	2.4408×10^{16}	1.8734×10^{-23}
0.715	0.0174	45	137.2	0.28	2.4408×10^{16}	1.7649×10^{-23}
0.720	0.0176	45	137.2	0.28	2.4408×10^{16}	1.7654×10^{-23}
0.725	0.0177	45	137.2	0.28	2.4408×10^{16}	1.7659×10^{-23}
0.730	0.0178	45	137.3	0.28	2.4408×10^{16}	1.7664×10^{-23}
0.735	0.0179	45	137.3	0.28	2.4408×10^{16}	1.7670×10^{-23}
0.740	0.0181	45	137.4	0.28	2.4408×10^{16}	1.7676×10^{-23}
0.745	0.0182	45	137.4	0.28	2.4408×10^{16}	1.7681×10^{-23}
0.750	0.0183	45	137.5	0.28	2.4408×10^{16}	1.7688×10^{-23}
0.755	0.0184	45	137.5	0.28	2.4408×10^{16}	1.7694×10^{-23}
0.760	0.0185	45	137.6	0.28	2.4408×10^{16}	1.7701×10^{-23}
0.765	0.0187	45	137.6	0.28	2.4408×10^{16}	1.7708×10^{-23}
0.770	0.0188	45	137.7	0.28	2.4408×10^{16}	1.7715×10^{-23}
0.775	0.0189	45	137.7	0.28	2.4408×10^{16}	1.7723×10^{-23}
0.780	0.0190	45	137.8	0.28	2.4408×10^{16}	1.7731×10^{-23}
0.785	0.0192	45	137.9	0.28	2.4408×10^{16}	1.7739×10^{-23}
0.790	0.0193	45	137.9	0.28	2.4408×10^{16}	1.7748×10^{-23}
0.795	0.0194	45	138.0	0.28	2.4408×10^{16}	1.7757×10^{-23}
0.800	0.0195	45	138.1	0.28	2.4408×10^{16}	1.7766×10^{-23}
0.805	0.0196	45	138.2	0.28	2.4408×10^{16}	1.7776×10^{-23}
0.810	0.0198	45	138.2	0.28	2.4408×10^{16}	1.7787×10^{-23}
0.815	0.0199	45	138.3	0.28	2.4408×10^{16}	1.7798×10^{-23}
0.820	0.0200	45	138.4	0.28	2.4408×10^{16}	1.7810×10^{-23}
0.825	0.0201	45	138.5	0.28	2.4408×10^{16}	1.7822×10^{-23}
0.830	0.0203	45	138.6	0.28	2.4408×10^{16}	1.7835×10^{-23}
0.835	0.0204	45	135.8	0.28	2.4409×10^{16}	1.7467×10^{-23}
0.840	0.0205	45	135.8	0.28	2.4409×10^{16}	1.7470×10^{-23}
0.845	0.0206	45	196.0	0.28	2.4405×10^{16}	2.5217×10^{-23}
0.850	0.0207	45	139.9	0.28	2.4408×10^{16}	1.7998×10^{-23}
0.855	0.0209	45	155.3	0.28	2.4408×10^{16}	1.9978×10^{-23}
0.860	0.0210	45	200.5	0.28	2.4405×10^{16}	2.5801×10^{-23}
0.865	0.0211	45	135.9	0.28	2.4409×10^{16}	1.7488×10^{-23}
0.870	0.0212	45	155.2	0.28	2.4408×10^{16}	1.9968×10^{-23}
0.875	0.0214	45	158.3	0.28	2.4408×10^{16}	2.0369×10^{-23}
0.880	0.0215	45	207.6	0.28	2.4405×10^{16}	2.6713×10^{-23}

Table 4.1: Alpha (α) vs corresponding values of objective function (Z), channel length (L), channel width (W), gate voltage (V_{gs}), transition frequency (F_t), gate capacitance (C_g). (continued)

Alpha α	Objective Function A	Channel Length L (nm)	Channel Width W (nm)	Gate Voltage V_{gs} (v)	Transition Frequency F_t (Hz)	Gate Capacitance C_g (F)
0.885	0.0216	45	139.6	0.28	2.4409×10^{16}	1.7956×10^{-23}
0.890	0.0217	45	136.1	0.28	2.4409×10^{16}	1.7515×10^{-23}
0.895	0.0218	45	136.2	0.28	2.4409×10^{16}	1.7522×10^{-23}
0.900	0.0220	45	162.9	0.28	2.4408×10^{16}	2.0963×10^{-23}
0.905	0.0221	45	218.6	0.28	2.4405×10^{16}	2.8130×10^{-23}
0.910	0.0222	45	221.1	0.28	2.4405×10^{16}	2.8458×10^{-23}
0.915	0.0223	45	136.5	0.28	2.4409×10^{16}	1.7559×10^{-23}
0.920	0.0225	45	226.6	0.28	2.4405×10^{16}	2.9165×10^{-23}
0.925	0.0226	45	171.1	0.28	2.4408×10^{16}	2.2015×10^{-23}
0.930	0.0227	45	136.8	0.28	2.4409×10^{16}	1.7601×10^{-23}
0.935	0.0228	45	175.3	0.28	2.4408×10^{16}	2.2560×10^{-23}
0.940	0.0229	45	144.0	0.28	2.4409×10^{16}	1.8527×10^{-23}
0.945	0.0231	45	181.7	0.28	2.4408×10^{16}	2.3378×10^{-23}
0.950	0.0232	45	137.5	0.28	2.4409×10^{16}	1.7688×10^{-23}
0.955	0.0233	45	138.4	0.28	2.4409×10^{16}	1.7810×10^{-23}
0.960	0.0234	45	138.8	0.28	2.4409×10^{16}	1.7864×10^{-23}
0.965	0.0236	45	139.4	0.28	2.4409×10^{16}	1.7933×10^{-23}
0.970	0.0237	45	269.1	0.28	2.4405×10^{16}	3.4627×10^{-23}
0.975	0.0238	45	141.3	0.28	2.4409×10^{16}	1.8180×10^{-23}
0.980	0.0239	45	276.7	0.28	2.4405×10^{16}	3.5607×10^{-23}
0.985	0.0240	45	280.6	0.28	2.4405×10^{16}	3.6109×10^{-23}
0.990	0.0242	45	149.8	0.28	2.4409×10^{16}	1.9278×10^{-23}
0.995	0.0243	45	163.2	0.28	2.4409×10^{16}	2.0993×10^{-23}
1.000	0.0244	45	292.5	0.28	2.4405×10^{16}	3.7641×10^{-23}

4.3 Summary:

In this chapter, using F_t and C_g the objective function (Z) was formulated. It is found that the objective function was convex. And using MATLAB, the optimization was done. After optimization, it has been found that, when alpha value is 0.635 and 0.640 the objective function maximized in such a way that transition frequency becomes highest (2.4409×10^{16}) and gate capacitance becomes lowest (1.7414×10^{-23}).

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion:

Transistors are the building blocks of integrated circuit. Modern CPUs contain millions of individual transistors that are microscopic in size. Transistors can likewise change the measure of current being sent. As a result of their minimum cost and high quality, resistors have generally replaced, also vaccum tubes for sound enhancement purposes. While in the early hours transistors were sufficiently expansive to hold close by, present day transistors are so little they can't be seen with the uncovered eye. With increasing number of transistors due to technology scaling and improved lithography technology, the focus of study over the last decade has been over power management and speed improvements. This microscopic size permits chip makers to fit a huge number of transistors into a solitary processor. Also it reduce the power consumptions that reduce loses of power. So in our thesis, we optimize our MOSFET's performance parameters such as channel length (L), channel width (W), applied gate voltage (V_{gs}) to reduce MOSFET size, relative capacitance such as gate capacitance (C_g) which is important for high frequency performance at a smaller size and lower input power in which the MOSFET operates at a weak inversion region. We perform convex optimization and get the optimal points at which transition frequency (F_t) will be the maximum and gate capacitance (C_g) will be minimum. We find that when α value is 0.635 and 0.640 the objective function maximized in such a way that transition frequency becomes highest (2.4409×10^{16}) and gate capacitance becomes lowest (1.7414×10^{-23}).This also tells us how we can use the values of α to manipulate the high speed and low voltage performance of a subthreshold mosfet device simultaneously.

As analog circuits are much more difficult to design than those which accomplish the same task digitally but digital circuits are a bit more expensive than an equally taken analog circuit. With these continuous improvement of MOSFET models, the door to analog designs is expanding. As this subthreshold model can be implemented in analog designs, it can help to design self-sufficient power devices in future.

5.2 Future Work:

In our thesis, we do not consider physical level properties of MOSFET to avoid further complexity. For example, random dopant fluctuation caused by variations in the manufacturing process of the device such as line edge roughness and gate length random fluctuation etc. This cause the variations in MOSFET's electrical characteristics such as drain current and transconductance etc. These variations are crucial in the statistical and variability aware design of MOSFET based applications.

Our aim is to take consideration of all physical level properties of MOSFET such as line edge roughness and gate length random fluctuation and make a layout design in CADENCE: EDA tools to get the actual practical response of our design.

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