DECLARATION

This is to certify that the thesis entitled, **"Design and Performance Analysis of Active Inductor Based Voltage Controlled Oscillator in 90nm CMOS Process for Wireless Applications"** is an outcome of the investigation carried out by the authors under the supervision of **Md. Tawfiq Amin PhD, EME**. It is also declared that neither of this thesis nor any part has not been submitted to elsewhere for the award of any other degree or diploma or other similar title or prize.

Thanking you,

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DEDICATION

"Parents were the only ones obligated to love you; from the rest of the world you had to earn it." - Ann Brashares

"No matter how far we come, our parents are always in us." - Brad Meltzer

To our parents…….

Md. Sirazul Islam
Mst. Selina Khatun

Mohammad Ali Hossain
Parvin Akther

Md. Shariful Islam
Mst. Musabbeha Chowdhury

SUPERVISOR'S CERTIFICATION

This is to certify that Md. Ahsanul Kabir Bulbul, Student ID: 201416021; Omar Faruqe, Student ID: 201416043; Md. Monjur Morshed Saikat: Student ID: 201416050; have completed their undergraduate thesis entitled **"Design and Performance Analysis of Active Inductor Based Voltage Controlled Oscillator in 90nm CMOS Process for Wireless Applications"** under my supervision. To the best of my knowledge, the report is their original work and was not submitted elsewhere for other purpose.

_____

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Last but not the least, we are obliged to thank our parents whose love and guidance were the main forces behind every bit of success that we have accomplished so far in our life.

ABSTRACT

This thesis represents the effective design of voltage controlled oscillator which is an integral part of modern RF communication system for varying output frequency with respect to input voltage. In this research ,the indispensable effecting parameters of designing VCO was anatomized properly with view to proceeding the research steps in a beneficial way and comparative analysis of different active inductor models was performed in an efficacious way. In addition, simulations of different active inductors were executed using cadence 6.16 environment which ease to depict the high performing active inductor in insightful research perspective. The simulation results showed the variation of performance of different active inductor models regarding quality factor, power consumption, inductance tunability and frequency range. It highly perspicuous from the simulation results that Weng-Kuo active inductor is superior to other established models due to high quality factor of(4.263@0.9GHz and 2.23 @2.7 GHz) as well as wide frequency range having a value of (7.462 GHz and 11.868GHz). Power consumption was also in optimum level with tenability of inductance and quality factor independently.

These facts intrigued to apply Weng-kuo active inductor for designing a VCO which would show satisfactory frequency range for Bluetooth applications, low phase noise and higher figure of merit with respect to the other cited works . The simulations of our designed VCO was performed via cadence 6.16 environment which has illustrated the performance appropriately .The oscillator yielded a differential output of 0.48 to-0.448 mV @ 2.4GHz and a tuning range of 2.17 GHz to 2.72GHz with a variation of control voltage of 0 V to .8 V. For Vcontrol = 0.4V, the frequency is 2.40887 GHz with a phase noise of -82.34 dBc/Hz@1MHz offset and power consumption was 4.18761 mW. The performance parameters exhibits stability with variation of control voltage along with a high power output that outperforms the other referred works. Performance comparison with several previously designed VCOs clinched that our designed VCO shows unique properties of consuming low power, stability and high power output which indicates the high power efficiency.

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NOMENCLATURE

RFIC	Radio Frequency Integrated Circuits
SoC	System-on-a-Chip
TTL	Transistor-Transistor Logic
PLL	Phase Looked Loop
ISM	Industrial, Scientific and Medical Radio Bands
RF	Radio Frequency
CAD	Computer-Aided Design
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
RF	Radio Frequency
KCL	Kirchoff's Current Law
MOSFET	Metal Oxide Silicon Field Effect Transistor
VCO	Voltage-Controlled Oscillator
EMF	Electromotive Force
FET	Field Effect Transistor
NMOS	Negative Metal Oxide Semiconductor
PMOS	Positive Metal Oxide Semiconductor
Q Factor	Quality Factor
FOM	Figure of Merit
OFDM	Orthogonal Frequency Division Multiplexing

CHAPTER 01

INTRODUCTION

1.1 Motivation

The last decade has witnessed a monumental growth in the communications industry. A significant part of this growth has been fuelled by an invigorated demand to stay connected using multiple forms of wireless communication. Radio frequency integrated circuits (RFIC's), which were often relegated to niche industries like the military and cable television in the past, are now at the heart of the burgeoning communication industry. Low-power, low-cost and high volume have for long been the nom de jeu in the integrated circuit industry [1]. Digital integrated circuits have relied on the high levels of integration and scalability that CMOS processes have offered to up the ante in performance metrics, while maintaining comprehensive pricing advantages.

As the demand of portable electronic and wireless communication products increases, chip designers aggressively attempt to add more functions in a single chip because of the rapid advance in complementary metal-oxide semiconductor (CMOS) technology. Scaling of transistors over the years, a case of Moore's law has resulted in a decrease in channel length [2].The following figure illustrates the decrease of transistor´s channel length over the years.

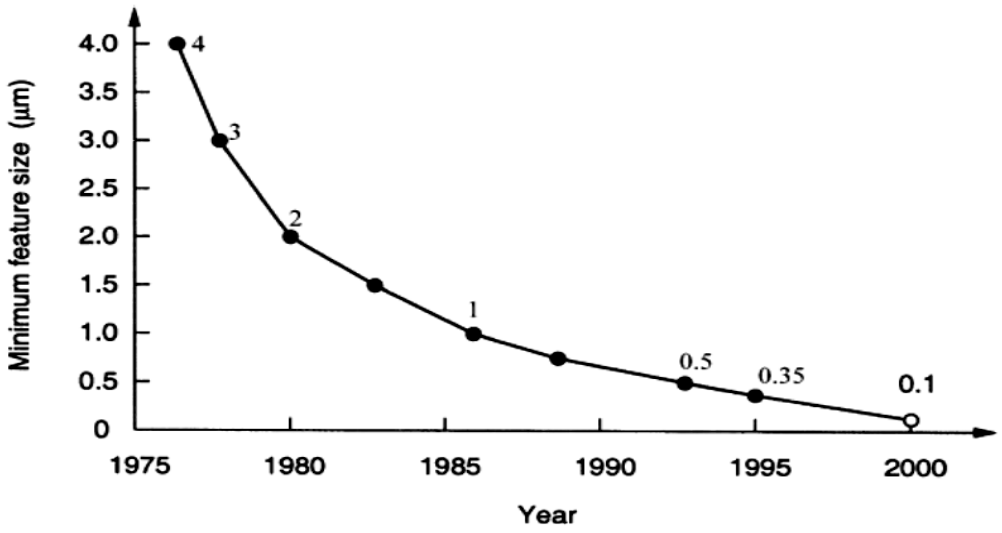


Figure 1.1: CMOS integration over the years

Channel length is taken as the reference geometrical parameter in a CMOS technology node. All geometrical dimensions in a circuit are considered to be scaled according to the channel length. Therefore, the decrease in channel length has led to integration of more and more transistors on a single chip and has also led to the decrease in the area of chip, which also has reduced the cost [3].

A system-on-a-chip (SoC) is designed to achieve a single chip composed of digital analog, and radio frequency (RF) subsystems. However, the main challenge of the SoC design is the mutual coupling between the subsystems, because such coupling degrades the performance of the SoC. Moreover, the complicated SoC design and chip testing prolong the design cycle, which impact the cost, time-to-market, and the benefit of using CMOS technology. CMOS would be the technology of choice to implement radio frequency (RF) designs for several unique characteristics like CMOS devices have large noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic circuits, for example transistor-transistor logic(TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to being implemented in VLSI chips [4].

In the era of modern communication system, voltage controlled oscillator (VCO) is multi-purposed radio frequency block. This is a special type of oscillating circuit with the property of varying output signal over a dynamic range which is controlled by input dc voltage and output frequency is directly in linear relation to the input voltage [5]. It is applied in numerous applications in case of radio frequency such as electronic jamming equipment, function generator, phase controlled loop, frequency synthesizers, frequency modulator(FM),pulse modulators(PM),frequency shift keying, phase looked loop(PLL) [6][7].

In the encompassing range in various applications of voltage-controlled oscillator (VCOs) circuits fundamentally planner spiral inductors are usually employed mainly because of their outstanding phase noise performance[8]-[12]. The usage of the spiral inductors exhibits several drawbacks: large chip area, complexity to achieve high inductive values in association with low values in quality factor and its geometry is not that much efficient leading to discourage to use at high density integration [8]. In order to overcome the drawbacks, active inductors can be used in an efficient way to achieve the objectives like low cost, low supply voltage, suitable operational frequency which are the important parameters for designing VCO circuits. An implementation of the active inductor is a methodology called the Gyrator-C configuration [13]-[14]. Recombining circuit elements such as resistor, capacitor, transistor in a benefitting manner which will act as an equivalence of impedance. This Gyrator-C configuration exhibits much higher values of inductance and quality factor in

quantitative comparison to traditional spiral inductors [15]-[16].Gyrator-C network configured in different ways and have variations in parameters such as frequency range, power consumption, inductance tunable range, requirement of silicon area for physical implementation [17][18].

Selecting good performing active inductor topology for designing active inductor based voltage controlled oscillator(VCO) for Bluetooth application was the primary concern. Implementing active inductor with high quality factor in designing VCO will show better performance in oscillation and the figure of merit will be higher. Considering this fact, initiatives were taken for further research on selecting active inductor model.

1.2 Objective

Although spiral inductors are the common implementation approach in ICs, it is possible to design active circuits, using the gyrator concept, that show an inductor impedance from some input terminal. These active-inductor circuits would save area and add easy tunability of the inductive value. Note the trend in RF communication systems today is towards more tunability and reconfigurability. Therefore, tunability of inductances is a desirable feature, which is not possible in conventional passive inductors. Several circuit topologies have been proposed in the past to implement active inductors based on gyrators. This worth has as an objective to compare their figures of merit in a given technology and determine the most promising in terms of losses (Q factor) and frequency response. Once this is achieved, it is proposed to demonstrate their suitability to be used in Voltage controlled Oscillator, comparing the circuit performance with other research works when conventional spirals are replaced by active inductors.

1.3 ISM Band

The **industrial, scientific and medical** (ISM) radio bands are radio bands (portions of the radio spectrum) reserved internationally for the use of radio frequency (RF) energy for industrial, scientific and medical purposes other than telecommunications. Examples of applications in these bands include radio-frequency process heating, microwave ovens, and medical diathermy machines. The powerful emissions of these devices can create electromagnetic interference and disrupt radio communication using the

same frequency, so these devices were limited to certain bands of frequencies. In general, communications equipment operating in these bands must tolerate any interference generated by ISM applications, and users have no regulatory protection from ISM device operation.

Despite the intent of the original allocations, and because there are multiple allocations, in recent years the fastest-growing uses of these bands have been for short-range, low power wireless communications systems. Cordless phones, Bluetooth devices, near field communication (NFC) devices, and wireless computer networks (Wi-Fi) all use the ISM frequencies, although these low power emitters are not considered ISM.

1.3.1 Definition

The ISM bands are defined by the ITU Radio Regulations (article 5) in footnotes 5.138, 5.150, and 5.280 of the Radio Regulations. Individual countries use of the bands designated in these sections may differ due to variations in national radio regulations. Because communication devices using the ISM bands must tolerate any interference from ISM equipment, unlicensed operations are typically permitted to use these bands, since unlicensed operation typically needs to be tolerant of interference from other devices anyway. The ISM bands share allocations with unlicensed and licensed operations; however, due to the high likelihood of harmful interference, licensed use of the bands is typically low. In the United States, uses of the ISM bands are governed by Part 18 of the Federal Communications Commission (FCC) rules, while Part 15 contains the rules for unlicensed communication devices, even those that share ISM frequencies. In Europe, the ETSI is responsible for regulating the use of Short Range Devices, some of which operate in ISM bands.

1.3.2 History

The ISM bands were first established at the International Telecommunications Conference of the ITU in Atlantic City, 1947. The American delegation specifically proposed several bands, including the now commonplace 2.4 GHz band, to accommodate the then nascent process of microwave heating; however, FCC annual reports of that time suggest that much preparation was done ahead of these presentations.

From the proceedings: "The delegate of the United States, referring to his request that the frequency 2450 Mc/s be allocated for I.S.M., indicated that there was in existence in the United States, and working on this frequency a diathermy machine and an electronic cooker,

and that the latter might eventually be installed in transatlantic ships and airplanes. There was therefore some point in attempting to reach world agreement on this subject."

Radio frequencies in the ISM bands have been used for communication purposes, although such devices may experience interference from non-communication sources. In the United States, as early as 1958 Class D Citizens Band, a Part 95 service, was allocated to frequencies that are also allocated to ISM.

In the U.S., the FCC first made unlicensed spread spectrum available in the ISM bands in rules adopted on May 9, 1985.

Many other countries later developed similar regulations, enabling use of this technology. The FCC action was proposed by Michael Marcus of the FCC staff in 1980 and the subsequent regulatory action took five more years. It was part of a broader proposal to allow civil use of spread spectrum technology and was opposed at the time by mainstream equipment manufacturers and many radio system operators.

1.3.3 Applications

However, as detailed below, the increasing congestion of the radio spectrum, the increasing sophistication of microelectronics, and the attraction of unlicensed use, has in recent decades led to an explosion of uses of these bands for short range communication systems for wireless devices, which are now by far the largest uses of these bands. These are sometimes called "non ISM" uses since they do not fall under the originally envisioned "industrial", "scientific", and "medical" application areas. One of the largest applications has been wireless networking (Wi-Fi). The IEEE 802.11 wireless networking protocols, the standards on which almost all wireless systems are based, use the ISM bands. Virtually all laptops, tablet computers, computer printers and cell phones now have 802.11 wireless modems using the 2.4 and 5.7 GHz ISM bands. Bluetooth is another networking technology using the 2.4 GHz band. Near field communication devices such as proximity cards and contactless smart cards use the lower frequency 13 and 27 MHz ISM bands. Other short range devices using the ISM bands are: wireless microphones, baby monitors, garage door openers, wireless doorbells, keyless entry systems for vehicles, radio control channels for UAVs (drones), wireless surveillance systems, RFID systems for merchandise, and wild animal tracking systems.

Some electrode less lamp designs are ISM devices, which use RF emissions to excite fluorescent tubes. Sulfur lamps are commercially available plasma lamps, which use a 2.45 GHz magnetron to heat sulfur into a brightly glowing plasma.

Long-distance wireless power systems have been proposed and experimented with which would use high-power transmitters and rectennas, in lieu of overhead transmission lines and underground cables, to send power to remote locations. NASA has studied using microwave power transmission on 2.45 GHz to send energy collected by solar power satellites back to the ground.

Also in space applications, a Helicon Double Layer ion thruster is a prototype spacecraft propulsion engine which uses a 13.56 MHz transmission to break down and heat gas into plasma.

1.4 Research Overview

The distinctive purpose of this work was to design a VCO specifically for the Bluetooth applications. The performance of the VCO is highly dependent on the inductor being used. Previously VCOs were implemented using spiral inductors yielding a low level of phase noise which is suitable for specific RF applications. Because of several draw backs of spiral inductors, active inductor can be used. Active inductor yields satisfactory performance of VCOs eradicating the drawbacks of spiral inductors. Active inductors exhibits characteristics as requirement of less silicon area, higher frequency range and frequency tunability. Emphasize was given on using active inductors for designing the VCO. Selection of high performance active inductor was the first concern for practical implementation from different active inductor models introduced like [48][31][29][17]. The second objective was to use the selected active inductor in designing VCO. Better oscillation, higher frequency, higher FOM were the performance criteria that were taken into the consideration. Comparative analysis and simulations of different active inductor models were performed. Results showed that Weng-Kuo active inductor gave the satisfactory performance such as high quality factor, inductance and frequency tunability. A VCO was designed using the Weng-Kuo active inductor. In 90 nm CMOS process, the simulations were done and compared to with other LC VCOs[56] [57][58]. Comparative analysis was performed considering several criteria like power consumption, phase noise, quality factor and figure of merit. .

1.5 Software Used

In this undergraduate thesis work, all the simulations are carried out in Cadence 6.16 version for effective analysis of different active inductors and VCO (voltage controlled oscillator)

1.6 Thesis Layout

This thesis is organized in eight chapters.

Chapter one provides with the motivation behind undertaking this thesis. That is why it was convincing for us to perform comparative analysis among different active inductor models and afterwards, to implement the proposed model for designing the VCO(voltage controlled oscillator).

Chapter two describes ins and outs of different spiral and active inductors and their advantages and disadvantages were depicted chronologically.

Chapter three deals with basic gyrator-C topology and different configuration of active inductor and their performance parameters.

Chapter four represents the basics of Voltage controlled Oscillators and brief analysis of different type of oscillators. In addition, design parameters of VCO were also demonstrated in an effective way.

Chapter five deals with LC VCOS based on spiral and active inductors.

Chapter six demonstrates Weng-Kuo active inductor based VCO design with specific design criteria.

Chapter seven illustrates simulations of different active inductors and our designed VCO for analyzing the performance parameters via cadence 6.16 version using 90nm CMOS process.

Chapter eight depicts the outcomes of our entire research with appropriate applications with insightful future scope

CHAPTER 02

SPIRAL AND ACTIVE INDUCTOR

2.1 Spiral Inductors

Monolithic on-chip inductors are also known as spiral inductors due to the way in which these inductors are laid out. Both planar and stacked spiral inductors have been developed and the detailed characterization and modeling of these inductors are available. Modern CAD tools for IC design are equipped with spiral inductors as standard elements in their component libraries.

2.1.1 Planar spiral inductors

Figure 2.1 is a sketch of square-shaped planar spiral inductors. The lumped equivalent circuit of spiral inductors is given in Figure 2.2, where L is the inductance of the spiral inductor, R_s represents the series resistance of the spiral caused by the skin-effect induced resistance in the spiral and the resistance induced by the eddy current in the substrate [19], C_s accounts for the capacitance due to the overlap of the spiral and the center-tap underpasses, C_{ox} denotes

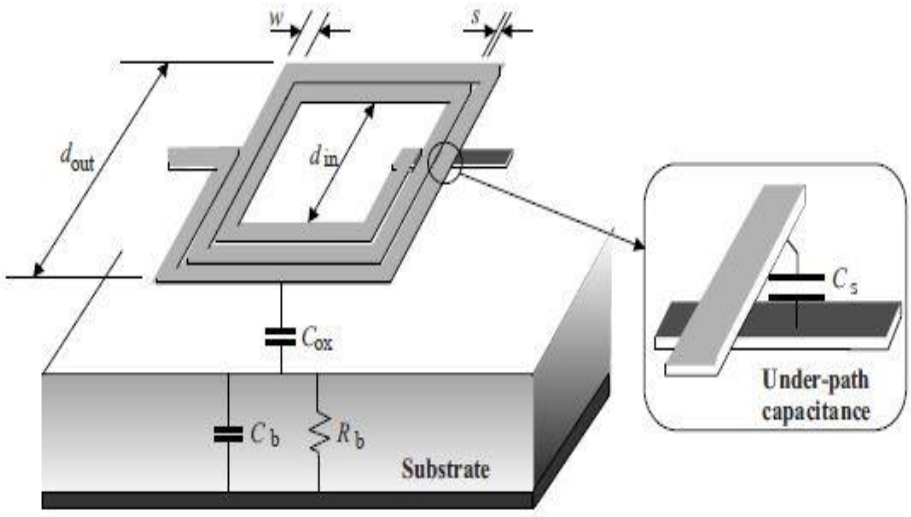


Figure 2.1: Square Shaped planar spiral inductors. W is the width of the spiral and s is the spacing between the turns of the spiral.

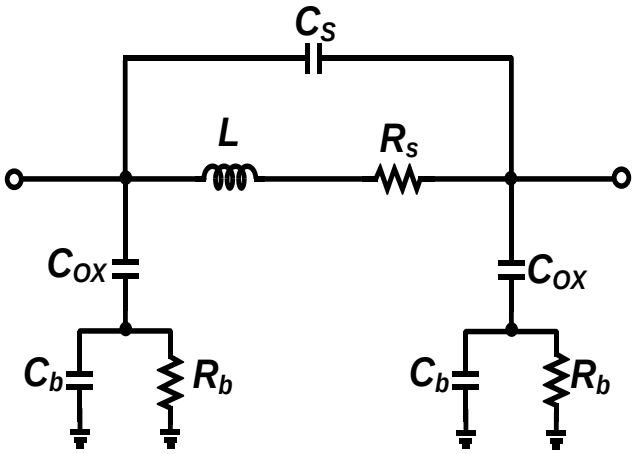


Figure 2.2: Lumped circuit model of planar spiral inductors.

the capacitance between the spiral and the substrate, C_b and R_b quantify the capacitance and resistance of the substrate, respectively. Although modern CMOS technologies are equipped with multiple metal layers, typically only the top metal layer is used to construct planar spiral inductors and transform-ers such that the unwanted parasitic capacitance between the spiral and the substrate is minimized. As pointed out in [32], the substrate loss accounts for 10-30% reduction of the quality factor of the spiral inductors in low GHz ranges, mainly due to the penetration of the electric field generated by the spiral into the substrate. A main drawback of planar spiral inductors is their low inductance.

2.1.2 Stacked spiral inductors

The inductance of spiral inductors can be increased significantly using stacked configurations, as shown in Figure 2.3, however, at the price of an in-creased spiral-substrate capacitance because the lower metal layers are also used in the construction of the inductors [20]. The total inductance of a stacked inductor with two spiral layers is given by

$$L_{total} = L_1 + L_2 + 2M \quad \text{.....(2.1)}$$

where L_1 and L_2 are the self-inductances of spirals 1 and 2, respectively, and M is the mutual inductance between the two spirals. Note the direction of the routing of the spirals in differential metal layers must be carefully

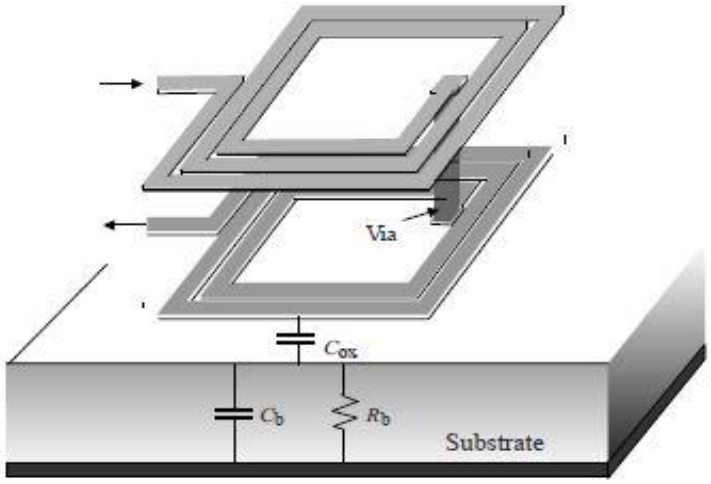


Figure 2.3: Square-shaped stacked spiral inductors.

chosen such that the total inductance increases. Figures 2.4 and 2.5 show the dependence of the measured inductance and self-resonant frequency of stacked inductors on the number of spiral layers [20]. It is seen that the inductance of stacked spiral inductors increases approximately linearly with the increase in the number of the spiral layers of the inductors. The self-resonant frequency of stacked inductors decreases with the increase in the number of spiral layers in a nonlinear fashion.

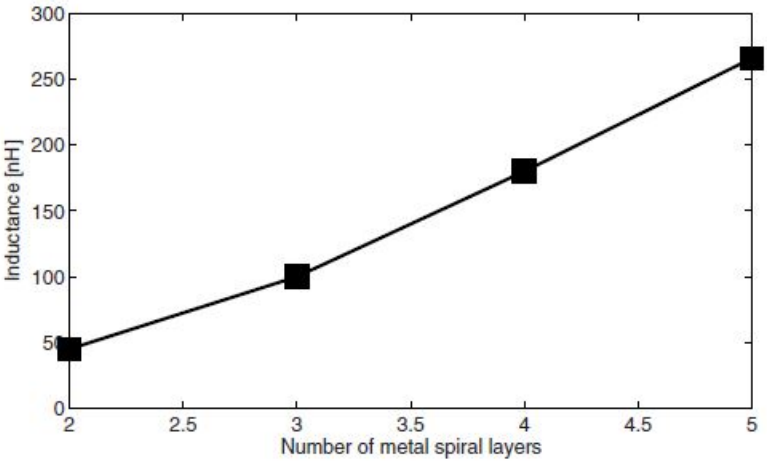


Figure 2.4: Dependence of the inductance of stacked inductors on the number of spiral layers.

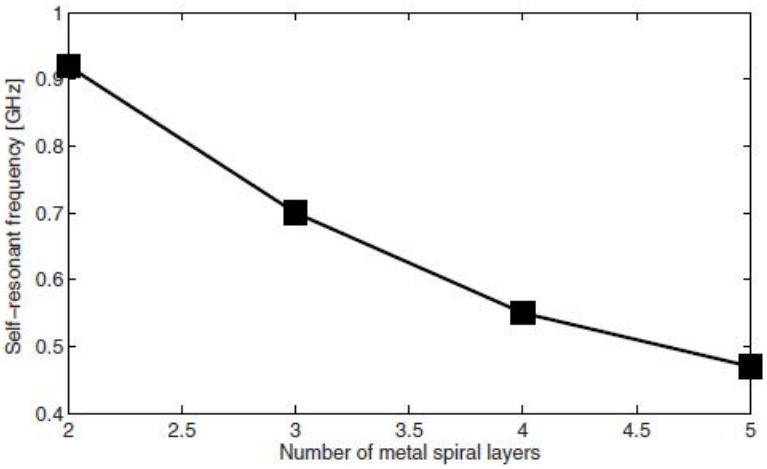


Figure 2.5: Dependence of the self-resonant frequency of stacked inductors on the number of spiral layers.

2.1.3 Layout of spiral inductors

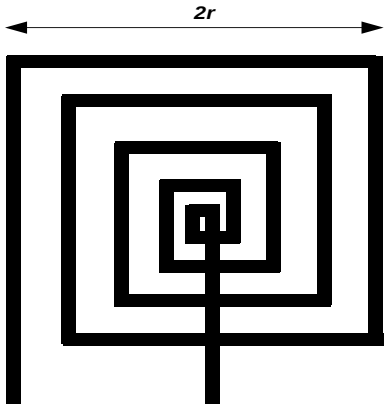


Figure 2.6: Typical layout of a spiral inductor.

A typical layout and model for a spiral inductor can be shown as given in Figure 2.6. Parameters of layout of spiral inductor

- L:total length of the wire
- W: width of the wire
- ω: angular frequency
- t: thickness of the wire

- σ: conductivity of the metal
- δ: skin depth
- n: number of loops

Relating parameters of the layout to the model except the inductance

$$R_s \approx \frac{L}{W.\sigma.\delta.(1-e^{-t/\delta})},\ \delta = \sqrt{\frac{2}{\omega.\mu_o.\sigma}} \quad \text{.....(2.2)}$$

$$C_p \approx n.W^2.\frac{\varepsilon_{ox}}{t_{ox}} \quad \text{.....(2.3)}$$

$$C_{ox} = W.L.\frac{\varepsilon_{ox}}{t_{ox}} \quad \text{.....(2.4)}$$

Now, assuming a ground (GND) connection, a parallel equivalent model can be achieved as shown in Figure 2.7

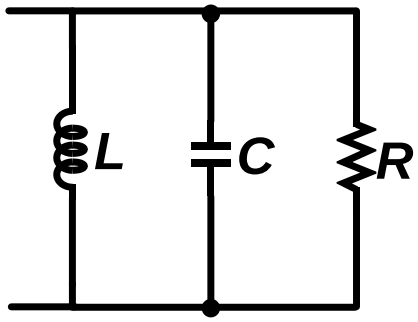


Figure 2.7: Parallel equivalent model of spiral inductor

$$Y = \frac{1}{R_P} + j\omega c + \frac{1}{j\omega L} = \frac{1}{R_P} + j(\omega c - \frac{1}{\omega L}) \quad \text{.....(2.5)}$$

2.1.4 Figures of merit of the inductors

The figures of merit of characterization of inductors are the Q factor, inductance value and the self-resonant frequency. They can be derived from the measurement of the admittance seen from the two port

By definition,

$$Q = -\frac{Im\{Y11\}}{Re\{Y11\}} = -R_p(\omega C - \frac{1}{\omega L}) \approx \frac{R_P}{\omega L} \quad \text{.....(2.6)}$$

$$L \approx -\frac{1}{\omega}\frac{1}{Im\{Y11\}} \quad \text{.....(2.7)}$$

$$f_{SR} = Im\{Y11\} = 0 \quad \text{.....(2.8)}$$

Figure 2.8 shows a graphical representation of the three figures of merit of the spiral inductor:

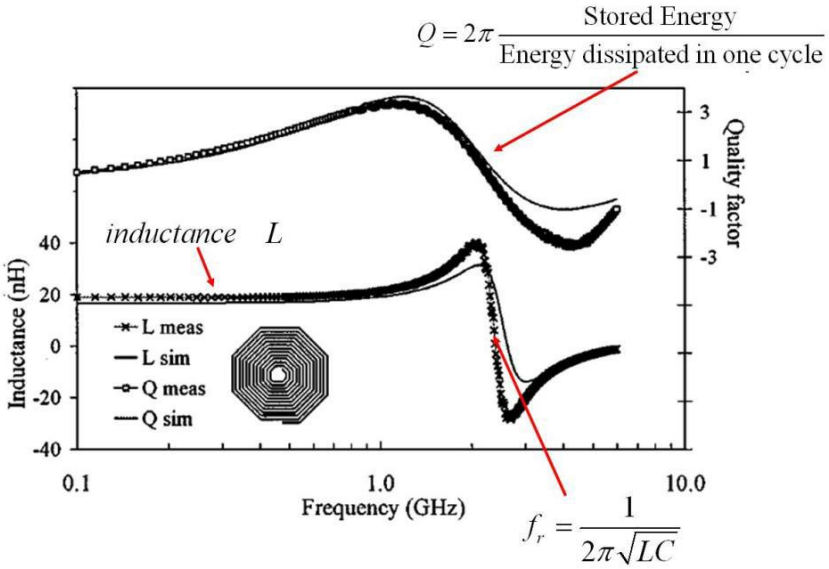


Figure 2.8: Three figures of merit of spiral inductor

2.2 Characteristics of Spiral Inductors

Spiral inductors offer the key advantages of superior linearity and a low level of noise. The performance and applications of spiral inductors are affected by a number of drawbacks that are intrinsic to the physical geometry of these passive devices and CMOS technologies in which spiral inductors are implemented. These drawbacks include

- **Low quality factor:** The quality factor of spiral inductors is limited by the ohmic loss of the spiral at high frequencies. Two sources that contribute to the ohmic loss of the spiral inductors exist: the skin-effect induced resistance of the spiral and the resistance induced by the eddy currents in the substrate. The former is proportional to the square-root of the frequency of the signal flowing in the spiral whereas the latter is proportional to the square of the frequency of the signal flowing in the spiral. Because

the resistance of the substrate in the lateral direction is much larger as compared with that in the vertical direction [21], the eddy currents in the literal direction in the substrate are small. The substrate eddy-current induced resistance of the spiral is often negligible as compared with the resistance caused by the skin-effect [22]. The quality factor of spiral inductors in standard CMOS is typically below 20, as is evident in Table 2.1 where the parameters of some recently reported CMOS spiral inductors are tabulated.

- **Low self-resonant frequency:** The self-resonant of a spiral inductor is the resonant of the LC tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low self-resonant frequency of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral. The typical self-resonant frequency of spiral inductors is in the low GHz range, as is evident in Table 2.1.

- **Low and fixed inductance:** As pointed out earlier that the inductance of aplanar spiral inductor is low and fixed once the number of the turns of the spiral is set. The only way to increase the inductance of the spiral inductor is to either increase the number of the turns of the spiral or use a stacked configuration where spirals on multiple metal layers are connected using vias. The former is at the expense of a large silicon area while the latter increases the spiral-substrate capacitance.

- **Large silicon area:** Due to the low inductance of spiral inductors, especially planar spiral inductors, and the fact that the inductance of these inductors is directly proportional to the number of the turns of the spiral of the inductors, the silicon area required for routing the spiral of the inductors is large. As an example, it was shown in [23] that a square-shaped spiral inductor of an inductance 8 nH will require 6 turns with d_{out} = 400μm. The actual silicon consumption of the inductor is larger than 400×400μm^2 when design rules on the minimum spacings are followed. Moreover, the design rules of most IC foundries prohibit the placement of either active or passive devices in the region between the spiral of the inductors and the substrate, making spiral inductors the most silicon-consuming components.

Table 2.1: Key parameters of some CMOS spiral inductors

Structure	Inductance (nH)	d_{out} (μm)	Turns	Q (ω_o)	f_o (GHz)	Year	Ref.
Square	3.5	330	4	11	3.9	1996	[21]
Square	<6	–	7	<6	1	1996	[22]
Square	15.2	310	8	<4	1.5	1998	[23]
Square	8	400	6	–	–	1999	[20]
Octagon	6	320	4	11	1.4	2003	[24]
Octagon	4.3	200	3	5	4	2003	[25]

2.3 Active Inductors

CMOS active inductors are active networks that consist mainly of MOS transistors. Resistors are sometimes used as feedback elements to improve the performance of active inductors. Under certain dc biasing conditions and signal-swing constraints, these networks exhibit an inductive characteristic in a specific frequency range. As compared with their spiral counterparts,CMOS active inductors offer attractive advantages.

2.3.1 Advantages of active inductors

- **Low silicon consumption:** Because only MOS transistors are usually required in the realization of CMOS active inductors and the inductance of these active inductors is inversely proportional to the transconductances of the transistors, the silicon consumption of CMOS active inductors is negligible as compared with that of their spiral counterparts.
- **Large and tunable self-resonant frequency:** CMOS active inductors with alarge self-resonant frequency are highly desirable. For example, the pass-band center frequency of an active inductor RF bandpass filter is typically set to the self-resonant frequency of the active inductor of the filter. The larger the self-resonant frequency of the active inductor, the higher the passband center frequency of the filter. In applications where CMOS active inductors are used for low-pass filters, these filters are operated at frequencies be-low their self-resonant frequency of active inductors. A large self-resonant frequency of active inductors ensures that the active inductors will

have an inductive characteristic over a large frequency range. The self-resonant frequency of a CMOS active inductor is the maximum frequency of the transconductors constituting the active inductor. When the basic configurations of transconductors, such as common-source and common-gate transconductors, are used, this frequency approaches f_T of the devices.

- **Large and tunable inductance:** The inductance of CMOS active inductors is inversely proportional to the transconductances of the transistors synthesizing the inductors. The smaller the width of the transistors, the larger the inductance. Also the inductance can be tuned conveniently by varying the dc biasing condition of the transistors synthesizing the inductor with a large inductance tuning range. The coarse tuning of the inductance of active inductors is typically attained in this way. The fine tuning of the inductance of active inductors can also be achieved by varying the load capacitance of the transconductors of the active inductors using MOS varactors.

- **Large and tunable quality factor:** The quality factor of CMOS activeinductors is set by the ohmic loss of the inductors, arising mainly from the finite output resistance of the transconductors of the inductors. The quality factor of CMOS active inductors can be increased by increasing this output resistance. A number of methods are available to boost the output resistance, such as cascodes, regulated cascodes, and negative resistor compensation. In each of these approaches, the degree of compensation can be varied. For example, in the cascode approach, the output resistance of a cascode-configured transconductor can be adjusted by varying the biasing voltage of the cascoding transistor. In the regulated cascode approach, the output resistance of the regulated-cascode configured transconductor can be changed by varying the voltage gain of its auxiliary voltage amplifier. In the negative resistor compensation approach, the resistance of the compensating negative resistor can be adjusted by varying the biasing current of the negative resistor.

- **Compatibility with digital CMOS technologies:** Spiral inductors are not available in low-cost digital-oriented CMOS processes. They are available only in more expensive mixed-mode CMOS technologies. CMOS active inductors, however, can be realized using standard digital CMOS processes.

CMOS active inductors have found increasing applications in areas where an inductive characteristic is required. These applications include LC and ring oscillators, RF bandpass filters, RF phase shifters, limiting amplifiers for optical communications, low-noise amplifiers for wireless communications, RF power dividers, ultra wideband low-noise amplifiers, and transceivers for high-speed data links over wire lines. Table 2.2 summarizes some of the recently published work where CMOS active inductors and trans-formers were employed.

Table 2.2: Applications and operating frequency of different CMOS active inductors

Reference	Year	Tech.	Applications	Remarks
Thanachayanont-Payne [29]	2000	0.8μm	IF Bandpass	100 MHz
Thanachayanont [30]	2000	0.8μm	LC VCO	0.45-1.2 GHz
Lin & Payne [31]	2000	0.35μm	LC VCO	1.1-2.1 GHz
Wu *et al.* [32]	2001	0.35μm	LC VCO	0.1-0.9 GHz
Thanachayanont [33]	2002	0.35μm	RF bandpass	2.4-2.6 GHz
Xiao &Schaumann [34]	2002	0.18μm	RF lowpass	4.57 GHz
Xiao *et al.* [35]	2004	0.18μm	RF bandpass	3.5-5.7 GHz
Lu *et al.* [36]	2005	0.18μm	RF power divider	4.5 GHz
Liang *et al.* [37]	2005	0.18μm	RF bandpass	3.45-3.6 GHz
Mahmoudi& Salama [38]	2005	0.18μm	QVCO	8 GHz
Lu *et al.* [39]	2006	0.18μm	LC VCO	0.5-3.0 GHz
Xiao &Schaumann [40]	2007	0.18μm	RF bandpass	3.34-5.72 GHz
Weng &Kuo [41]	2007	0.18μm	RF bandpass	2-2.9 GHz
Tang *et al.* [42]	2007	0.18μm	VCOs	1.6 GHz

- For bandpass filters, the frequency range is the passband center frequency range.
- For VCOs, the frequency range is the oscillation frequency range.
- For limiting amplifiers, the frequency is the bandwidth of the amplifiers

The applications of active inductors, however, are affected by several difficulties arising from the intrinsic characteristics of MOS devices. These difficulties include a limited dynamic range, a high level of noise, and a high sensitivity to process spread, supply voltage fluctuation, and ground bouncing. It should be noted that these limitations are not unique to CMOS active inductors but rather common to all synthesized devices. Also, the effect of many of these difficulties can be reduced through innovative designs. For example, the limited dynamic range of active inductors can be expanded using class AB configurations where the voltage swing of active inductors can be made nearly rail-to-rail [43]. The effect of the high sensitivity to process spread can be minimized by making use of the tunability of both the inductance and quality factor of active inductors. The effect of supply voltage fluctuation and ground bouncing can be greatly reduced by using replica-biasing techniques and proper circuit configurations [44].The effect of the high level of the noise of active inductors on the phase noise of LC oscillators with active inductors can be minimized by boosting the quality factor of the active inductors [45].

New design techniques are yet critically needed to further improve the performance of active inductors and transformers. The emerging applications of CMOS active inductors continue to be unfolded along with the inception of new design techniques and circuit topologies of these active devices.

CHAPTER 03

CMOS ACTIVE INDUCTOR TOPOLOGIES

3.1 Lossless Single- Ended Gyrator-C Active Inductors

A gyrator-C network is nothing but back-back transconductors having one port associated with a capacitor. When the input and output impedances of the transconductors are infinite the network is said to be lossless. Single ended indicates that any one end of the network is connected to a ground. That's the reason the definitive name of the network is Lossless Single–Ended Gyrator-C Active inductor.

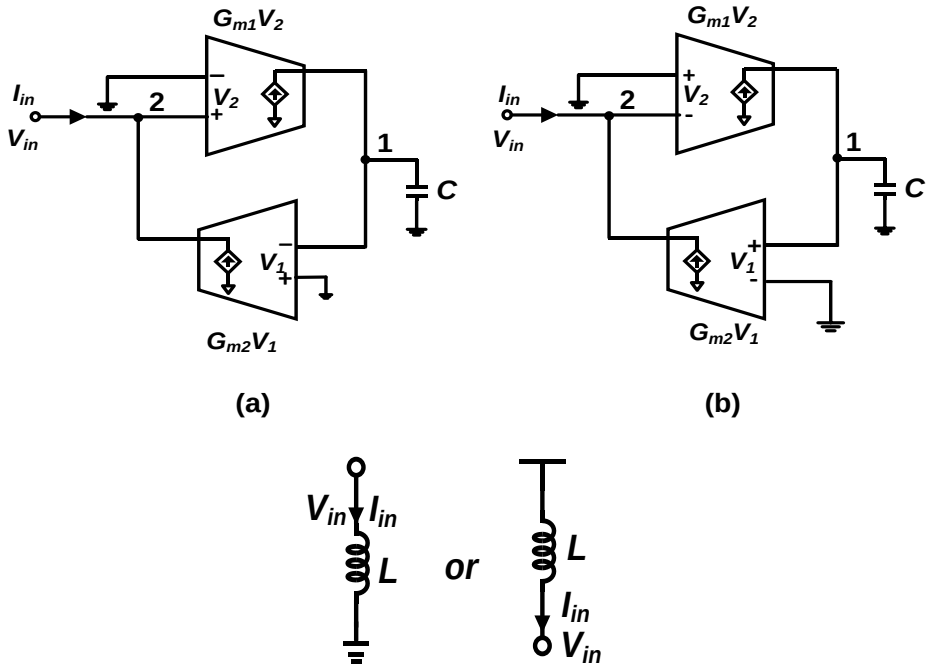


Figure 3.1: Lossless single-ended Gyrator-C active inductors.

a) Positive transconductance in forward path and negative in the feedback path

(b) Negative transconductance in forward path and positive in feedback path

Illustration of the equations:

At node (2) , applying KCL

$I_{in} + G_{m2}V_1 = 0$

$I_{in} = -G_{m2}V_1$……..……(3.1)

But V_1 = Current× Impedance

$$V_1 = -G_{m1}V_2 \times \frac{1}{sC}$$

Replacing in the equation (3.1),

$$I_{in} = -G_{m2}(-G_{m1} \times \frac{1}{sC})$$

or, $I_{in} = \frac{G_{m2}G_{m1}V_2}{sC}$

so, $I_{in} = \frac{V_2}{\frac{sC}{G_{m2}G_{m1}}}$

Now the admittance at port 2 of the gyrator-C network is given by

$$Y = \frac{I_{in}}{V_2}$$

$$Y = \frac{1}{s(\frac{C}{G_{m1}G_{m2}})} \text{ .....(3.2)}$$

From the denominator of the equation (3.2)

$$\frac{C}{G_{m2}G_{m1}} = \frac{\frac{Q}{V}}{\frac{I}{V}\frac{I}{V}} = \frac{QV}{I^2} = \frac{Q}{I}\frac{V}{I} = \frac{V}{\frac{I}{\frac{Q}{I}}} = \frac{V}{\frac{I}{t}} = L \quad \text{[as } Q=It\text{]}$$

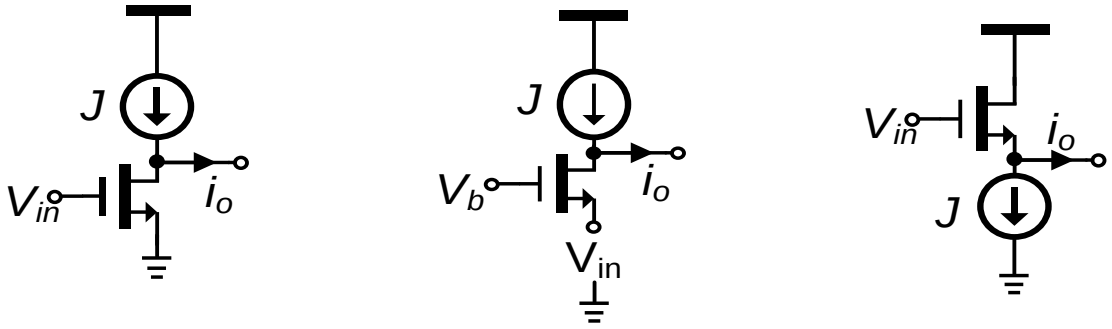
Thus a single ended lossless inductor is emulated at the port 2 of gyrator-C network which has an inductance of $L = \frac{C}{G_{m1}G_{m2}}$

And this synthesized inductor is known as gyrator-C active inductor of which inductance is proportional to the load capacitance and inversely proportional to the product of the transconductance of the tranconductors. The impedance due to inductance is $X_L = sL$ $[s=2\pi f]$

Both figure(3.1(a)) and figure(3.1(b)) will work as a single ended inductor. But basic difference is there between the two configurations. Figure(3.1(a)) has a positive transconductance in the forward path and a negative transconductance in the feedback path. Figure(3.1(b)) has a negative transconductance in the forward path and a positive transconductance in the feedback path. Although the transconductors of gyrator-C networks can be configured in various ways, the constraint that the synthesized inductors should have

- A large frequency range.
- A low level of power consumption.
- A small silicon area.
- A high quality factor.

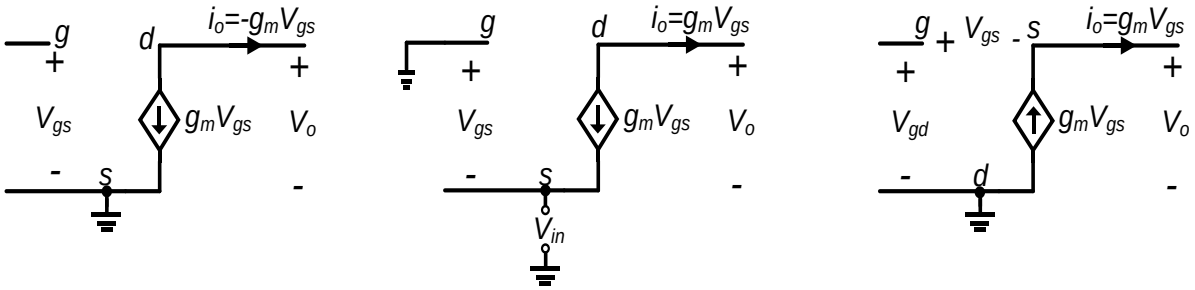
These transconductors be configured as simple as possible. Figure 3.2 shows the simplified schematics of the basic transconductors that are widely used in the configuration of gyrator-C active inductors. In a shortsighted manner, with the increment of the input applied voltage , the output current (i_o) of a transconductor enhances, at that point it might be said that the transconductor has a positive transconductance. On the contrary, the decrement of the output current(i_o) of a transconductor, then it can be illustrated as a transconductor having a negative transconductance.



(a) (b) (c)

Figure 3.2: Schematic diagram of basic transconductors.

a. Common Source b. Common Gate c. Common Drain



(a) (b) (c)

Figure 3.3: Small signal model of basic transconductors.

a. Common Source b. Common Gate c. Common Drain

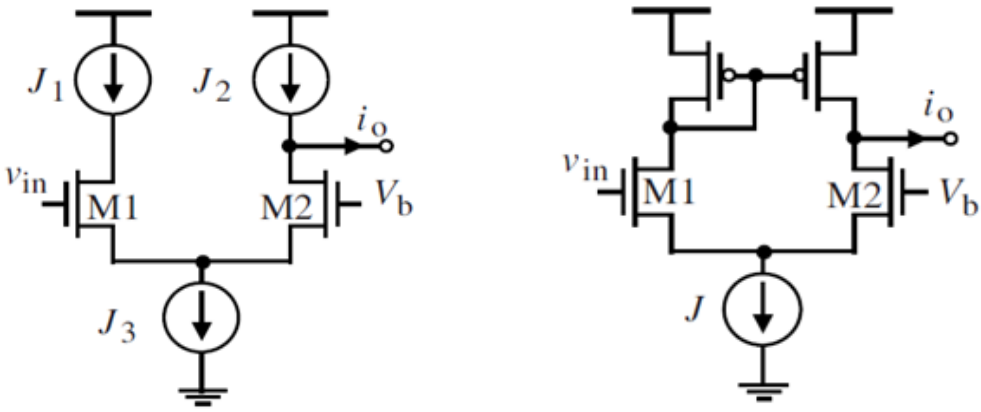


Figure 3.4: Differential pair transconductors.

Common-gate, common-drain, and differential-pair transconductors all have a positive transconductance while the common-source transconductor has a negative transconductance. To demonstrate this, consider the common-gate transconductor. An increase in v_{in} will lead to a decrease in i_D. Because $i_o = J - i_D$, i_o will increase accordingly. So the transconductance of the common-gate transconductor is positive. Similarly, for the differential-pair

transconductor in figure 3.4 An increase in v_{in} will result in an increase in i_{D1}. Since $i_{D2} = J_3 - i_{D1}$, i_{D2} will decrease. Further $i_o = J_2 - i_{D2}$, i_o will increase. The differential-pair transconductor thus has a positive transconductance.

3.2 Lossless Floating Gyrator-C Active Inductors

An inductor is said to be floating if both the terminals of the inductor are not associated with either the ground or power supply of the circuits containing the active inductor. Floating gyrator-C active inductors can be constructed in a similar way as single-ended gyrator-C active inductors by replacing single ended transconductors with differentially-configured transconductors, as shown in the figure

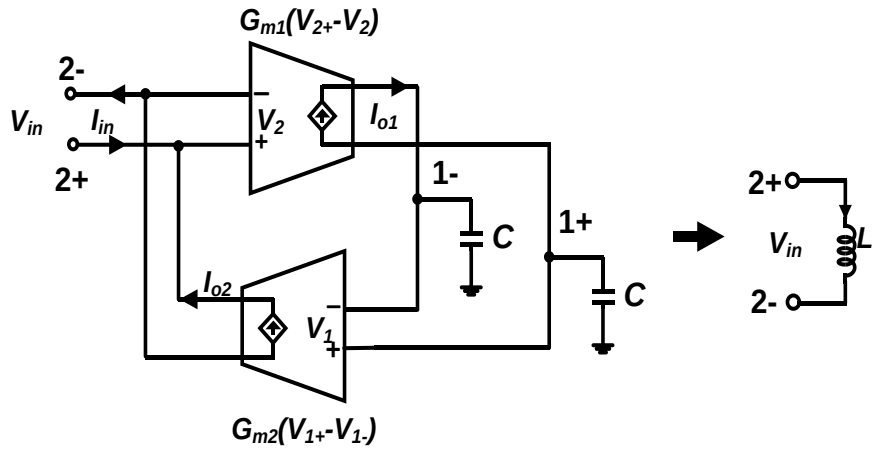


Figure 3.5: Lossless floating gyrator-C active inductors

$$V_{in1}^{+} = -\frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-})$$

$$V_{in1}^{-} = \frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \quad \text{.....(3.3)}$$

$$I_{o2} = g_{m2}(V_{in1}^{+} - V_{in1}^{-})$$

We have

$$I_{o2} = \frac{2g_{m1}g_{m2}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \quad \text{.....(3.4)}$$

The admittance looking into port 2 of the gyrator-C network is given by

$$Y = \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}}$$

$$= \frac{1}{s(\frac{2C}{g_{m1}g_{m2}})} \quad \text{.....(3.5)}$$

Eq(3.5) reveals port 2 of the gyrator-C network behaves as a floating inductor with is inductance given by,

$$L = \frac{2C}{g_{m1}g_{m2}}$$

Floating gyrator-C active inductors offer the following attractive advantages over their single-ended counterparts:

- The differential design of the transconductors successfully rejects the common mode disturbances of the system, making them especially appealing for applications where both analog and digital circuits are manufactured on a similar substrate.
- The level of the voltage swing of floating inductors is twice that of the comparing single-ended active inductors.

3.3 Lossy Single-Ended Gyrator-C Active Inductors

Inductors are called lossy when the input and output inpedances of transconductors of gyrator-C configuration are finite. After implementing MOS, the input and output impedances of the network become finite. The lossy network is inductive upto a particular frequency which is called self-resonant frequency.

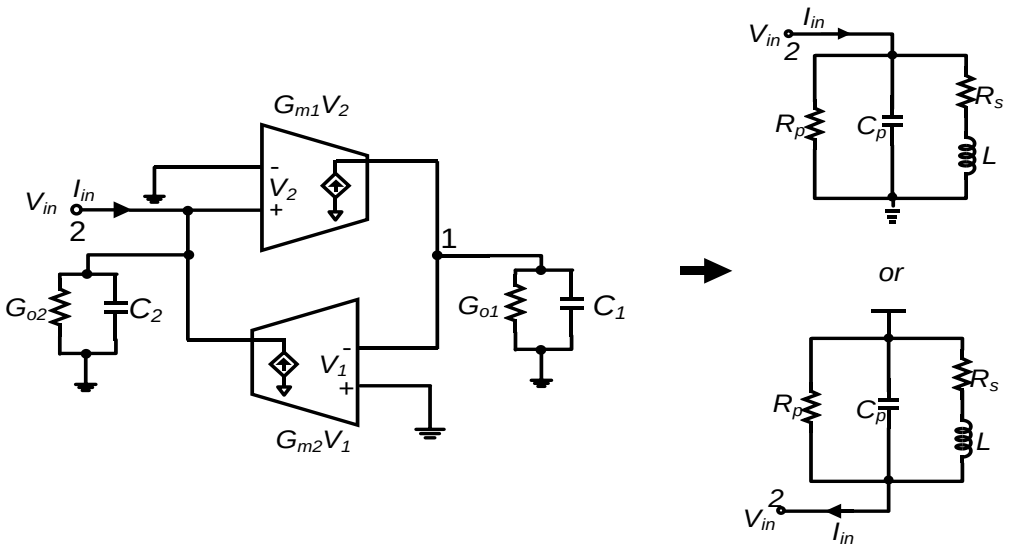


Figure 3.6: Lossy single-ended Gyrator-C active inductors. C_1 and G_{o1}, C_2 and G_{o2} denote the total capacitances and conductances at node 1 and 2, respectively.

Consider the gyrator-C network shown in figure 3.6 where G_{o1} and G_{o2} denote the total conductances at nodes 1 and 2, respectively. Note G_{o1} is due to the finite output impedance of transconductor 1 and the finite input impedance of transconductor 2. To simplify analysis, we continue to assume that the transconductances of the transconductors are constant. Write KCL at nodes 1 and 2

Applying KCL at node 1 and 2

$G_{m1}V_2 = (sC_1 + G_{o1})V_1$……..(3.6)

$I_{in} + G_{m2}V_1 = (sC_2 + G_{o2})V_2$……..…….…….(3.7)

Solving (3.6) and (3.7)

$Y = \frac{I_{in}}{V_2}$

$Y = sC_2 + G_{o1} + \frac{1}{s(\frac{C_1}{G_{m1}G_{m2}}) + \frac{G_{o1}}{G_{m1}G_{m2}}}$.....(3.8)

Equation (3.8) represents a RLC networks and its parameters are given by

Parallel resistance, $R_p = \frac{1}{G_{o2}}$

Parallel capacitance, $C_p = C_2$

Series resistance with inductor, $R_p = \frac{G_{o1}}{G_{m1}G_{m2}}$

Inductance, $L = \frac{C_1}{G_{m1}G_{m2}}$

Comments on the preceding results :

- When the input and output conductances of the transconductors are considered, the gyrator-C network behaves as a lossy inductor with its parasitic parallel resistance R_p, parallel capacitance C_p, and series resistance R_s. R_p should be maximized while R_s should be minimized to low the ohmic loss. The finite input and output impedances of the transconductors of the gyrator-C network, however, have no effect on the inductance of the active inductor.
- R_p and C_p are solely due to G_{o2} and C_2. G_{o1} and C_1 only affect R_s and L.
- The resonant frequency of the RLC networks of the active inductor is given by

  $\omega_o = \frac{1}{LC_p} = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} = \sqrt{\omega_{t1}\omega_{t2}}$……..…….(3.9)

  Where,$\omega_{t1,2} = \frac{G_{m1,2}}{C_{1,2}}$……..…..…(3.10)

  is the cut-off frequency of the transconductors. ω_o is the self-resonant frequency of the gyrator-C active inductor. This self-resonant frequency is typically the maximum

frequency at which the active inductor operates. The self-resonant frequency of an active inductor is set by the cut-off frequency of the transconductors constituting the active inductor.

The small-signal behavior of a gyrator-C active inductor is fully characterized by its RLC equivalent circuit. The RLC equivalent circuit of gyrator-C active inductors, however, cannot be used to quantify the large-signal behavior, such as the dependence of the inductance on the dc biasing condition of the transconductors and the maximum signal swing of the gyrator-C active inductors.

- The finite input and output impedances of the transconductors consisting active inductors result in a finite quality factor. For applications, for example, band pass filters active inductors with a substantial quality factor are compulsory. In these cases, Q - upgrade strategies that can offset the unfavorable impact of R_p and R_s ought to be utilized to support the quality factor of the active inductor.

3.4 Lossy Floating Gyrator-C Active Inductors

Lossy floating gyrator-C active inductors can be analyzed in a similar way as lossy single-ended gyrator-C active inductors. Consider the lossy floating gyrator-C network shown in Figure 3.7. We continue to assume that the transconductances of the transconductors are constant.

Writing KCL at nodes 1-, 1+, 2-, and 2+ yields

$$-G_{m1}(V_2^+ - V_2^-)+(\frac{sC_1+G_{o1}}{2})(V_1^- - V_1^+)=0\text{…….……}\quad(3.10)$$

$$I_{in} + (\frac{sC_2+G_{o1}}{2})\,(V_2^- - V_2^+) + G_{m2}(V_1^+ - V_1^-)=0\text{……..…..}\quad(3.11)$$

Solving (3.10) & (3.11)

$$Y=\frac{I_{in}}{V_2^+-V_2^-}$$

$$= s\frac{C_2}{2}+\frac{G_{o2}}{2}+\frac{1}{s\left(\frac{C_1}{2G_{m1}G_{m2}}\right)+\frac{G_{o1}}{2G_{m1}G_{m2}}}\text{…….....}\quad(3.12)$$

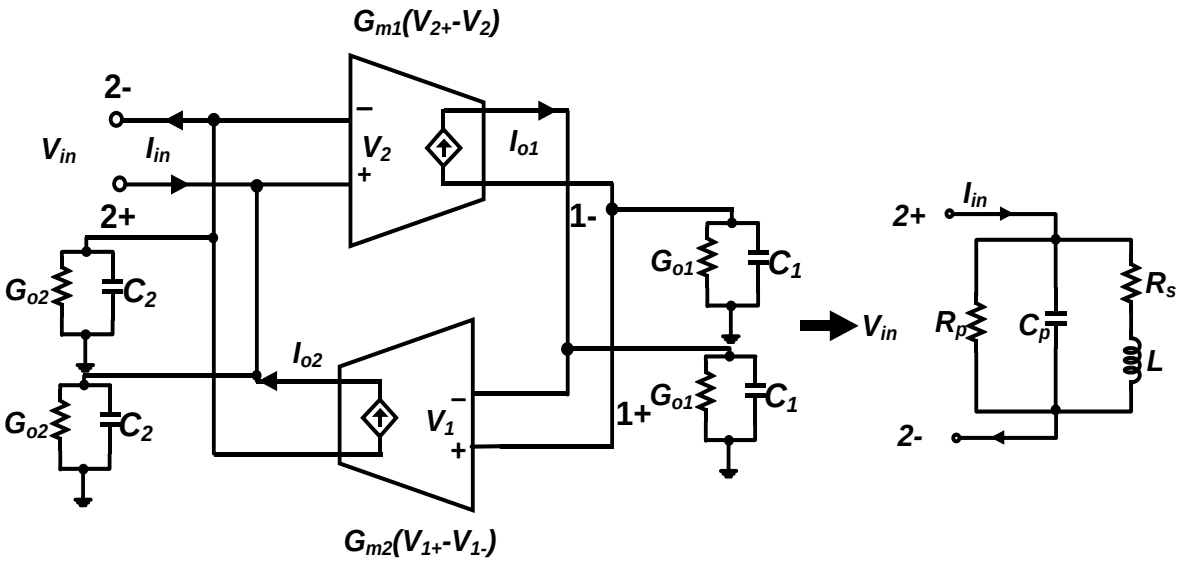


Figure 3.7:Lossy floating gyrator-C active inductors. C_1 and G_{o1}, C_2 and G_{o2} represent the total capacitances and conductances at nodes 1 and 2, respectively.

Eq(3.11) can be represented by the RLC network in figure 3.7 with is parameters given by

Parallel resistance, $R_p = \frac{2}{G_{o2}}$

Parallel capacitance, $C_p = \frac{C_2}{2}$

Series resistance, $R_s = \frac{\frac{G_{O1}}{2}}{G_{m1}G_{m2}}$

Inductance, $L = \frac{\frac{C_1}{2}}{G_{m1}G_{m2}}$

3.5 Performance Parameters of Active Inductors

3.5.1 Frequency range

It was appeared in the previous that a lossless gyrator C active inductor shows an inductive characteristics over the whole frequency range. A lossy gyrator-C active inductor, nonetheless, just displays an inductive characteristic over a particular frequency range. This

frequency range can be gotten by inspecting the impedance of the RLC identical circuit of the lossy active inductor.

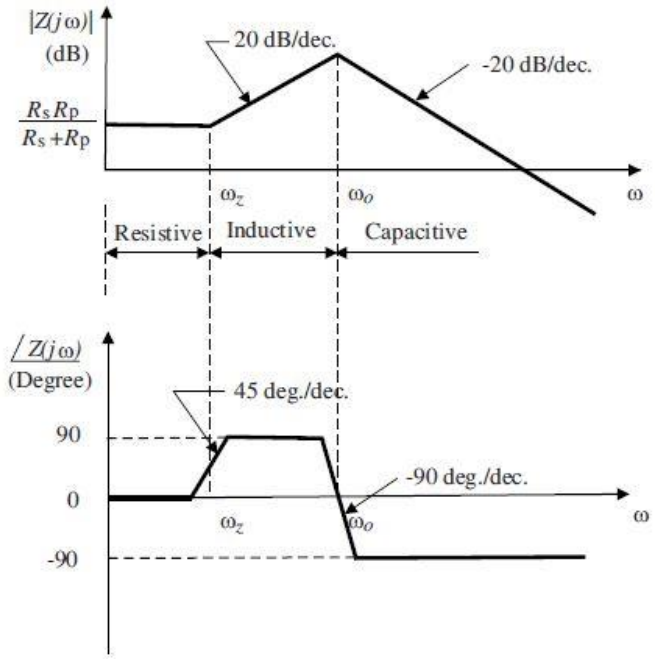


Figure 3.8: Bode plots of the impedance of lossy Gyrator-C active inductors

$$Z = \left(\frac{R_s}{C_p L}\right) \frac{s\frac{L}{R_s}+1}{s^2+s\left(\frac{1}{R_p C_p}+\frac{R_s}{L}\right)+\frac{R_p+R_s}{R_p C_p}} \quad \text{.....(3.13)}$$

When complex conjugate poles are encountered, te pole resonant frequency of *Z*is given by

$$\omega_p = \sqrt{\frac{R_p+R_s}{R_p C_p L}} \quad \text{.....(3.14)}$$

Because $R_p >> R_s$ Eq. 3.14 is simplified to

$$\omega_p \approx \sqrt{\frac{1}{LC_p}} = \omega_o \quad \text{.....(3.15)}$$

Where ω_o is the self resonant frequency of the active inductor. The zero frequency is given by

$$\omega_z = \frac{R_S}{L} = \frac{G_{O1}}{C_1} \quad \text{.....(3.16)}$$

The Bode plots of Z are outlined in figure 3.8. It is apparent that the gyrator C network is resistive when $\omega<\omega_z$, inductive when $\omega_z<\omega<\omega_o$, and capacitive when $\omega >\omega_o$. The frequency range in which the gyrator-C network is inductive is bring down limited by ω_z and upper-limited by ω_o. Likewise watched is that R_p has no impact on the frequency range of the active inductor. R_s, be that as it may, influences the lower bound of the frequency range over which the gyrator-C network is inductive. The upper bound of the frequency range is set by the self-resonant frequency of the active inductor, which is set by the cut-off frequency of the transconductors constituting the active inductor. For a given inductance L, to expand the frequency, both R_s and C_p ought to be limited.

3.5.2 Quality factor

The quality factor Q of an inductor measures the proportion of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle. For spiral inductors, the quality factor of these inductors is independent of the voltage/current of the inductors. This property, nonetheless, does not hold for active inductors as the inductance of these inductors relies on the transconductances of the transconductors constituting the active inductors and the load capacitance. At the point when active inductors are utilized as a part of uses, for example, LC oscillators, the inductance of the active inductors is a strong function of the swing of the voltage and current of the oscillators. To measure the of the ratio net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle and relate it to the performance of LC oscillators, specifically, the phase noise of the oscillators, an alternative meaning of the quality factor that records for the swing of the voltage/current of the active inductors is needed.

Instantaneous quality factor:

The quality factor Q of an inductor quantifies the ratio of the net magnetic energy stored in the inductor to its ohmic loss in one oscillation cycle

$$Q=\frac{\text{Net magnetic energy stored}*2\pi}{\text{Energy dissipated in one oscillation cycle}}$$

For a linear inductor, the complex power of the active inductor is obtained from

$$P(j\omega) = I(j\omega)V^*(j\omega)$$
$$= Re[Z][I(i\omega)]^2 + iIm[Z][I(i\omega)]^2 \text{…….....(3.17)}$$

Where *Re[Z]* and *Im[Z]* are the resistance and inductive reactance of the inductor, respectively, *V(jω)* and *I(jω)* are the voltage across and the current through the inductor, respectively, the superscript [*] is the complex conjugation operator. The first term in (3.10) quantifies the net energy loss arising from the parasitic resistances of the inductor, whereas the second term measures the magnetic energy stored in the inductor. Eq.(3.10) in this case becomes

$$Q = (Im[Z])/(Re[Z]) \text{ ……..(3.18)}$$

Eq.(3.11) gives a helpful approach to measure Q of linear inductors including active inductors.

Active inductors are linear when the swing of the voltages/currents of the inductors are little and all transistors of the active inductors are legitimately biased. The quality factor of a lossy Gyrator C active inductor can be gotten straightforwardly from (3.19) and (3.18)[25]

$$Q = \left(\frac{\omega L}{R_s}\right)\frac{R_p}{R_p+R_s[1+(1+(\frac{\omega L}{R_s})^2]}[1 - \frac{R_s^2 C_p}{L} - \omega^2 LC_p \text{…..(3.19)}$$

The first term is denoted by

$$Q_1 = \frac{\omega L}{R_s} \text{……..…….…....(3.20)}$$

Quantifies the quality factor of the active inductor at low frequencies. The second term, denoted by

$$Q_2 = \frac{R_p}{R_p+R_s[1+(1+(\frac{\omega L}{R_s})^2]} \text{……..……(3.21)}$$

Accounts for the effect of the finite output impedance of deep sub-micron MOSFETs, whereas the third term, denoted by

$$Q_3 = 1 - \frac{R_s^2 C_p}{L} - \omega^2 LC_p \text{…….……(3.22)}$$

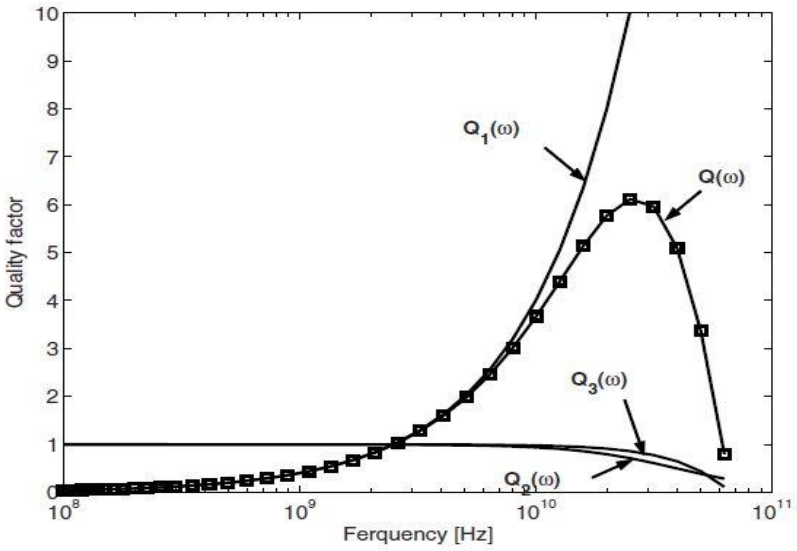


Figure 3.9: Frequency dependence of the quality factor of active inductors

demonstrates that the quality factor vanishes when frequency approaches the cut-off frequency of the transconductors of the active inductor. $Q_2$and Q_3 show themselves at high frequencies as it were.

The sensitivity of the quality factor of the active inductor regarding R_s and R_p is examined in Figure 3.9 individually. It is seen that Q_1 rules the nature of the active inductor and is subsequently generally used to measure the quality factor of active inductors.

To boost the quality factor of active inductors, R_s must be limited. Four methodologies can be utilized to diminish R_s

1. **Lowering G_{01}:** Because $R_s = \frac{G_{o1}}{G_{m1}G_{m2}}.R_s$ can be lowered by G_{01} directly. Since G_{o1}istypically the output impedance of the transconductor with a positive transconductance, the use of transconductors with a large output impedance is critical.

2. **Increasing G_{m1}&G_{m2}:** R_s can be lowered by expanding G_{m1} and G_{m2}specifically. Since the transconductances of the transconductors are specifically proportional to the dc biasing currents and the width of the transistors of the transconductors, Rs can be lowered by either increasing the dc biasing currents and flows or increasing the transistor width. The previous, be that as it may, increases the static power

consumption of the active inductors though the later lowers the self-resonant frequency of the active inductors. Another drawback of this approach is that the inductance of the inductors L will also be influenced.

3. **Cascodes:** Reduce G_{o1} using advanced circuit techniques, such as cascodes. Cascodes are effective in lowering the output conductance and can be used here to reduce G_{o1}.

4. **Shunt negative resistor:** Use a shunt negative resistor at the output of the positive transconductor to cancel out the parasitic resistances, both series and parallel, of active inductors.[47]

3.5.3 Power consumption

Spiral inductors do not consume static power. gyrator-C active inductors, however, consume dc power, mainly due to the dc biasing currents of their transconductors. The power consumption of gyrator-C active inductors themselves is usually not of a critical concern because the inductance of these inductors is inversely proportional to the transconductances of the transconductors constituting the inductors. To have a large inductance, G_{m1} and G_{m2} are made small. This is typically achieved by lowering the dc biasing currents of the transconductors. When replica-biasing is used to minimize the effect of supply voltage fluctuation on the inductance of active inductors, as to be seen shortly, the power consumed by the replica-biasing network must be accounted for. Also, when negative resistors are employed for boosting the quality factor of active inductors, their power consumption must also be included. Often the power consumption of an active inductor is set by that of its replica-biasing and negative resistor networks.

3.6 Implementation of Single-Ended Active Inductors

The requirement for a high self-resonant frequency of active inductors requires that the transconductors of these active inductors be designed as simple as possible. This also lowers their level of power consumption and reduces the silicon area required to fabricate the inductors. Most reported gyrator-C active inductors employ a common-source configuration as negative transconductors, common-gate, source follower, and differential pair

configurations as positive transconductors. These basic transconductors have the simplest configurations subsequently the highest cutoff frequencies and the lowest silicon consumption.

The load capacitor of the transconductors is realized using the intrinsic capacitance C_{gs} of the transistors of the transconductors directly to maximize the upper bound of the frequency range of the active inductors and to avoid the use of expensive floating capacitors, which are available only in mixed-mode CMOS processes. MOS varactors are often added in parallel with C_{gs} to tune the inductance of active inductors.

3.6.1 Basic Gyrator-C active inductors(Common Source & Common Drain)

Focusing on figure 3.1(b)

Forward path **Feedback path**

In forward path $i_o = -G_{m1} V_2$. (negative transconductance) and in feedback path $i_o = G_{m2}V_1$. (positive transconductance).

Thus the common source configuration exhibits the negative transconductance while the common drain configuration exhibits positive transconductance. Therefore a common source configuration in the forward path and a common drain configuration in the feedback path are applied to emulate the basic gyrator-C configuration.

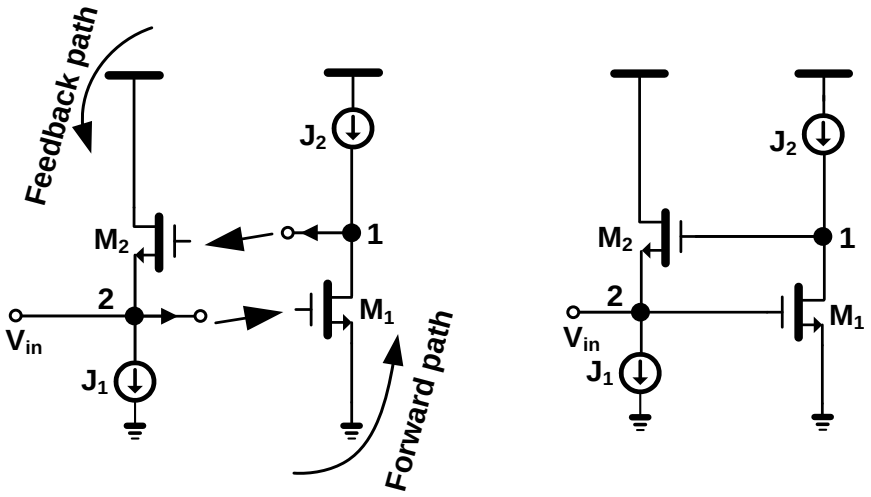
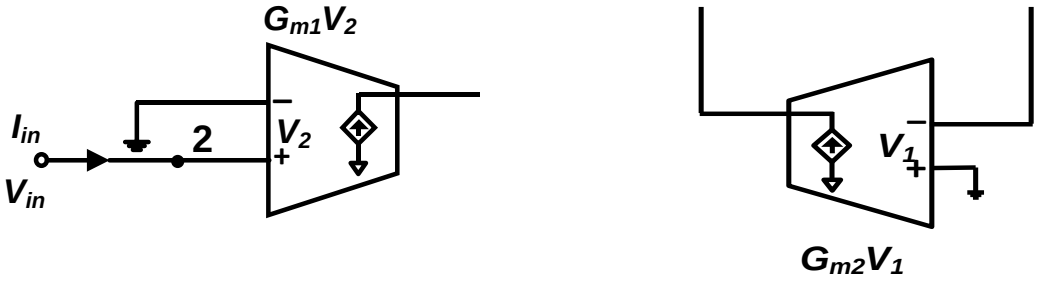


Figure 3.10: Simplified schematic of Basic Gyrator-C active inductor(Common source and Common drain)

3.6.2 Basic Gyrator-C active inductors(Common Source & Common Gate)

Similarly, focusing on figure 3.1(a)



Forward path **Feedback path**

In forward path $i_o = G_{m1}V_2$. (positive transconductance) and in feedback path $i_o = -G_{m2}V_1$. (negative transconductance).

Thus the common source configuration exhibits the negative transconductance while the common gate configuration exhibits positive transconductance. Therefore a common gate configuration in the forward path and a common source configuration in the feedback path are applied to emulate the basic gyrator-C configuration.

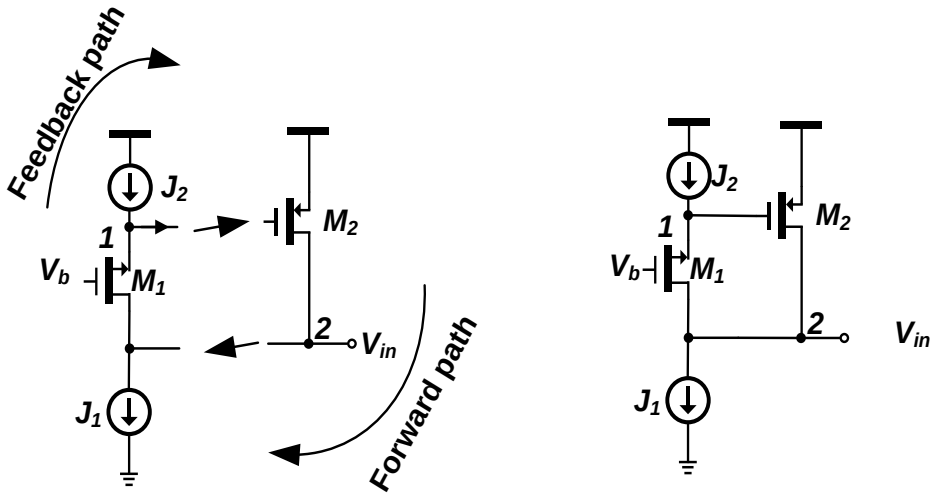


Figure 3.11: Simplified schematic of Basic Gyrator-C active inductor(Common source and Common Gate)

For figure 3.10 & 3.11, $C_1 = C_{gs2}$, $G_{o1} \approx g_{o1}$, $G_{m1} = g_{m1}$, $C_2 = C_{gs1}$, $G_{o2} \approx g_{m1}$, and $G_{m2} = g_{m2}$, where g_{oj} and g_{mj}, $j = 1, 2$, are the output conductance and transconductance of transistor j, respectively. The parameters of the equivalent RLC network of the active inductor is given by

Parallel resistance, $R_p = \frac{1}{G_{o2}}$

Parallel capacitance, $C_p = C_2$

Series resistance with inductor, $R_p = \frac{G_{o1}}{G_{m1}G_{m2}}$

Inductance, $L = \frac{C_1}{G_{m1}G_{m2}}$

3.7 Different Active Inductor Models

3.7.1 Yodprasit-Ngarmnil active inductor

This model is developed on double feedback transconductane topology. Here positive feedback is used to raise a resistance for negating the inductor loss and the negative feedback is to conceive inductive input impedance so that the Q

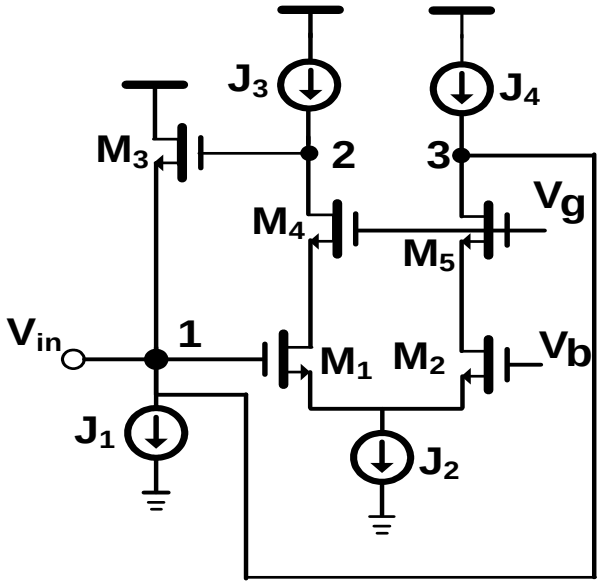


Figure 3.12:Yodprasit-Ngarmnil Active Inductor

factor can be enhanced. In the circuitry shown in Figure.3.12, for producing positive feedback, the active inductor input terminal and drain of M5 is connected electrically. As there is resistive loss in the Yodprasit-Ngarmnil active inductor, a negative resistor with resistance of $-R_{P,total}$ is connected in parallel with $R_{P,total}$. By this way, the net resistive loss of designed active inductor demolishes. To analyze the performance of this type of inductor, quality factor can be defined as

$$Q = \frac{\sqrt{g_{m_3} g_{m1} C_{gs_3} C_{gs_1}}}{\frac{C_{gs_1}}{r_{o_1}} + 2\frac{C_{gs_1}}{r_{o_3}}} \quad \text{.....(3.23)}$$

Q can be tuned by varying $g_{m_{1,2}}$ or $r_{o1,2.}$ As the preceding parameters change the inductance,$r_0$of $M_1$and M_2can be changed and this variation can be achieved by employing the cascade configuration.[48]

3.7.2 Lin-Payne active inductor

Lin-Payne active inductor methodology satisfies two major purposes. i) Under low parasitic, it has made possible high frequency circuit operation, and ii) Maximize the dynamic range

through sufficient voltage headroom. For this design requirement, a minimum level of supply voltage is expressed as

$V_{DD_{min}} = V_{GSp} + V_{DSat}$……..….... (3.24)

This minimum supply voltage for outer transistor M_2 is higher with a quantitative comparison to inner transistor branch M_1. For lower branch M_1,

$V_{DD_{min}} = V_{GSp} - V_{GSn} + V_{DSat}$……..……(3.25)

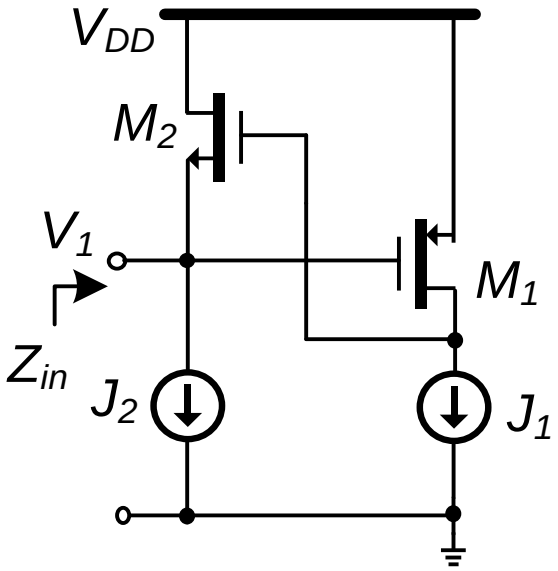


Figure 3.13: Lin-Payne active inductor

This equation connotes that for the current source I_1 a considerably large voltage headroom is left which is the key factor for varying tuning range.[31]

3.7.3 Thanachayanont-Payne active inductor

For the low phase noise and low power performance of the LC-VCO, the LC-tank should have high Q. It was indicated out before that amplifying the frequency range of active inductors, ω_z ought to be limited and ω_0 ought to be amplified. Expanding ω_0 is fairly troublesome in light of the fact that ω_0 of active inductors is set by the cut-off frequency of the transconductors constituting the active inductors. The frequency of the zero of active

inductors given by $\omega_z = \frac{g_{01}}{C_{gs2}}$, then again, can be brought down by either increasing C_{gs2}or diminishing g_{01}. The previous is at the cost of bringing down ω_0 and ought to in this way be kept away from. To diminishg_{01}, Thanachayanont and Payne proposed the cascode active inductors appeared in figure 3.13.

Cascode can be executed in both of the two transconductors, as appeared in figure. 3.13. The impedance of Thanachayanont-Payne cascade active inductor is given by

$$Z \approx \left(\frac{g_{01}g_{03}}{C_{gs1}C_{gs2}g_{m3}}\right)\frac{s\left(\frac{C_{gs2}g_{m3}}{g_{01}g_{03}}\right)+1}{s^2+s\left(\frac{g_{01}g_{03}}{C_{gs2}g_{m3}}+\frac{g_{01}}{C_{gs1}}\right)+\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \ldots\ldots\ldots(3.26)$$

The self-resonant frequency of the active inductor is given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.27)$$

and it stays unaltered. It ought not be astounded to see that cascodes try not to change ω_0 . This is on account of cascodes are not subject to Miller impact and has no impact on the transmission bandwidth. Cascode designs therefore can successfully enhance the frequency range scope of active inductors by bringing down the lower bound of the frequency range of active inductors.[29]

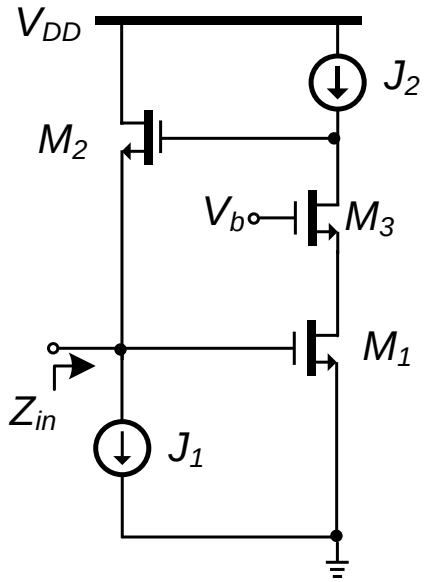


Figure 3.14:Thanachayanont-Payne active inductor

3.7.4 Weng-Kuo Cascode active inductor

Weng-Kuo cascode active inductor negates the limitation of that the inductance and the quality factor can't be varied. The simplified schematic of Weng-Kuo active inductor is shown in figure 3.14 where g_{m1} is proportional to J_1+J_3 while gm3 is only proportional to J_1. The parameters are defined as

Inductance, $L = \frac{C_{gs2}}{g_{m1}g_{m2}}$

Series resistance, $R_S = \frac{g_{01}g_{03}}{g_{m1}g_{m2}g_{m3}}$

Parallel capacitance, $C_P = C_{gs1}$,

Parallel resistance, $R_P = \frac{1}{g_{o2}}$.

And the Q factor is given by

$$Q(\omega_0) = \frac{\omega_{oL}}{R_s} = \frac{g_{m3}}{g_{01}g_{03}}\sqrt{\frac{g_{m1}g_{m2}C_{gs2}}{C_{gs1}}} \quad \text{.....(3.28)}$$

ω_0 can be tuned by varying g_{m1} and g_{m2}while Q can be tuned by varying g_{m3} only. So the tuning of Q can be made independent of ω_0. For the tuning of ω_0, Q will be affected.[41]

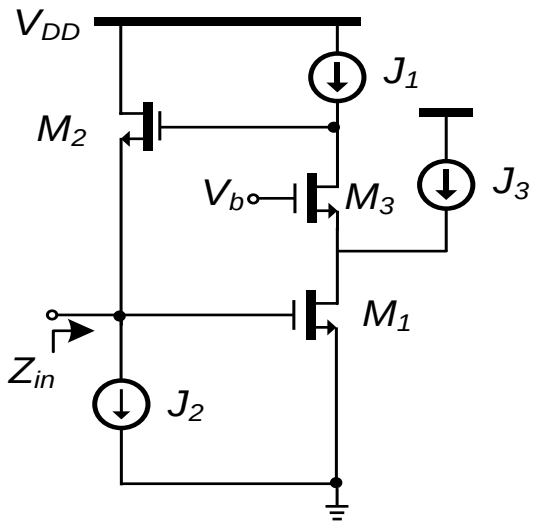


Figure 3.15:Weng-Kuo cascade active inductor

CHAPTER 04

OSCILLATOR

4.1 General Concept

An Oscillator is an electronic circuit which produces a continuous, repeated and alternating waveform. Oscillators convert a DC supply voltage from a power supply into an AC output of desired frequency, as decided by its circuit components which can have a wide range of different wave shapes and frequencies that can be either simple sine waves or complicated in nature such as square waves, triangular waves, and saw-tooth waves depending upon the application. A repetitive input signal is not required except to synchronize oscillations in some applications. Oscillators are widely used in numerous electronic devices like signal generator, touch-tone telephone, musical instruments, radio/television transmitters etc.

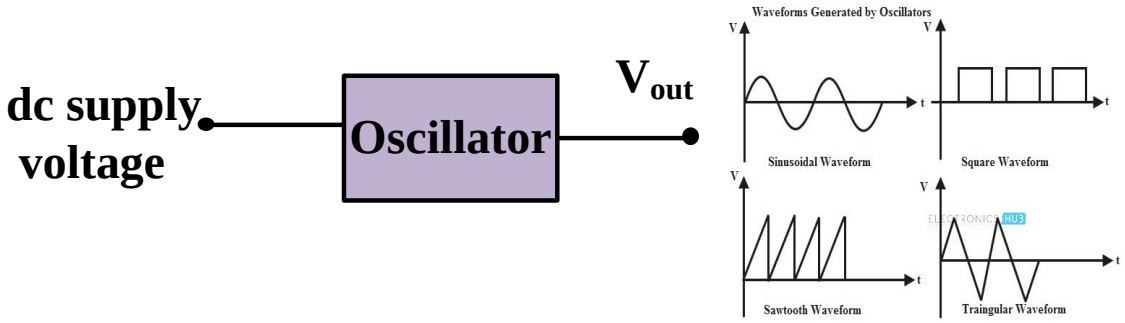


Figure 4.1: Oscillator (Basic)

4.2 Classification

Oscillators can be classified into two major types.

1. Feedback oscillators
2. Relaxation oscillators

4.2.1 Feedback oscillator

One type of oscillator is the feedback oscillator. Feedback oscillator is a circuit which returns a portion of the output signal to the input with no net phase shift, resulting in a increase of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp).

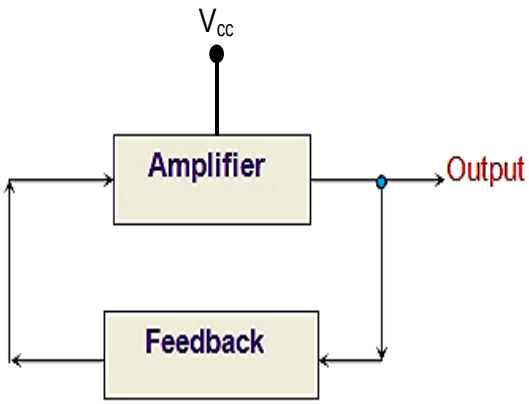


Figure 4.2: Feedback oscillator

4.2.2 Relaxation oscillator

A second type of oscillator is the relaxation oscillator. Instead of feedback, a relaxation oscillator uses an RC timing circuit to generate a waveform that is generally a square wave or other non-sinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.3 Further Classification

Oscillators can be classified into various types depending on the parameter considered.

- Based on the Feedback Mechanism
  1. Positive Feedback Oscillators
  2. Negative Feedback Oscillators
- Based on the Shape of the Output Waveform
  1. Sine Wave Oscillators
  2. Square or Rectangular Wave oscillators
  3. Sweep Oscillators (which produce saw-tooth output waveform)
- Based on the Frequency of the Output Signal
  1. Low Frequency Oscillators
  2. Audio Oscillators (whose output frequency is of audio range)
  3. Radio Frequency Oscillators

4. High Frequency Oscillators
5. Very High Frequency Oscillators
6. Ultra High Frequency Oscillators

- Based on the type of the Frequency Control Used
  1. RC Oscillators
  2. LC Oscillators
  3. Crystal Oscillators (which use a quartz crystal to result in a frequency stabilized output waveform)

- Based on the Nature of the Frequency of Output Waveform
  1. Fixed Frequency Oscillators
  2. Variable or Tunable Frequency Oscillators

4.4 Operation of Oscillator

The basic principle behind the working of oscillators can be understood by analyzing the behavior of a LC tank circuit shown by figure 1, which employs an inductor L and a completely pre-charged capacitor C as its components. Here, at first, the capacitor starts to discharge via the inductor, which results in the conversion of its electrical energy into the electromagnetic field, which can be stored in the inductor. Once the capacitor discharges completely, there will be no current flow in the circuit. However, by then, the stored electromagnetic field would have generated a back emf which results in the flow of current through the circuit in the same direction as that of before.

This current flow through the circuit continues until the electromagnetic field collapses which results in the back-conversion of electromagnetic energy into electrical form, causing the cycle to repeat. However, now the capacitor would have charged with the opposite polarity, due to which one gets an oscillating waveform as the output.

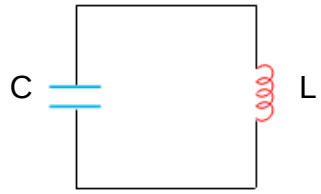


Figure 4.3: LC Tank circuit

However, the oscillations which arise due to the inter-conversion between the two energy-forms cannot continue forever as they would be subjected to the effect of energy loss due to the resistance of the circuit. As a result, the amplitude of these oscillations decreases steadily to become zero, which makes them damped in nature. These oscillations decay to zero as soon as the energy in the tank is consumed. If too much power is moved from the circuit, the energy may be completely consumed before the first cycle of oscillations can take place yielding the over damped response. This indicates that in order to obtain the oscillations which are continuous and of constant amplitude, one needs to compensate for the energy lost. Nevertheless, it is to be noted that the energy supplied should be precisely controlled and must be equal to that of the energy lost in order to obtain the oscillations with constant amplitude.

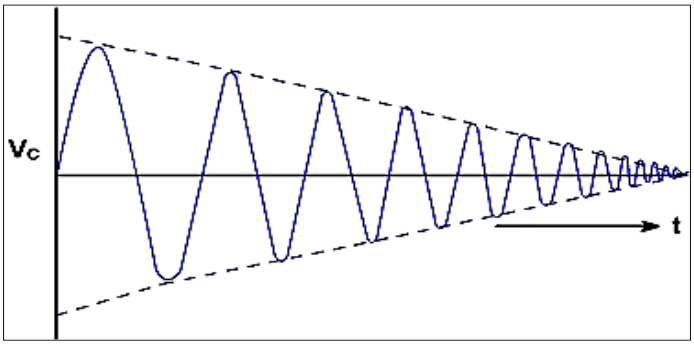


Figure 4.4: Oscillaton reduced due to losses(damped oscillation)

Since energy lost may be related to a positive resistance, it follows that the circuit would gain energy if an equivalent negative resistance were available. The negative resistance, supplies whatever energy the circuit lose due to positive resistance. Certain devices exhibit negative resistance characteristics, an increasing current for a decreasing voltage. The energy supplied by the negative resistance to the circuit, actually comes from DC source that is necessary to bias the device in its negative resistance region.

Another technique for producing oscillation is to use positive feedback. Positive feedback is characterized by the condition wherein a portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a reinforcement of the output signal.

Considering an amplifier with an input signal v_{in} and output v_0 as shown in fig. 4. The amplifier is inverting amplifier and may be transistor or FET or OPAMP. The output is 180° out of phase with input signal $V_0 = -A\,Vin$ (A is negative)

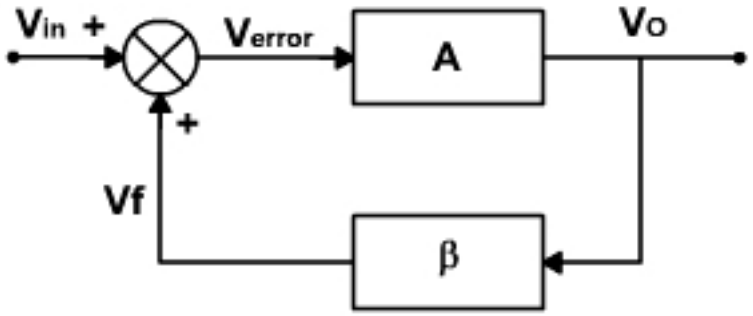


Figure 4.5: Feedback topology of oscillator

Now a feedback circuit is added. The output voltage is fed to the feedback circuit. The output of the feedback circuit is again 180° phase shifted and also gets attenuated. Thus the output from the feedback network is in phase with input signal V_{in} and it can also be made equal to input signal.

If this is so, V_f can be connected directly and externally applied signal can be removed and the circuit will continue to generate an output signal. The amplifier still has an input but the input is derived from the output amplifier. The output essentially feeds on itself and is continuously regenerated. This is positive feedback. The overall amplification from V_{in} to V_f is 1 and the total phase shift is zero. Thus the loop gain $A\beta$ is equal to unity.

When this criterion is satisfied then the closed loop gain is infinite. i.e. an output is produced without any external input.

$V_0 = A\, V_{error} = A\,(V_{in} + V_f) = A\,(V_{in} + \beta V_0)$ ……...….(4.1)

or $(1-A\beta)\,V_0 = A\,V_{in}$

or When $A\beta = 1$, $V_0 / V_{in} = \infty$

The criterion $A\beta = 1$ is satisfied only at one frequency. This is known as Barkhausen Criterion. Oscillation will not be sustained, if at the oscillator frequency, $A\beta < 1$ or $A\beta > 1$. If $A\beta$ is less than unity then $A\beta V_{in}$ is less than V_{in}, and the output signal will die out, when the externally applied source is removed. If $A\beta > 1$ then $A\beta V_{in}$ is greater than V_{in} and the output voltage builds up gradually. If $A\beta = 1$, only then output voltage is sine wave under steady state conditions.

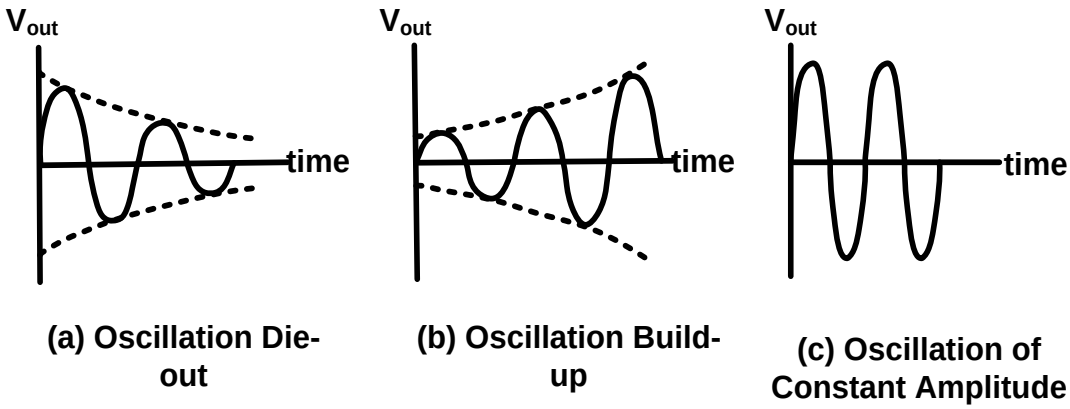


Figure 4.6: Oscillation Effects

Certain conditions are required to be fulfilled for sustained oscillations and these conditions are that

(i) The loop gain of the circuit must be equal to (or greater than) unity and

(ii) The phase shift around the circuit must be zero. These two conditions for sustained oscillations are called **Barkhausen criteria.**

In a practical oscillator, it is not necessary to supply a signal to start the oscillations. Instead, oscillations are self-starting and begin as soon as power is applied. This is possible because of electrical noise present in all passive components. Therefore, as soon as the power is applied, there is already some energy in the circuit at f_o, the frequency for which the circuit is designed to oscillate. This energy is very small and is mixed with all the other frequency components also present, but it is there. Only at this frequency the loop gain is slightly greater than unity and the loop phase shift is zero. At all other frequency the Barkhausen criterion is not satisfied. The magnitude of the frequency component f_o is made slightly higher each time it goes around the loop. Soon the f_o component is much larger than all other components and ultimately its amplitude is limited by the circuits own non-linearities (reduction of gain at high current levels, saturation or cut off). Thus the loop gain reduces to unity and steady stage is reached. If it does not, then the clipping may occur.

Practically, $A\beta$ is made slightly greater than unity. The voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained. But if $A\beta = 1$ and due to some reasons if $A\beta$ decreases slightly than the oscillation may die out and oscillator stop functioning.[52][54]

4.5 Oscillators With RC Feedback Circuits

4.5.1 The Wien-Bridge oscillator

One type of sinusoidal feedback oscillator is the Wien-bridge oscillator. The Wien Bridge oscillator is a standard oscillator circuit for low to moderate frequencies, in the range 5Hz to about 1MHz. It is mainly used in audio frequency generators. The Wien-bridge is an ac bridge in which balance is obtained only at a particular supply frequency. In this oscillator, the Wien-bridge is used as the feedback network between input and output. A lead-lag circuit is an essential element of the Wien-bridge oscillator. R_1 and C_1 together form the lag portion of the circuit; R_2 and C_2 form the lead portion. The operation of this lead-lag circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C_2. As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.

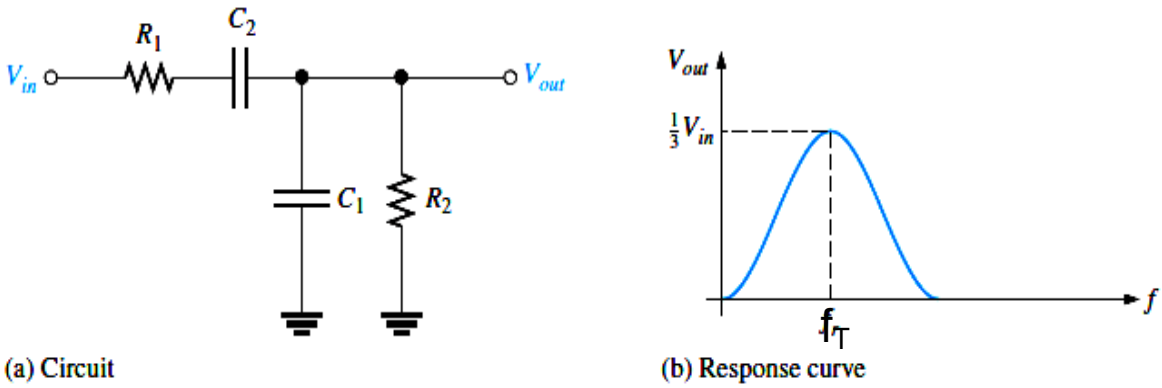


Figure 4.7: Response curve for the lead-lag circuit of Wien-bridge

The output voltage peaks at a frequency called the resonant frequency f_T.

Resistors R_1 and R_2 and capacitors C_1 and C_2 form the frequency-adjustment elements and resistors R_3 and R_4 form part of the feedback path. The op-amp output is connected as the bridge input at points a and c. The bridge circuit output at points b and d is the input to the op-amp.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \quad \text{.....(4.2)}$$

$$f_T = \frac{1}{2\pi\sqrt{(R_1 C_1 R_2 C_2)}} \quad \text{.....(4.3)}$$

if $R_1=R_2=R$ and $C_1=C_2=C$,

$f_T = \frac{1}{2\pi RC}$ ……..(4.4)

and $\frac{R_3}{R_4} = 2$……..……...……(4.5)

Thus a ratio of R_3 to R_4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the desired frequency.[49]

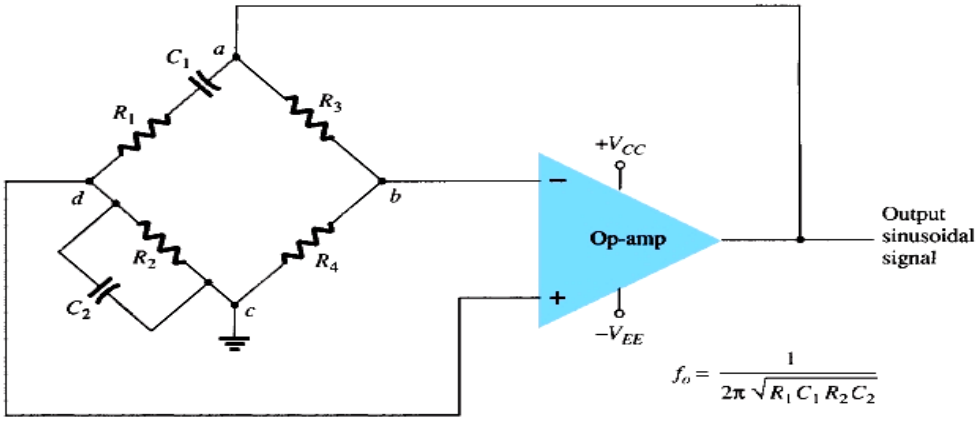


Figure 4.8: Wien-bridge circuit

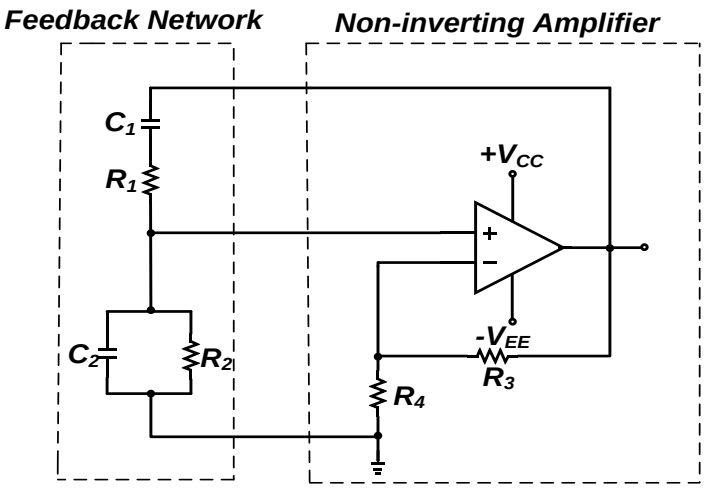


Figure 4.9: Simplified Wien-bridge circuit

4.5.2 The Phase-Shift oscillator

An example of an oscillator circuit that follows the basic development of a feedback circuit is known as the phase-shift oscillator. If the amplifier has an internal phase shift of 180° and the network provides a further 180° phase shift, the signal fed back to the input can be amplified

to reproduce the output. The circuit is then generating its own input signal, and a state of oscillation is sustained.

Figure shows an IC operational amplifier connected as an inverting amplifier to give a 180° phase shift between amplifier input and output. An RC network consisting of three equal-value capacitors and three equal resistors is connected between the amplifier output and input terminals. Each stage of the network provides some phase shift to give a total of 180° from output to input. The frequency of the oscillator output depends upon the capacitor and resistor values employed. Using basic RC circuit analysis methods, it can be shown that the network phase shift is 180° when the oscillating frequency is

$$f = \frac{1}{2\pi\sqrt{6}RC} \quad \text{.....(4.6)}$$

$\beta = {}^{1}/_{29}$ and the phase shift is 180°.

For the loop gain βA to be greater than unity, the gain of the amplifier stage must be greater than $1/\beta$ or 29: $A > 29$ [49]

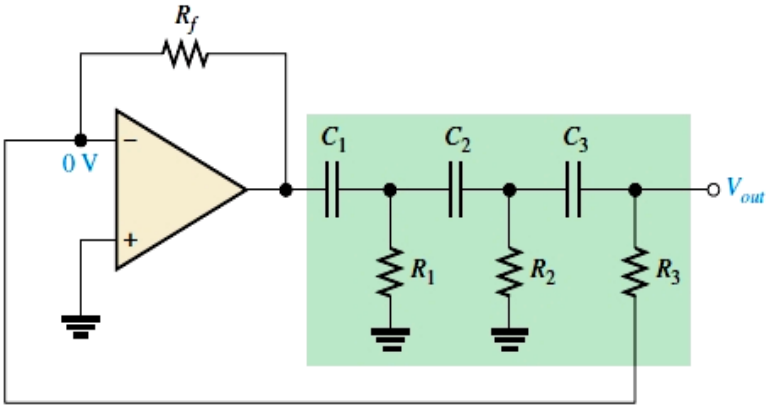


Figure 4.10: Phase shift oscillator circuit

4.5.3 Twin-T oscillator

Another type of RC feedback oscillator is called the twin-T because of the two T-type RC filters used in the feedback loop, as shown in Figure 4.11. One of the twin-T filters has a low-pass response, and the other has a high-pass response. The combined parallel filters produce a band-stop or notch response with a center frequency equal to the desired frequency of oscillation f_T. Oscillation cannot occur at frequencies above or below because of the negative feedback through the filters. At f_T however, there is negligible negative feedback; thus, the positive feedback through the voltage divider (R_1 and R_2) allows the circuit to oscillate.[49]

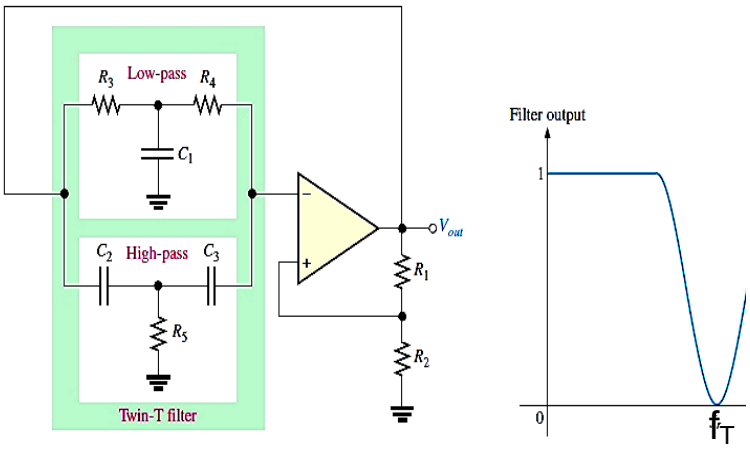


Figure 4.11: Twin T oscillator circuit and output waveform

4.6 Oscillators With LC Feedback Circuits

4.6.1 The Colpitts oscillator

Colpitts Oscillator is a type of LC oscillator which falls under the category of Harmonic Oscillator and was invented by Edwin Colpitts in 1918. The Colpitis oscillator circuit uses an LC network (C_1, C_2 and L) to provide the necessary phase shift between amplifier output voltage and feedback voltage. In this case the network acts as a filter to pass the desired oscillating frequency and block all other frequencies. The output voltage is developed across C_1. The feedback voltage is developed across C_2. The filter circuit resonates at the desired oscillating frequency. For resonance, $X_L=X_{CT}$ where X_{CT} is the reactance of the total capacitance in parallel with the inductance. This gives the resonant frequency (and oscillating frequency) as

$$f = \frac{1}{2\pi\sqrt{(LC_T)}} \quad \text{.....(4.7)}$$

where $C_T=\frac{C_1C_2}{C_1+C_2}$.Consideration of the LC network shows that its attenuation (from the amplifier output to input) is

$$\beta = \frac{X_{C1}}{X_L - X_{C1}} \quad \text{.....(4.8)}$$

It can be shown that when the 180° phase shift is achieved $(X_L\text{-}X_{C1}) = X_{CT}$. This gives $\beta=X_{C1}/X_{C2}$. For the loop gain to equal 1, $\beta A = 1$, and $A\frac{X_{C1}}{X_{C2}} \geq 1$. As for other oscillator circuits, the loop gain should be greater than unity to ensure that the circuit oscillates.[49][52]

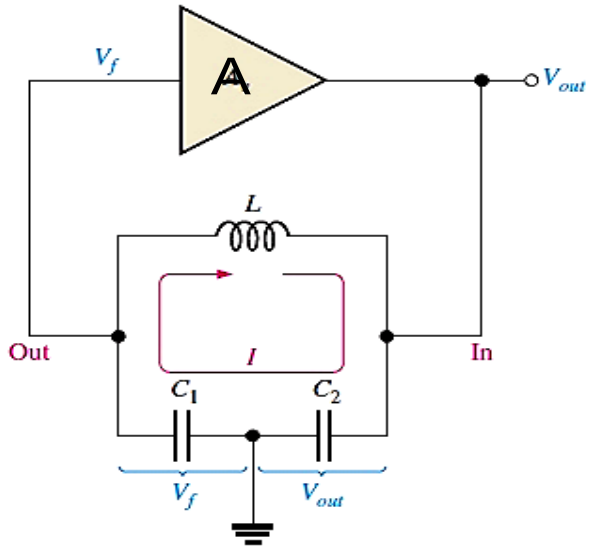


Figure 4.12: The Colpitts oscillator circuit

4.6.2 The Hartley oscillator

The Hartley oscillator circuit is similar to the Colpitts oscillator, except that the phase-shift network consists of two inductors and a capacitor instead of two capacitors and an inductor. L_1 and L_2 may be wound on a single core, so that there is mutual inductance between them. In this case the total inductance is given by $L_T=L_1+L_2+2M$ where M is the mutual inductance. As in the case of the Colpitts circuit, the frequency of oscillation is the resonant frequency of the phase-shift network. [49][51]

$$f=\frac{1}{2\pi\sqrt{(CL_T)}} \quad \text{.....(4.9)}$$

The attenuation of the phase shift network is $\beta=\frac{X_{L1}}{X_{L1}-X_C}$. for a 180° phase shift $(X_{L1} — X_C)$ can be shown to equal X_{L2}. For the loop gain to be at least 1, $A\frac{X_{L1}}{X_{L2}} \geq 1$.

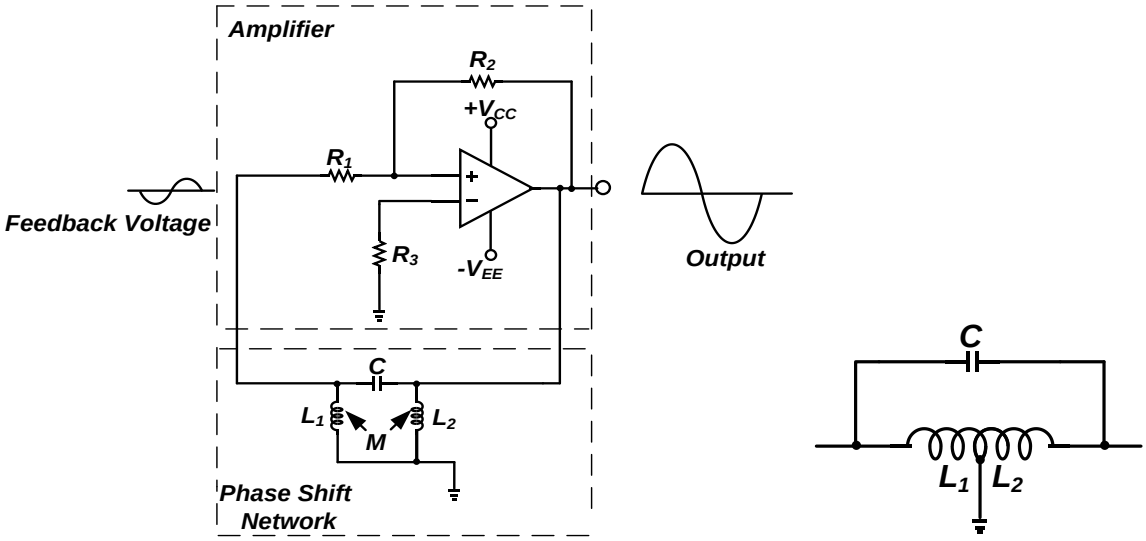


Figure 4.13: The Hartley oscillator

4.6.3 The Armstrong oscillator

This type of LC feedback oscillator uses transformer coupling to feed back a portion of the signal voltage, as shown in figure 4.14. It is sometimes called a "tickler" oscillator in reference to the transformer secondary or "tickler coil" that provides the feedback to keep the oscillation going. The Armstrong is less common than the Colpitts, and Hartley, mainly because of the disadvantage of transformer size and cost. The frequency of oscillation is set by the inductance of the primary winding (L_{pri}) in parallel with C_1.[49][51]

$$f_T = \frac{1}{2\pi\sqrt{(L_{pri}C_1)}} \quad \text{.....(4.10)}$$

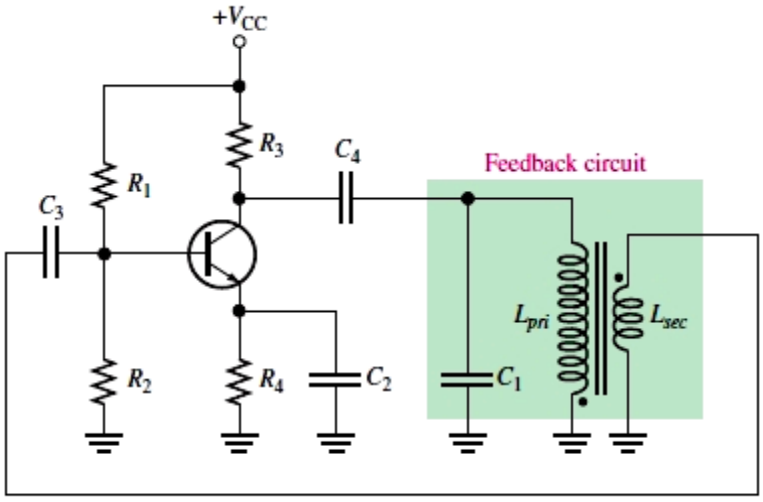


Figure 4.14: The Armstrong oscillator

4.7 Voltage Controlled Oscillator(VCO)

A voltage controlled oscillator (VCO) is an crucial component in the field of RF high frequency communication systems. Voltage controlled oscillator is an oscillator with an output signal whose output can be varied over a range, which is controlled by the input DC voltage. It is an oscillator whose output frequency is directly related to the input voltage. The oscillation frequency varies from few hertz to hundreds of GHz. By varying the input DC voltage, the output frequency of the produced signal is adjusted. The design of a high performing voltage controlled oscillator, VCO is not a trivial task. Consideration of the circuit, components used and the layout all play a role in determining the performance. This requires sound theoretical design, followed by careful choice of all the components.

When the input voltage is zero, the oscillation frequency is set to a minimal value ω_o, which can be adjusted to zero also. The oscillation frequency for a VCO is given by the following expression: $\omega=\omega_o+K_oV_{in}$,Where K_o is the gain coefficient (rad/s/volt).

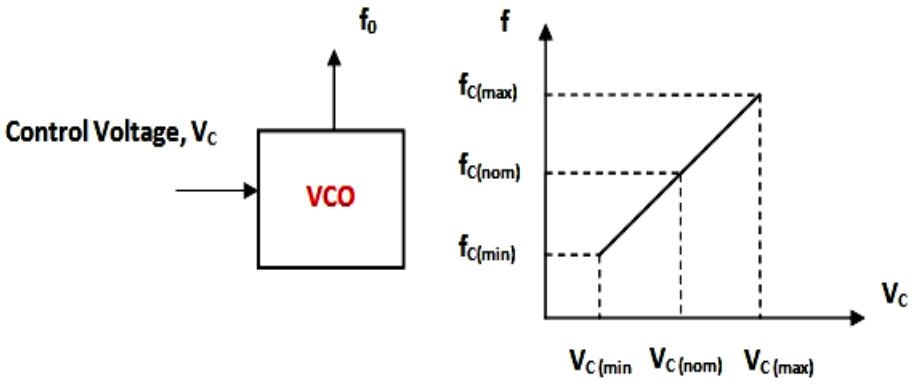


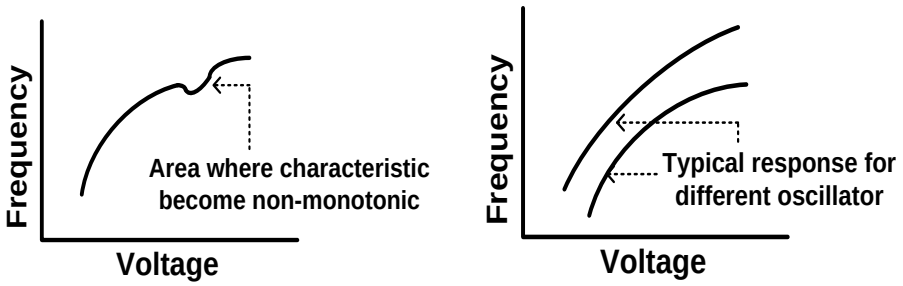
Figure 4.15: Voltage Controlled Oscillator block diagram

The figure above represents the basic working of voltage controlled oscillator. Here, it can be seen that at nominal control voltage represented by $V_{C(nom)}$, the oscillator works at its free running or normal frequency, $f_{C(nom)}$. As the control voltage decreases from nominal voltage, the frequency also decreases and as the nominal control voltage increases, the frequency also gets higher value.[52][53][54]

4.7.1 VCO design requirements

- **Phase noise**: Phase Noise in VCO is of particular importance in order to meet the sensitivity, adjacent channel and blocking requirements. In digital modulation scheme the VCO's Phase Noise affects the Bit Error Rate requirements.

- **Tuning slope**: The tuning slope is the slope of the frequency to voltage tuning characteristic at any point and is the same as modulation sensitivity. The slope could be positive or negative. For a positive slope, the output frequency increases as the tuning voltage increases. Similarly for a negative slope, the output frequency decreases as the tuning voltage increases. It is an important characteristic for any voltage controlled oscillator used in a phase locked loop that the voltage to frequency curve is monotonic, i.e. it always changes in the same sense, typically increasing frequency for increasing voltage. In other words the frequency is single valued at any tuning voltage and that the slope has the same sign across the tuning range. If it changes, as can happen in some instances normally as a result of spurious resonances, etc., this can cause the loop to become unstable. Accordingly, this must be prevented for satisfactory performance of PLL.



(a) **(b)**

Figure 4.16: Voltage Controlled Oscillator v/f curve

- **Tuning gain**: The gain of the voltage controlled oscillator is measured in terms of volts per Hz (or V/MHz, etc). As implied by the units it is the tuning shift for a given change in voltage. The voltage controlled oscillator gain affects some of the overall loop design considerations and calculation.

- **VCO tuning range:** It is obvious that the voltage controlled oscillator must be able to tune over the range that the loop is expected to operate over. This requirement is not

always easy to meet and may require the VCO or resonant circuit to be switched in some extreme circumstances. The desired tuning range is dictated by two parameters: (1) the variation of VCO center frequency with process and temperature. (2) application dependent frequency range. At the extreme conditions of process and temperature, the center frequency of CMOS oscillators may vary by a factor of two. Thus a adequate wide tuning range is maintained to ensure the output van be driven o desired value.

- **Supply and Common Mode rejection:** VCOs are vulnerable to noise, specially when realized in a single ended form. Even sometimes supply sensitivity is showed by differential oscillators too. High noise immune design of a VCO is a difficult task. The control line of a VCO might also be coupled with noise. So more advisable to employ differential paths for both the oscillation signal and the control line.

- **Power dissipation:** VCOs endure trades off between noise, speed and power dissipation. Typical power dissipation is 1 to 10 mW.

- **Output amplitude:** Large output amplitude makes the waveform less sensitive to noise. The amplitude trades with power disipation, supply voltage and tuning range. An unappealing effect is that he amplitude might vary across the tuning range.

- **Output signal purity:**The output waveform of a VCO may not be perfectly peiodic with a constant control voltage. Noise in the output phase and frequency cnsists of electronic noise in the device and supply noise. These effects are classified as jitter and phase noise and determined by application requirements.

4.8 Ring Oscillator

Ring oscillator is the cascaded combination of delay stages connected in a close loop chain. The ring oscillators designed with a chain of delay stages have created great interest because of their numerous useful features. This oscillator creates phase shift of 2π and gain in each stage so that the Barkhausen criteria is satisfied. The phase shift is π/N in each stage, where N is the number of stages. The remaining phase shift is rendered by dc inversion. This type of VCO can generate oscillation frequency but no tuning range which is not expected as wide tuning range is needed in modern digital communication system. Therefore, this ring VCO is more sensitive to noise (phase noise, supple sensitivity and common-mode-rejection) than

other kinds. The oscillation frequency of ring VCO can be determined by estimating the delay time

$f_{osc} = \frac{1}{2N\tau}$……..……...……(4.11)

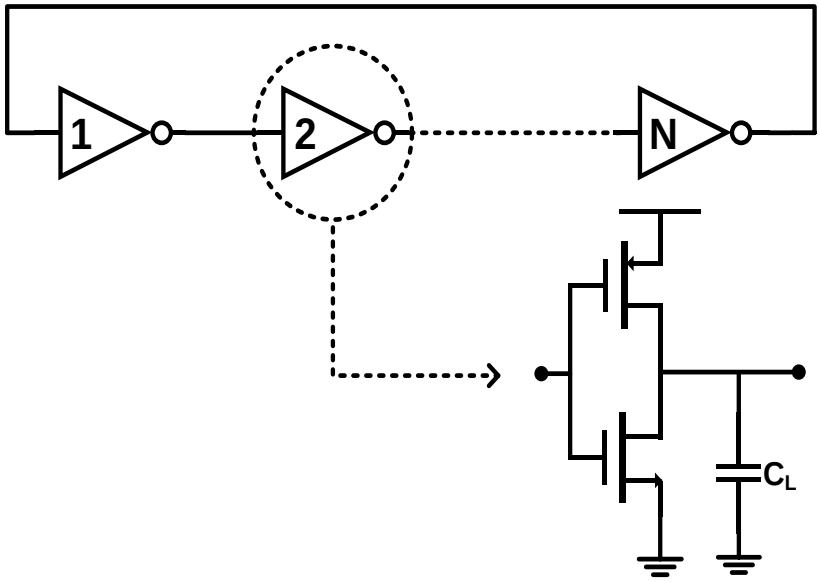


Figure 4.17: Ring Oscillator

Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input. The final output is asserted a finite amount of time after the first input is asserted and the feedback of the last output to the input causes oscillation. A circular chain composed of an even number of inverters cannot be used as a ring oscillator. The last output in this case is the same as the input. [50]

Table 4.1: Difference between Ring VCO and LC VCO

	Ring VCO	LC VCO
Tuning range	Very wide due to current variation	Narrow: proportional to the square root of varactor tuning.
Phase noise	Very poor: widen loop bandwidth to reduce.	Very good: filtering inherent to LC tank.
Power consumption	Can vary greatly: higher power needed for good phase noise.	Greater than ring VCO power consumption with equivalent frequency coverage but consumes lower power for same phase noise.
Gain	High: sensitive to power supply noise injection, Not suitable for SONET transmit clocks, Poor stability at high frequency.	Low: very sensitive to supply source variations and noise injection.
Layout area	Small.	Large area for inductor required Require a lot of characterization, Poor integration and more complicated design.
Overall performance comparison	Common approach for digital chips Many ways to control frequency Multiphase clock generation Wide frequency tuning range Low power/area at low frequency.	Common approach for RF design, Good stability, Long-term and period jitter filtering lead to Low long-term and period jitter Transients in RC oscillators are faster than in LC, and oscillation frequency is proportional to the tail current.

CHAPTER 05

LC VOLTAGE CONTROLLED OSCILLATOR (VCO)

5.1 Introduction

Another class of VCOs employs inductors and capacitors to define the oscillation frequency is called the LC VCOs. These circuits can be realized in both integrated and discrete form but with different topologies and design constraints. These VCOs are designed using inductors, capacitors and an amplifier. Very high frequency voltage controlled oscillations can be generated by using inductors and capacitors. This architecture is preferred for sinusoidal wave output.

5.1.1 General LC tank VCOs

A general LC VCO consists of an inductor, *L* and a capacitor, *C* building an parallel resonant tank. An active element *-R*, compensating the losses of the inductor and the losses of the capacitor. The circuit results into an oscillator with angular center frequency $\omega_c = \frac{1}{\sqrt{LC}}$.

As the capacitance *C* is proportional to the tuning voltage input V_{in}, also ω_c is dependent on V_{in} and the oscillator results in a voltage controlled oscillator. The capacitor C in figure 5.1 not only consists of a variable capacitor to tune the oscillator, but it also includes the parasitics or fixed capacitances of the inductor, the active elements, and of any load connected to the VCO (output driver, mixer, prescaler, etc.).

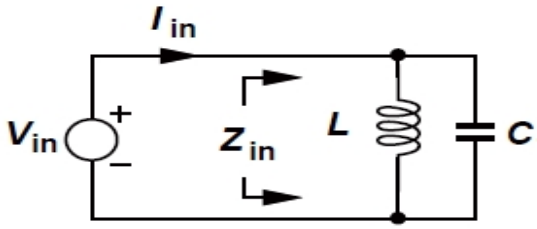


Figure 5.1: Impedance of a parallel LC tank.

An ideal parallel LC tank provides an impedance given by $Z_{in} = Ls \,||\, \frac{1}{Cs} = \frac{Ls}{LCs^2+1}$. For a sinusoidal input voltage, $s=j\omega$ and $Z_{in} = \frac{jL\omega}{1-LC\omega^2}$. the impedance goes to infinity at $\omega_c = \frac{1}{\sqrt{LC}}$.

At $\omega = \omega_c$, the inductor and the capacitor exhibits equal and opposite impedances ($jL\omega_c$ and $\frac{1}{jC\omega_c}$), canceling each other out and yielding an open circuit. That is an infinite impedance. The tank circuit resonates at $\omega = \omega_c$. in real applications, the impedance of a parallel LC

tank does not go to infinity at the resonant frequency. They suffer from resistive components. The circuit is now called a “lossy tank” to emphasize the loss of energy within the inductor’s resistance. [50][54]

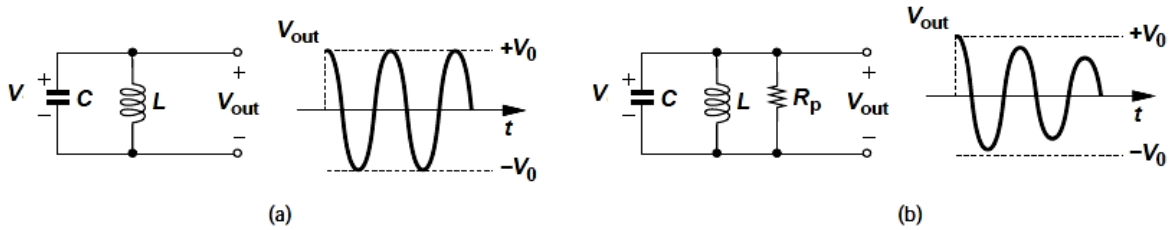


Figure 5.2: Time-domain behavior of (a) ideal and (b) lossy tanks

5.1.2 Cross coupled LC VCOs

An oscillator must have a sufficiently large voltage gain in order to satisfy Barkhausen criteria and start an oscillation in a short period of time. A common source stage using a parallel LC tank is in figure 5.1. The voltage gain of a delay stage is given by $A_v = -g_m Z$, where Z is the impedance of the LC tank. A large voltage gain exists at the self-resonant frequency of the LC tank. This is because for an ideal LC tank, the impedance of the tank at the resonant frequency is infinite, ω_c. i.e. $Z(j\omega_c) = \infty$, where $\omega_c = \frac{1}{\sqrt{LC}}$ is the resonant frequency of the LC tank, L and C are the inductance and capacitance of the tank respectively. For a lossy LC tank, $Z(j\omega_c)) = R_p$, where R_p is the shunt resistance of the tank.

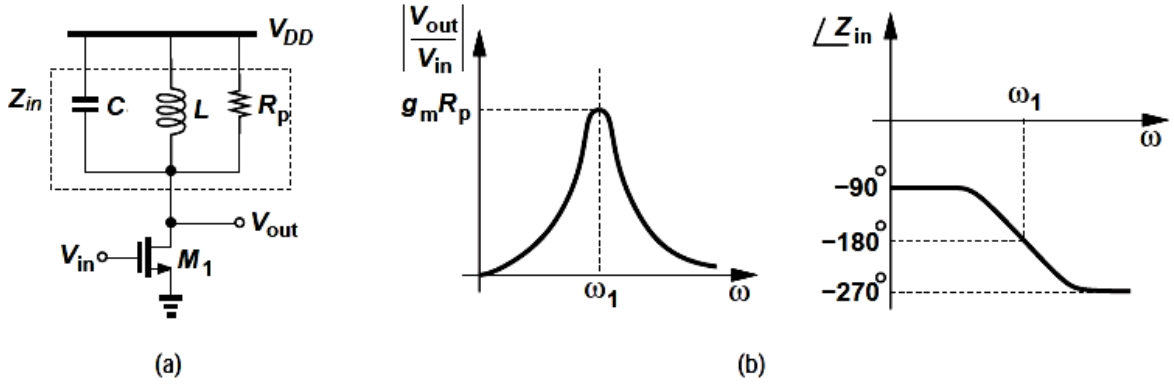


Figure 5.3: (a) CS stage with a tank load, (b) magnitude and phase plots of the stage

When neglecting the capacitances of the transistor, the voltage gain of the common-source amplification stage with a lossy LC tank load at the resonant frequency of the LC tank is given by $A = -g_m R_p$. The CS stage thus exhibits a gain that reaches a maximum of $g_m R_p$ at resonance and approaches zero at very low or very high frequencies. The phase shift at ω_c is

equal to 180◦ because the load reduces to a resistor at resonance. The total phase shift around the loop must reach 360◦ at a finite frequency, but figure (b) reveals that this is not possible. If one more CS stage is inserted then each stage provides 180◦, for a total phase shift of 360◦. Thus, the circuit oscillates at ω_c if the loop gain at this frequency is sufficient. Since each stage has a voltage gain of $g_m R_p$ at ω_c, Barkhausen's loop gain criterion translates to $(g_m R_p)^2 \geq 1$. A critical issue in the above topology is that the bias current of the transistors is poorly defined. Since no current mirror or other means of proper biasing are used, the drain currents of M_1 and M_2 vary with process, supply voltage, and temperature. For example, if the transistors' threshold voltage is lower than the nominal value, then the peak value of V_X yields a greater overdrive voltage for M_2 and hence a larger drain current. To resolve this issue, the gate of each device is tied to the drain of the other. M_1 and M_2 almost resemble a differential pair whose output is fed back to its input.

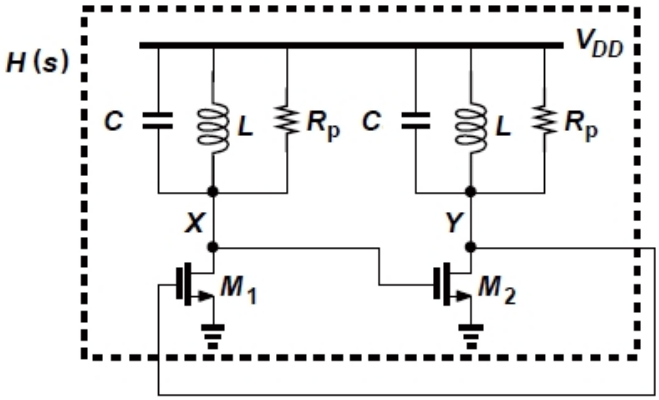


Figure 5.4: Two LC-load CS stages in a loop

If the tank is lossy, in order to start an oscillation and sustain the oscillation, a negative resistor connected in parallel with the LC tanks is required to cancel out the resistance of the tanks so that the tanks are lossless. The added negative resistor has two distinct functions : (i) The amplification stages of the LC oscillator have sufficiently large voltage gains to start an oscillation. (ii) The loss of the oscillator is sufficiently small so that an oscillation of a constant amplitude can be sustained.

A widely used differential negative resistor is the cross-coupled transistor pair consisting of $M_{1,2}$ and the tail biasing current source J, as shown in figure 5.5 A tail biasing current source in this case is needed to provide dc biasing currents for $M_{1,2}$ and to tune the resistance. The resistance of the negative resistor can be tuned by varying the dc biasing current. The

resistance of the negative resistor must be at least equal to the resistance of the LC tanks so that the ohmic loss of the tanks can be eliminated completed. For practical circuits, a rule-of-thumb is to set the resistance of the negative resistor three times the resistance of the LC tanks so that the effect of process variation, supply voltage fluctuation, and temperature drift of practical LC oscillators can be accounted for adequately. [18][50][54]

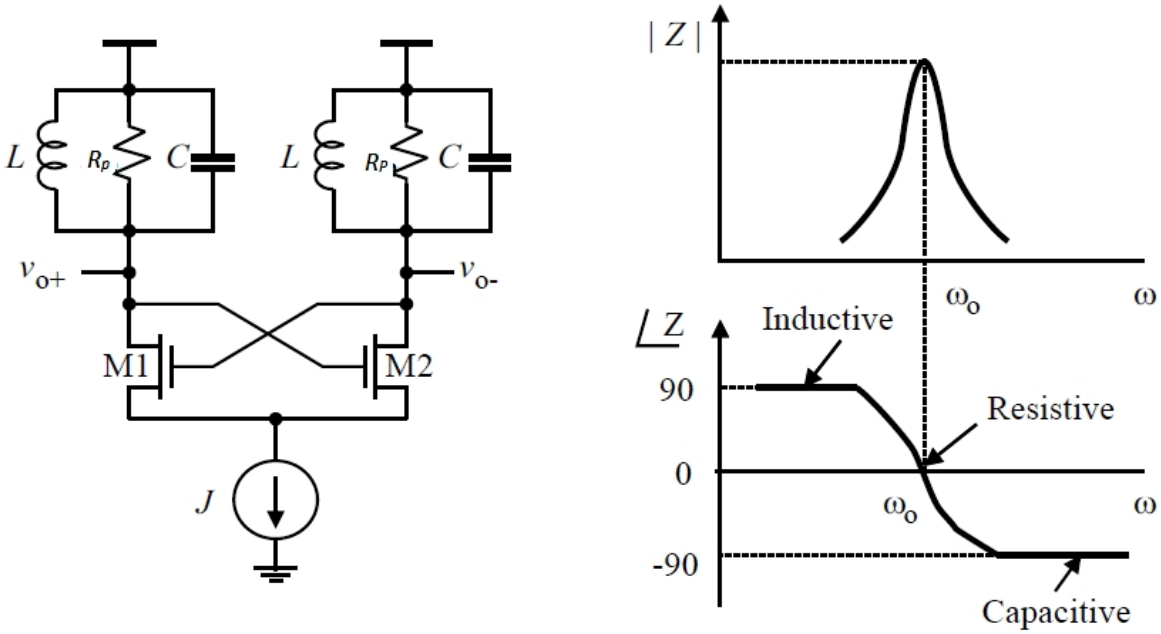


Figure 5.5: Cross coupled LC VCO

5.2 LC Tank Properties

LC VCOs are mainly based on LC tanks. So the properties of the LC tank plays a vital role in the overall performance of the VCO.

- Series and Parallel Resistance: The parallel LC tank is preferred to the series LC circuit. The parallel LC tank is closer to the physical losses in the integrated inductors and the insight into the optimal inductor design is improved significantly. For the two circuits to approximately equivalent

  $$R_p = \frac{L_s}{CR_s} \quad \text{.....(5.1)}$$

- Center Frequency: An LC-tank can be treated as a bandpass filter, its center frequency is the frequency f_c (or angular frequency $\omega_c = 2\pi f_c$) where the amplitude response reaches its maximum. It has been calculated that

$\omega_c = \frac{1}{\sqrt{LC}}$……..…….(5.2)

The environment dictates the center frequency in which the VCO can be operated. A VCO may be required to operate at the clock rate or even twice that in the clock generation network of a microprocessor.[55]

5.3 Phase Noise

Phase noise is interpreted as the ratio of the peak carrier signal to the noise at a specific offset off the carrier expressed in dB below the carrier in a 1-Hz bandwidth. Since most measurements done are in a wider bandwidth, the correction factor is

C = 10 log(B)……..(5.3)

Considerable study has been done about the phase noise of VCOs. Numerous mathematical models have been proposed too. The most cited expression of power of the single side band phase noise of a VCO is stated as[59]

$$L(\Delta\omega) = 10\log\{\frac{2FkT}{P_s}[1 + (\frac{\omega_0}{2Q\Delta\omega})^2](1 + \frac{\Delta\omega_1/_{f^3}}{\Delta\omega})\}\text{……..…...}(5.4)$$

Where $\Delta\omega$ is the frequency offset from the oscillation frequency ω_0, Q is the quality factor of the oscillator, F is the excess noise factor, k is Boltzmann constant, T is absolute temperature in degrees Kelvin, P_s is the average power loss of the oscillator and $\Delta\omega_1/_{f^3}$ is the corner frequency between$\frac{1}{f^2}$ and $\frac{1}{f^3}$ regions. 1/f-noise is up-converted to the vicinity of the oscillation frequency. This region is identified as the $1/f^3$-region and affects the phase noise of the oscillators the most. The $1/f^2$-region of the phase noise spectrum is due to the white noise sources of the oscillators whereas the flat region is due to the white noise sources of the output buffers.

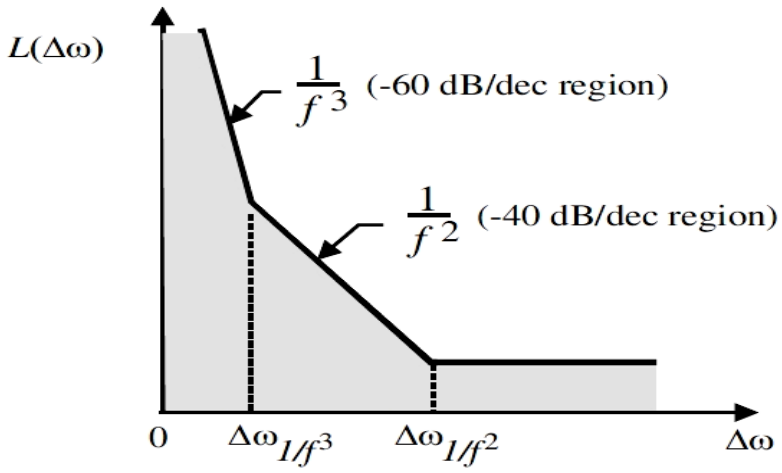


Figure 5.6: Phase noise spectrum of oscillators

5.4 Figure of Merit

The performance of VCOs is difficult to compare as they feature different center frequencies, power consumption P_{supply}, and phase noise over offset frequency. A widely accepted figure of merit has been introduced in

$FOM = L(f_o, \Delta f) - 10 \log \left(\left(\frac{f_0}{\Delta f}\right)^2 / \left(\frac{P_{supply}}{mW}\right)\right)$ ……(5.5)

where $L(f_o, \Delta f)$ is the single-side-band noise at the offset frequency Δf from the carrier frequency f_0.

This FOM is a direct deviation of Leesons empirical phase noise [59] expression normalized to the power consumption. For a fair comparison the worst-case measured phase noise of a VCO-design should be taken into account. The performance of a VCO is regarded to be better with a more negative value or higher absolute value of the figure of merit.

5.5 LC VCOs With Spiral Inductors Drawbacks

Spiral inductors based LC VCOs render a pivotal privilege of a low level of phase noise. These VCOs often used in various wireless applications where stringent constraint on phase noise exists. Tuning of frequency of monolithic spiral LC VCO is typically carried out by varying the capacitance of the LC tanks as the inductance tuning of spiral inductors in a

monolithic integration is rather difficult. MOS varactors are usually employed to realize the capacitors. As a result, monolithic spiral LC oscillators have a small frequency tuning range. Spiral LC VCO endures a number of setbacks.

- **Low self-resonant frequency** - The self-resonant frequency of a spiral inductor is set by the inductance of the spiral and the parasitic capacitance between the spiral and the substrate. The large metal area of the spiral gives rise to a large spiral substrate capacitance, which limits the self-resonant frequency of spiral inductors to a few GHz typically.

- **Low quality factor** - The ohmic losses of spirals at high frequencies, mainly due to the skin-effect induced resistance of the spirals and the substrate eddy-current induced resistance, limits the quality factor of spiral inductors to below 20 typically. Although the ohmic losses can be compensated for by employing negative resistors, the compensation result is generally poor over a large frequency range. This is because negative resistors are active networks while the parasitic resistance of spirals is a strong function of frequency.

- **Large Si Area** - A notable disadvantage of LC oscillators with spiral inductors or transformers is the large silicon area required for the fabrication of the spiral inductors and transformers. Not only the inductance of spiral inductors is low, the silicon area occupied by spiral inductors is also proportional to the inductance of the spiral inductors. Often, the silicon area of a RF front-end is primarily consumed by a few spiral inductors.

5.6 LC VCOs With Active Inductors

5.6.1 LC VCOs with Lin-Payne active inductors

Lin-Payne active inductors were used in design of LC oscillators. Figure 5.7 shows the simplified schematic of a LC oscillator with Lin-Payne active inductors. The pMOS transistor branches are used as inductance tuning branches subsequently frequency tuning branches while the nMOS transistor branches are connected to a negative resistor to cancel out the parasitic resistances of the active inductor. The resistance of the negative resistor is tuned by varying J_2 for a total compensation. This in turn adjusts the quality factor of the LC

oscillator. The inductance of the active inductors is tuned by varying J_1. The quality factor and oscillation frequency of the oscillator can thus be tuned independently.

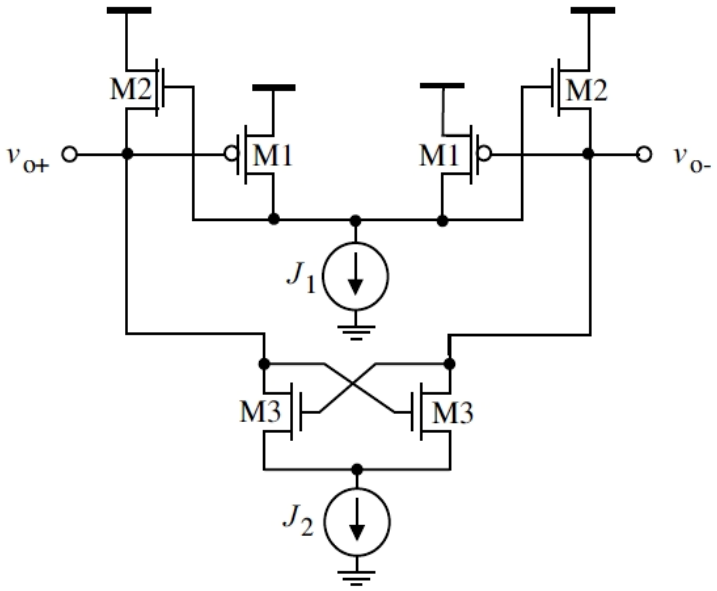


Figure 5.7: Simplified schematic of LC VCO with Lin-Payne active inductors

It was demonstrated in [28] that in a 0.35μm implementation of a LC oscillator with Lin-Payne active inductors, the phase noise of the oscillator when Q = 7 was -83 dBc/Hz at 600 kHz frequency offset from a 1.5 GHz oscillation frequency. The power consumption of the oscillator was 2.5 mW. When Q = 24, the phase noise was reduced to -88 dBc/Hz at 600 kHz frequency offset from a 2.5 GHz oscillation frequency. The power consumption in this case was 4.5 mW. The frequency tuning range of the oscillator was 48%. The total active area of the oscillator excluding the biasing current sources was only 24 μm^2.[18]

5.6.2 LC VCOs with Wu Current-Reuse Active Inductors

Figure 5.8 is the simplified schematic of a voltage-controlled LC oscillator employing Wu current-reuse active inductors. Transistors $M_{1,2,3a/b}$ form two Wu current reuse active inductors whose inductance is tuned by varying the dc biasing current J_1. Transistors $M_{4a/b}$ and J_2 form a negative resistor whose resistance is given by $-\frac{2}{g_{m4}}$ approximately and is tunable by varying J_2. This negative resistor is used to cancel out the parasitic resistances of the active inductors. As demonstrated in [43], the silicon area of the VCO implemented in a 0.35μm 3V CMOS technology was only 100μm×120μm. Frequency tuning range of the VCO

was from 100 MHz to 900 MHz with phase noise of approximately -95 dBc/Hz at 500 kHz frequency offset. The high level of the phase noise is mainly due to the use of the active inductors and the tail current source of the negative resistor. Note that the phase noise can be improved by removing the tail current source of the negative resistor with the downside that the resistance of the negative resistor will not be variable. [18]

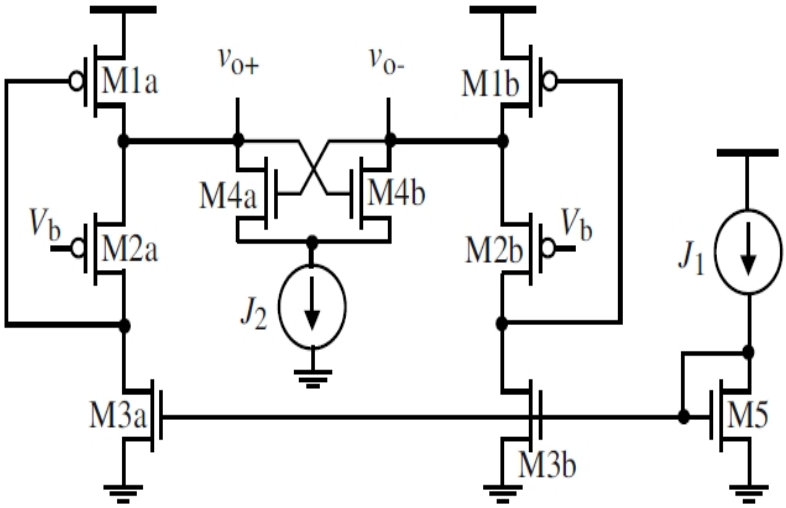


Figure 5.8 : Simplified schematic of LC VCO with Wu current-reuse active inductors

CHAPTER 06

PROPOSED ACTIVE INDUCTOR BASED VCO

6.1 Weng-Kuo Active Inductor

Till now from the previous chapter, it was found for Weng-Kuo active inductor

Inductance, $L = \frac{C_{gs2}}{g_{m1}g_{m2}}$.....(6.1)

Series resistance, $R_S = \frac{g_{01}g_{03}}{g_{m1}g_{m2}g_{m3}}$.....(6.2)

Parallel capacitance, $C_P = C_{gs1}$.....(6.3)

Parallel resistance, $R_P = \frac{1}{g_{o2}}$.....(6.4)

Self-resonant frequency, $\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}}$.....(6.5)

Quality factor, $Q(\omega_0) = \frac{\omega_o L}{R_s} = \frac{g_{m3}}{g_{01}g_{03}}\sqrt{\frac{g_{m1}\, g_{m2}C_{gs2}}{C_{gs1}}}$ .....(6.6)

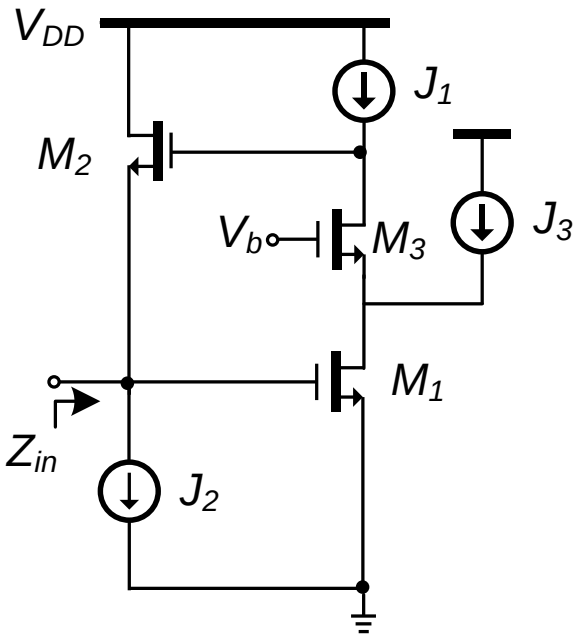


Figure 6.1: Weng-Kuo active inductor

J_1 & J_2 are used for biasing MOSFETS. J_3 is used for tuning the inductance and Q factor independently. As the ideal current source is impractical, J_1 , J_2 and J_3 have been replaced by M_4, M_6 and M_5 which act as current sources operating in saturation region.

6.1.1 Design criteria

- The power consumption should be as low as possible.
- The series resistance R_s should be as low as possible so that the Q factor will increase because of reduced ohmic loss.
- The self-resonant frequency should be higher so that the active inductor can be used in high frequency applications.

6.1.2 Applied formula

The drain to source current through a n-MOS is given by,

$$I_{DS} = \frac{W}{L}\mu_n C_{OX}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}] \dots\dots When\ V_{DS} < (V_{GS} - V_{th})[Linear\ region]$$

.....(6.7)

$$I_{DS} = \frac{1}{2}\frac{W}{L}\mu_n C_{OX}(V_{GS} - V_{TH})^2 \dots\dots When\ V_{DS} > (V_{GS} - V_{th})[Saturation\ region]$$

.....(6.8)

Here, $\mu_n C_{OX}$=process parameter

V_{TH}= Threshold voltage

V_{DS}= Drain to source vlotage

The transconductane of n-MOS is given by

$$g_m = \sqrt{2\mu_n C_{OX}\frac{W}{L}I_{Ds}}$$.....(6.9)

As the process parameter is always fixed, if W/L ratio or the drain to source current I_{DS} is changed, then g_m will be changed.

6.1.3 Choosing (W/L) ratio for MOSFETs used in Active Inductor

M_2: M_2 is used as feedback transistor for the feedback path and it has positive transconductance as it is in common drain configuration. If is concentrated on the previously described equations, it can be noticed that the increment of g_{m2} will decrease the series

resistance R_s for which the Q factor will increase and likewise the self-resonant frequency will increase. So the higher the estimation of g_{m2} i.e. W/L ratio, the better for the Q factor and self-resonant frequency. But increment of the W/L causes enhancement the drain to source current (I_{ds}), which will increase the power consumption. So the optimum value of the W/L ratio is 15μm/100nm which is comparatively greater than others to boost the Q factor and the self-resonant frequency.

M_1: M_1 is employed as forward path transistor and has negative transconductance due to its common source configuration. The increment of g_{m1} will happen the same changes in the performance parameters such as series resistance, Q factor and self-resonant frequency as described for the preceding transistor M_2. So the optimum value of the W/L ratio is 27μm/200nm which almost same as M_2.

M_3: M_3 is used as cascode to maximize the frequency range by reducing the zero frequency $\omega_z(=\frac{g_{01}}{C_{gs2}})$ that divides the zero frequency by a factor of $g_{m3}r_{o3}$. Again it contributes to decrease the series resistance R_s and upgrade the Q factor at the same rate. The optimum value of W/L ratio which has been achieved from simulation is 30μm/350nm.

M_4 and M_6: These two transistors are substitute of the biasing current sources J_1 and J_3 which are operated in saturation region as it is known that MOS operated in saturation region acts as current source. The higher value of W/L ratio will result in an increment of the drain to source current. Though it will boost the g_{m2}, g_{m3} and g_{m1}, it will further support the power consumption. As g_{m1}, g_{m2} and g_{m3} have already been increased by choosing a higher W/L ratio so the W/L ratio of M_4 and M_6 will be kept as low as possible to curtail the power consumption. The optimized value of W/L ratio is 10μm/200nm for M_4 and 5μm/200nm for M_6.

M_5: M_5 is the replacement of the current source J_3 which is used for tuning inductance and Q factor independently. Also it has a contribution for increasing the transconductance of the M_1 i.e. g_{m1} without distorting the other parameters. But there also exists a contradictory case that increasing W/L will further increase the power consumption. So the optimum value is 22μm/200nm.

6.2 Schematic Representation of Active Inductor

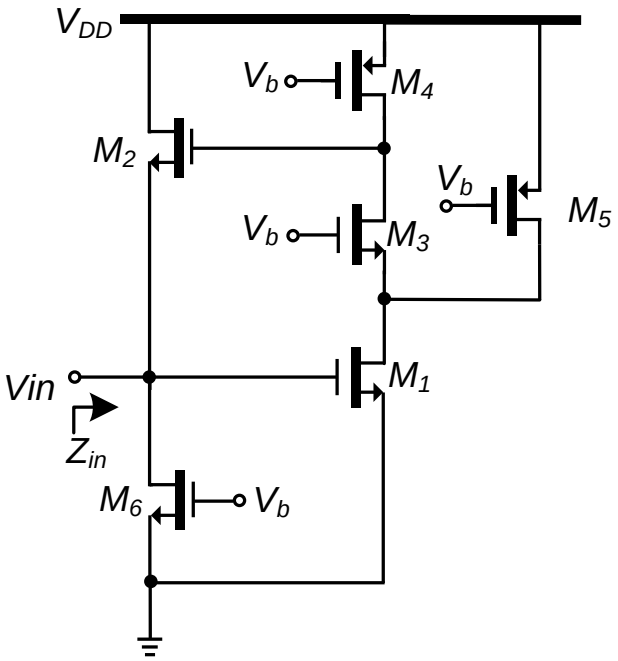


Figure 6.2: Weng-Kuo active inductor for the designed VCO

Table 6.1: Widths and lengths of the implemented transistors

MOS	Width(µm)	Length(nm)
M_1	27	200
M_2	15	100
M_3	30	350
M_4	10	200
M_5	22	200
M_6	5	200

6.3 Active Inductor Based VCO

6.3.1 Barkhausen criteria

A small change In DC power supply or noise component in oscillator circuit can start oscillation and to maintain oscillation in circuit must satisfy Barkhausen's criterion.

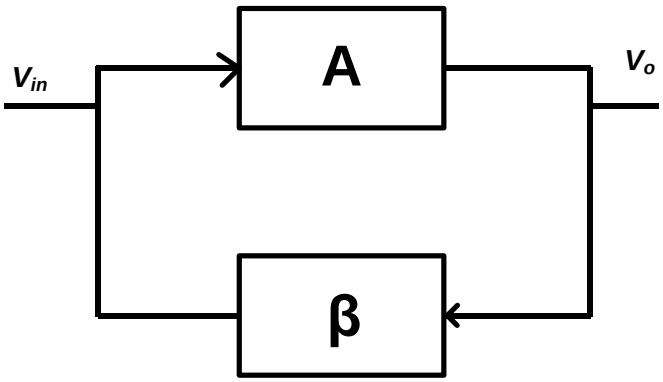


Figure 6.3 block diagram of oscillator

V_{in} =input voltage

V_o =output voltage

A = forward path gain

β = small fraction of output signal is feedback to input

- From the diagram we can conclude that, feedback voltage $(V_f) = \beta A V_{in}$
- Barkhausen's criterion states that,
  The loop gain is equal to unity in absolute magnitude, that is, $|\beta A| = 1$

1. $|\boldsymbol{\beta A}| > 1$**:** In this condition, feedback is greater than the input voltage Thus addition of input wave and feedback wave will result in larger amplitude wave and as oscillation goes on the amplitude will increase and this can be harmful for device.
2. $|\boldsymbol{\beta A}| < 1$: In this condition, feedback is less than the input voltage Thus addition of input wave and feedback wave will result in smaller amplitude wave and as oscillation goes on the amplitude will gradually decrease and oscillations will die out.
3. $|\boldsymbol{\beta A}| = 1$**:** In this condition, feedback equal to the input voltage Thus addition of input wave and feedback wave will result wave having amplitude of input and as

oscillation goes on the amplitude will remain constant and hence a sustained oscillation is achieved.

- The phase shift around the loop is zero or an integer multiple of 2π.
  $\angle\beta A = 2\pi n, n \in 0,1,2.....$ Complex value of βA is given by

  $\beta A = 1 + j0$.....(6.10)

- In above expression imaginary part is zero because we assume phase shift zero or 360º now if phase shift isn't zero then $|\beta A| \neq 1$, which is not suitable condition for oscillation. For phase shift equal to 180º $|\beta A| = 1$ but input and feedback signal will be out of phase and they will cancel each other hence phase shift must be an integer multiple of 2π.

6.3.2 Conditions

- ❖ The oscillator must provide a large voltage gain to satisfy Barkhausen criteria in order to start oscillation.
- ❖ The total phase shift must be -180 degrees.

6.3.3 Choosing the configuration

Common source stage: When the source terminal of an MOS amplifier is common for both input and output, then the configuration is known as common source configuration. A common source configuration provides an output of -180 phase shift with a gain of $-g_m R_D$ where R_D is the drain resistance at the output terminal.

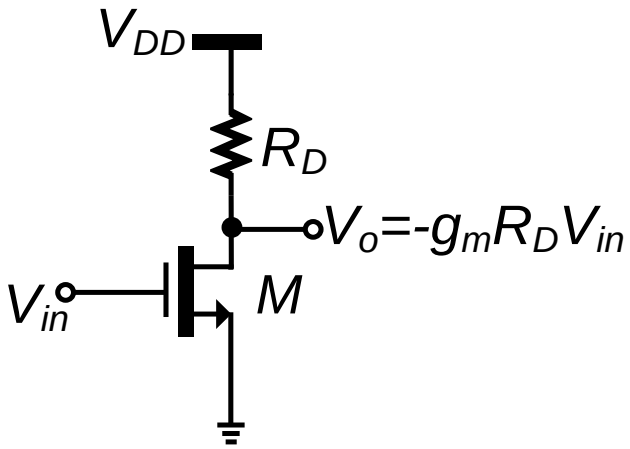


Figure 6.4: Common source amplifier

The gain of the common source stage is given by A_v=-$g_m R_D$. So now neglecting the capacitances of the transistor, the voltage gain of the common-source amplification stage with a lossy LC tank load at the resonant frequency of the LC tank is given by A_v=-$g_m R_p$, where R_p is the parallel resistance of the tank. Now a phase delay of -180 is not practically possible, so two back to back common source amplifiers are required to provide the large phase shift. This back to back configuration, also called cross coupled transistor pair will act as negative resistor to provide large voltage gain by outperforming the ohmic loss of the LC tank.

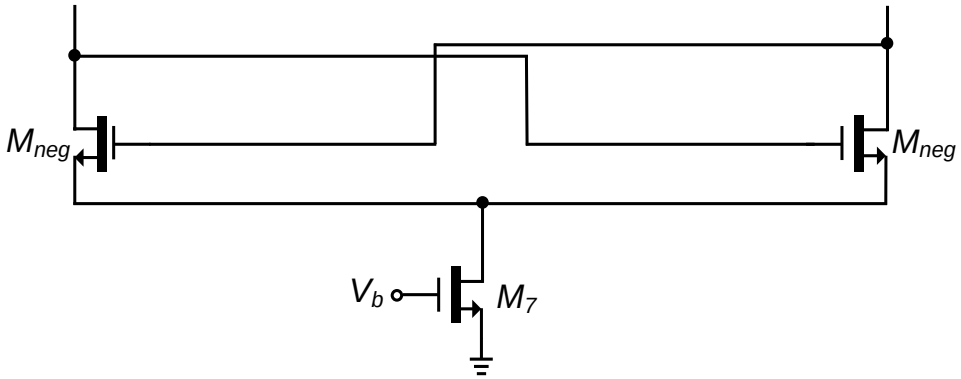


Figure 6.5: Cross coupled transistor pair

Here M_7 is operated in saturation region which will act as current source for biasing the cross-coupled transistor pair to control the g_m.

6.3.4 Choosing W/L ratios and applied voltages

M_{neg}: As the voltage gain of the oscillator must be sufficiently large and the voltage gain of the common source stage is $-g_m R_D$ so W/L ratio needs to be chosen in such a way that the g_m is in its maximum value. The maximum width is 30µm in 90nm CMOS process and the minimum channel length is 100nm (though it is 90nm, but Virtuoso Cadence does not allow to use 90nm rather it offers to use a minimum of 100nm). So the W/L ratio for the $\boldsymbol{M_{neg}}$ is 30µm/100nm to achieve maximum gm. But the higher value of W/L or g_m has also a disadvantage. It increases the power consumed by the MOSFETs which reduces the output oscillation's amplitude as well as the output power.

M_7: M_7 is used as biasing current source for controlling the resistance of the cross-coupled transistors. The more the W/L ratio for M_7 the more the value of I_{ds} as well as g_m . The higher value of I_{ds} will cause the higher value of gm for the M_{neg}. As g_m for M_{neg} has already been increased to its maximum value, so an optimum value of 30µm/100nm has been chosen with a multipliers of 3 for M_7.

M_{cap}: The MOS capacitors (M_{cap}) with a dc voltage source are employed to vary the oscillation frequency of the designed VCO. MOS with shorted drain and source terminal acts as capacitor which can be used as variable capacitor called MOS varactor . Here W/L ratio for the M_{cap} is 120nm/10µm with a multipliers of 15 and it provides a capacitance of 18.096fF.

Supply voltage, biasing voltage and control voltage: Supply voltage V_{DD}=1.8 V is used. A biasing voltage of V_b=0.5 V is used to operate the MOS which acts as current source in saturation voltage. $V_{control}$=0V to 0.8V is used to tune the capacitances of the M_{cap} as well as the oscillation frequency.

Table 6.2 summarizes the VCO's network

Table 6.2: Summary of W/L ratios & applied voltages used in proposed VCO's network

MOS	Width(µm)	Length(nm)
$\mathbf{M_1}$	27	200
$\mathbf{M_2}$	15	100
$\mathbf{M_3}$	30	350
$\mathbf{M_4}$	10	200
$\mathbf{M_5}$	22	200
$\mathbf{M_6}$	5	200
$\mathbf{M_7}$	30	300 (multipliers=3)
$\mathbf{M_{neg}}$	30	100
$\mathbf{M_{cap}}$	0.120	10 μm(multipliers=15)
Supply voltage ,V_{DD}=1 V		
Biasing voltage V_b=0.5 V		
Control voltage, $V_{control}$=0 to 0.8 V		

The next section illustrates the schematic representation of the proposed active inductor based VCO . The dotted lines represents the active inductor's section, M_{neg}s are cross coupled transistor pair. M_{cap}s are MOS capacitors and M_7 at the tail of the network works as biasing current sources for M_{neg}.

6.4 Schematic Representation of Proposed Active Inductor Based VCO

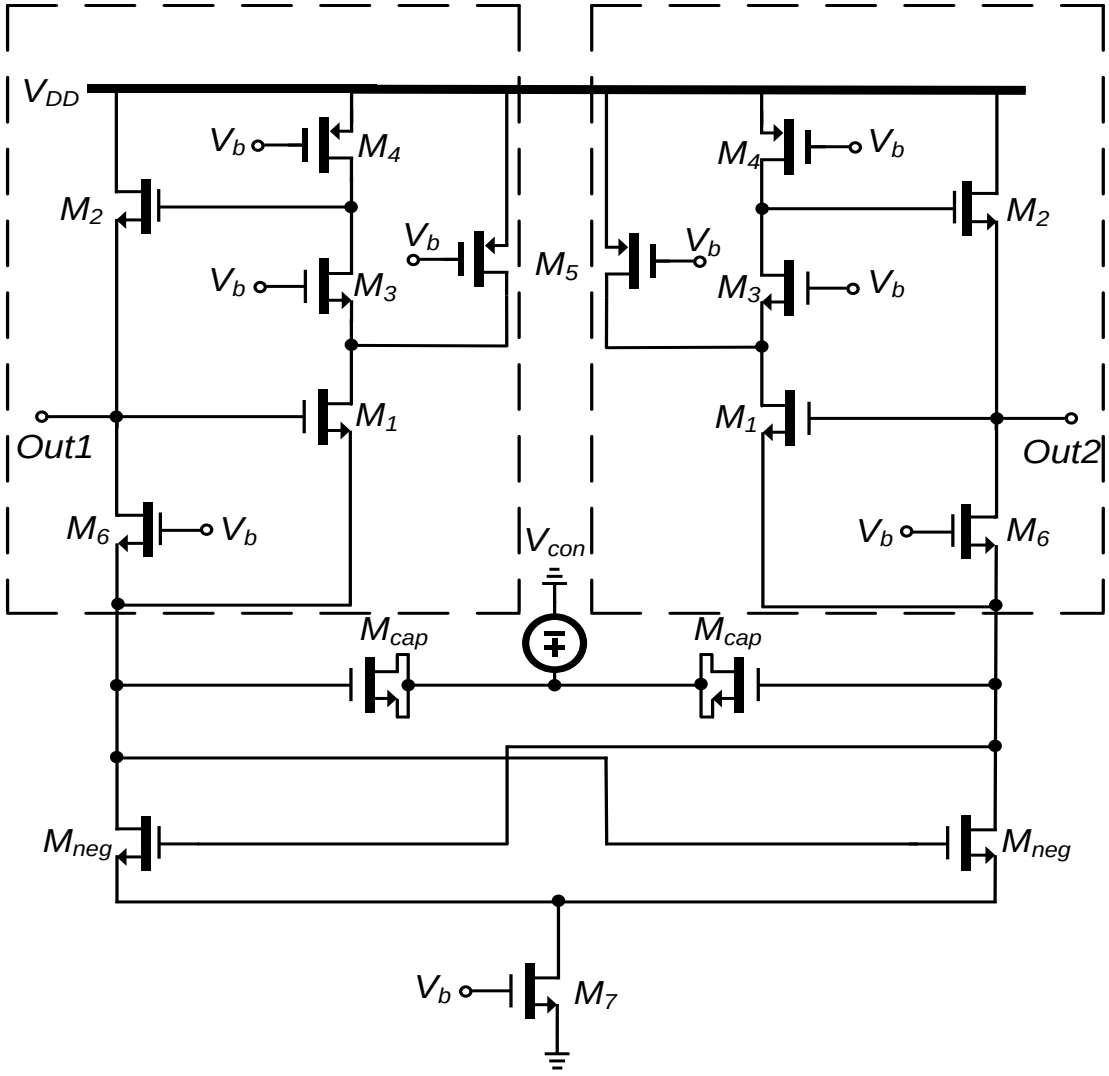


Figure 6.6: Proposed Active Inductor based VCO

CHAPTER 07

SIMULATION RESULTS

7.1 Comparative Analysis of Active Inductors

7.1.1 Simulation

To compare the performance of different active inductor topologies, simulations have been performed in Cadence 6.16 environment using the 90 nm CMOS technology. In simulations, channel length of all NMOS and PMOS transistors are set at 200 nm and the width of NMOS and PMOS are set at 10μm and 20μm respectively. The s- parameter simulation has been performed to obtain the inductance and quality factor of the investigated models of active inductor. The s-parameter simulation has been accomplished with an ac source in series with a resistance of 50 ohm and a capacitor of 100pF for dc isolation. For less-lossy active inductors, the ideal current source of 300μA has been used. NMOS at the V_{DD} to input terminal (according to maximum Q factor based on gyrator-C network) has width of 30μm and length of 200nm. V_{DD}=1.8V has been used as supply voltage.

7.1.2 Comparison of different models

The comparison has been done based on different parameters like quality factor, inductance, power consumption and self-resonant frequency. Figure 7.1 & 7.2 shows the variation of Q factor for different models where figure 7.3 & 7.4 shows the variation of inductance.

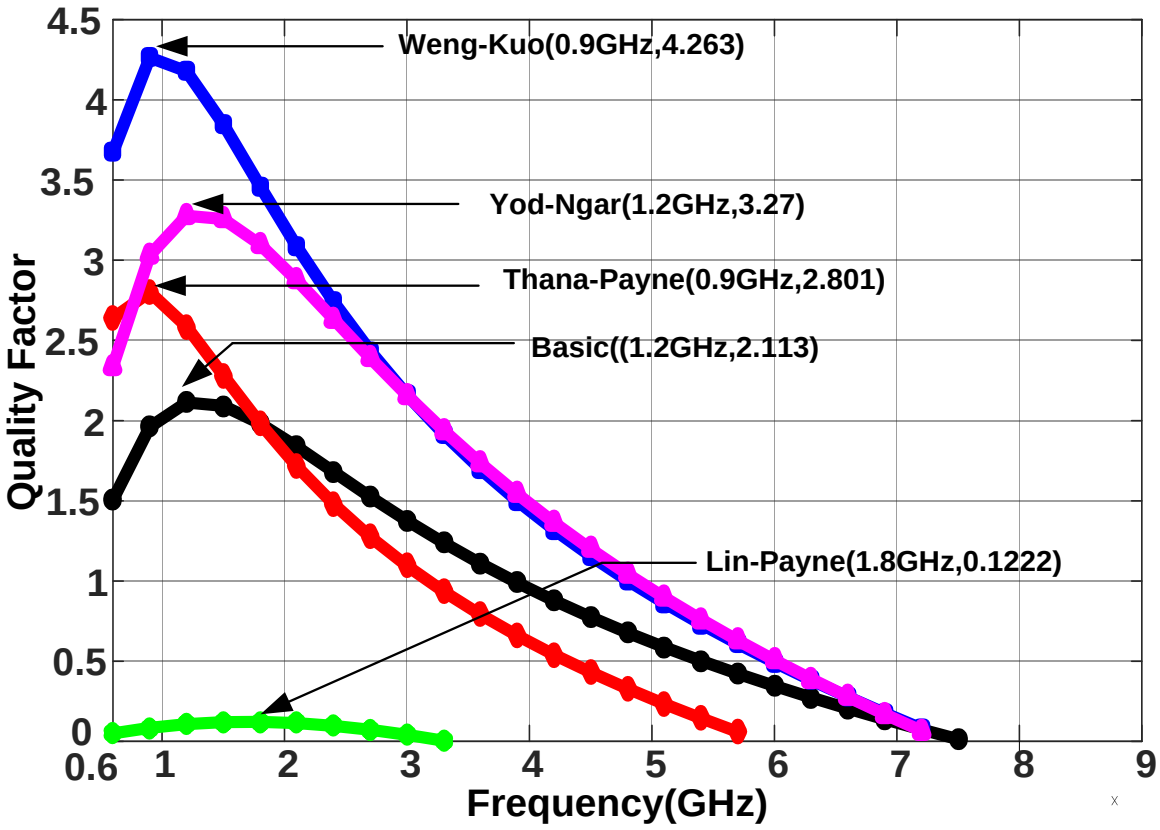


Figure 7.1: Variation of quality factor with frequency for different models with constant current source

In figure 7.1 and 7.2 stated above, it is comprehensively noticed that quality factor has increased linearly at low frequency and reached to maximum level .But after attaining maximum value, the factor has started to decrease owing to finite output impedance and the self-resonant of the inductor. The quality factor is annihilated at the point when the frequency is proceeded the cut off or self-resonant frequency of the inductor. That means the quality factor becomes zero at that point.

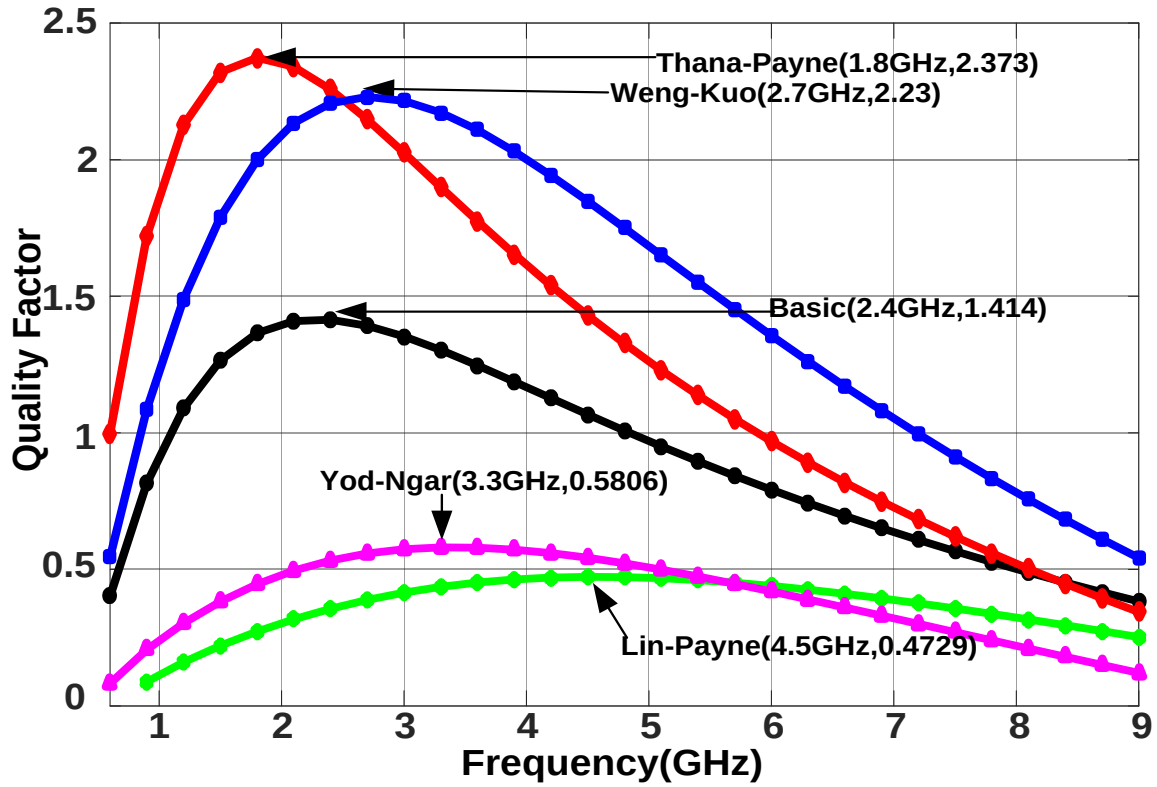


Figure 7.2: Variation of quality factor with frequency for different models with saturated MOS as current source.

After exceeding the self-resonant frequency or cut off frequency, the Q factor becomes negative as the inductance of the inductor becomes negative. The negative inductance refers that the inductor will act as capacitor which is not desirable. So, the higher cut off frequency/ self-resonant frequency depicts the better performance of the inductor.

In figure 7.1, constant current sources have been employed for biasing. As a result, the net emerged loss from the parasitic resistance is less due to absence of the transistor as the transistor contributes to loss from its resistance. On the contrary, in figure 7.2, emerged loss from parasitic resistance increases on account of inserting MOS device which degrades the quality factor. Inspite of this drawback, the insertion of MOS enhances the frequency range as well as inductance.

Yodprasit-Ngarmnil introduced parallel negative resistance for enhancing the Q factor which reduces parallel parasitic resistance of active inductors. Nevertheless employing MOS as current source in circuitry does not affect significantly since quality factor appears for this is 0.5806 which is much lower comparing to others. The self-resonant frequency increases from 7.40 GHZ to 10.294 GHz due to insertion of MOS but the degradation of the Q factor from 3.142 to 0.5806. On the other hand, in case of using constant current source the quality factor

improves but not capable of exceeding the outcome of Weng-Kuo. In addition, the power consumption is greater than Weng-kuo.

Lin- Payne active inductor which substitutes ideal current source with saturated MOS, maximizes the frequency range with low voltage headroom. It exhibits a self-resonant frequency of 3.332 GHz and 12.317 GHz. but the power consumption (14.35mW) is greater than the others while the quality factor is very low for both cases.

Weng-Kuo active inductor is the modified version of Thanachynont-Payne. But both have unique property of enhancing the frequency range by a cascaded MOS. But Weng-Kuo offers wider frequency range than Thanachynont-Payne which are 7.5 GHz and 11.87 GHz. In addition, Weng-Kuo is preferable than other models having the property of tunability of the quality factor and inductance independently which have been made possible after introducing an additional current source in the circuitry. Though the power consumption of this active inductor is more than Thanachynont-Payne (1.08 mW and 8.38 mW) and quantity is 10.71 mW due to the additional current source, it is highly advantageous with increased quality factor with the numerical values of 4.263 and 2.373.

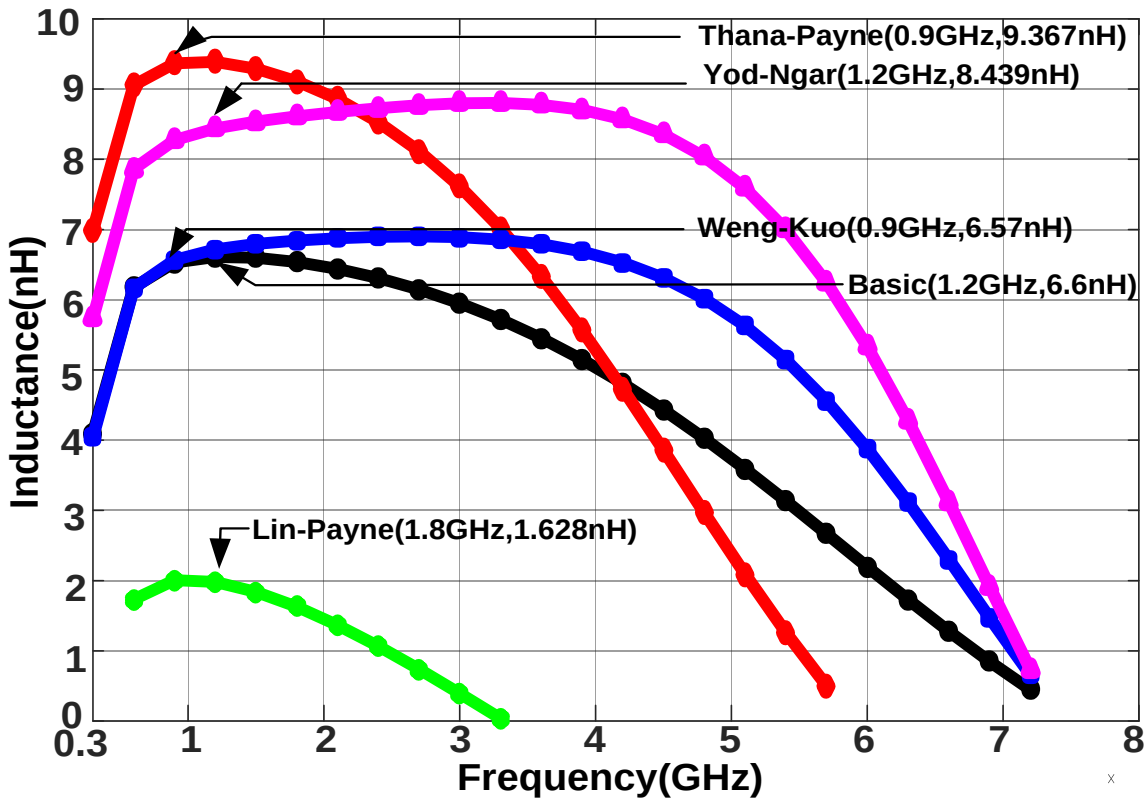


Figure 7.3: Variation of inductance with frequency for different models with constant current source.

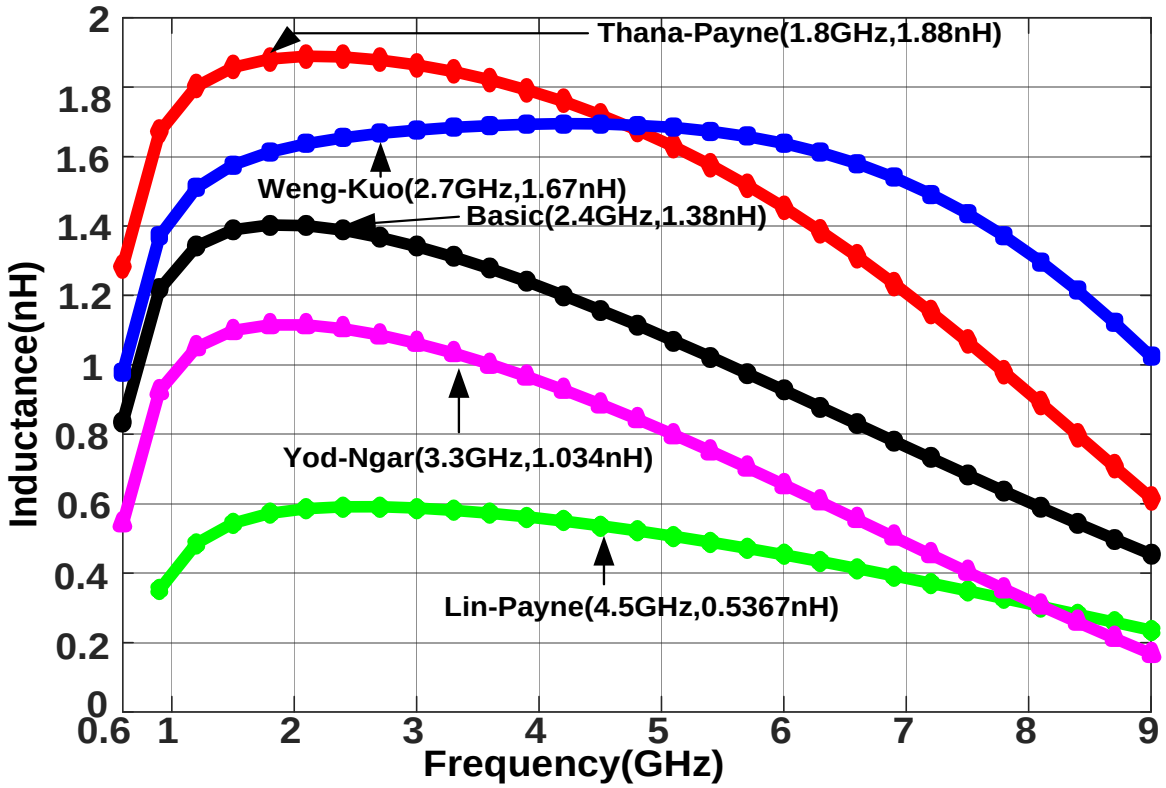


Figure 7.4: Variation of inductance with frequency for different models with saturated MOS as current source.

Figure 7.3 and 7.4 depicts the variation of inductance with frequency for the selected models. Figure 7.3 represents the case where ideal current sources are employed for biasing where figure 7.4 represents the fact where saturated MOSs in case of substituting the ideal current source with saturated MOS. If concentration is given on the graph of the inductance, it can be observed primarily that the inductance increases and after attaining a maximum value the inductance starts decreasing. After self-resonant frequency the inductance becomes negative which indicates that the inductor acts as capacitor that is not desirable. For using ideal current source, the peak inductance for all the inductors occurs at lower frequency. But after substituting current source with saturated MOS, the peak inductive frequency as well as the frequency range at which the inductor shows inductive properties increases though the parasitic loss evolves due to insertion of MOS.

Table 7.1and table 7.2 summarize the simulation results.

Table 7.1: Active inductors with constant current source

	Basic Gyrator-C	Yodprasit/ Ngarmnil	Lin/Payne	Thanachayaont/ Payne	Weng/ Kuo
Quality Factor	2.112 @1.2GHz	3.142 @1.2GHz	.1222 @1.8 GHz	2.801 @0.9GHz	4.263 @0.9GHz
Inductance (nH)	6.6 @1.2 GHz	8.439 @1.2GHz	1.628 @1.8GHz	9.367 @0.9GHz	6.57nH @0.9GHz
Power (mW)	1.08	2.34	1.08	1.08	1.62mW
f_0 **(GHz)**	7.57	7.40	3.332	5.923	7.462 GHz

Table 7.2: Active inductors with saturated MOS as current source

	Basic Gyrator-C	Yodprasit/ Ngarmnil	Lin/Payne	Thanachayanont/ Payne	Weng /Kuo
Quality Factor	1.414 @2.4GHz	0.5806 @3.3GHz	0.4729 @4.5GHz	2.373 @1.8GHz	2.23 @2.7GHz
Inductance (nH)	1.38 @2.4GHz	1.034 @3.3GHz	0.5367 @4.5GHz	1.88 @1.8GHz	1.67 @3GHz
Power (mW)	8.18	12.6	14.35	8.38	10.63
f_0 **(GHz)**	13.177	10.294	12.317	11.362	11.868

So focusing on the Weng-Kuo, the following properties can be found

Table 7.3: Performance parameters for Weng/Kuo active inductor

Parameters	Inductor with Constant Current source	Inductor with saturated MOS Current source	Comment
Maximum Q factor	4.263 @0.9GHz	2.23 @2.7GHz	Good and greater than others
Inductance @ Q	6.57nH @0.9GHz	1.67 @3GHz	--------
Power Consumption	1.62 mW	10.63 mW	Increased Due to an Additional Current Source but less than Yod-Ngar and Lin-Payne
Self-resonant frequency	7.462 GHz	11.868	Wide frequency range
Special property	Tunability of Inductance and Q factor independently		

7.2 Oscillator

Figure 7.5 represents the proposed active inductor based VCO where the dotted section points out the single ended active inductor (M_1 –M_6) forming the differential configuration. The cross coupled pair of MOS (M_{neg}) is used to provide negative resistance to start oscillation with a large voltage gain. A MOS (M_7) current source is used to regulate the resistance of the cross coupled MOS transistors. MOS M_{cap} along with the control voltage source $V_{control}$ is used to tune the oscillation frequency of the oscillator.

7.2.1 Simulation

Simulations of active inductors and proposed VCO have been performed via Cadence 6.16 environment using the 90 nm CMOS technology.

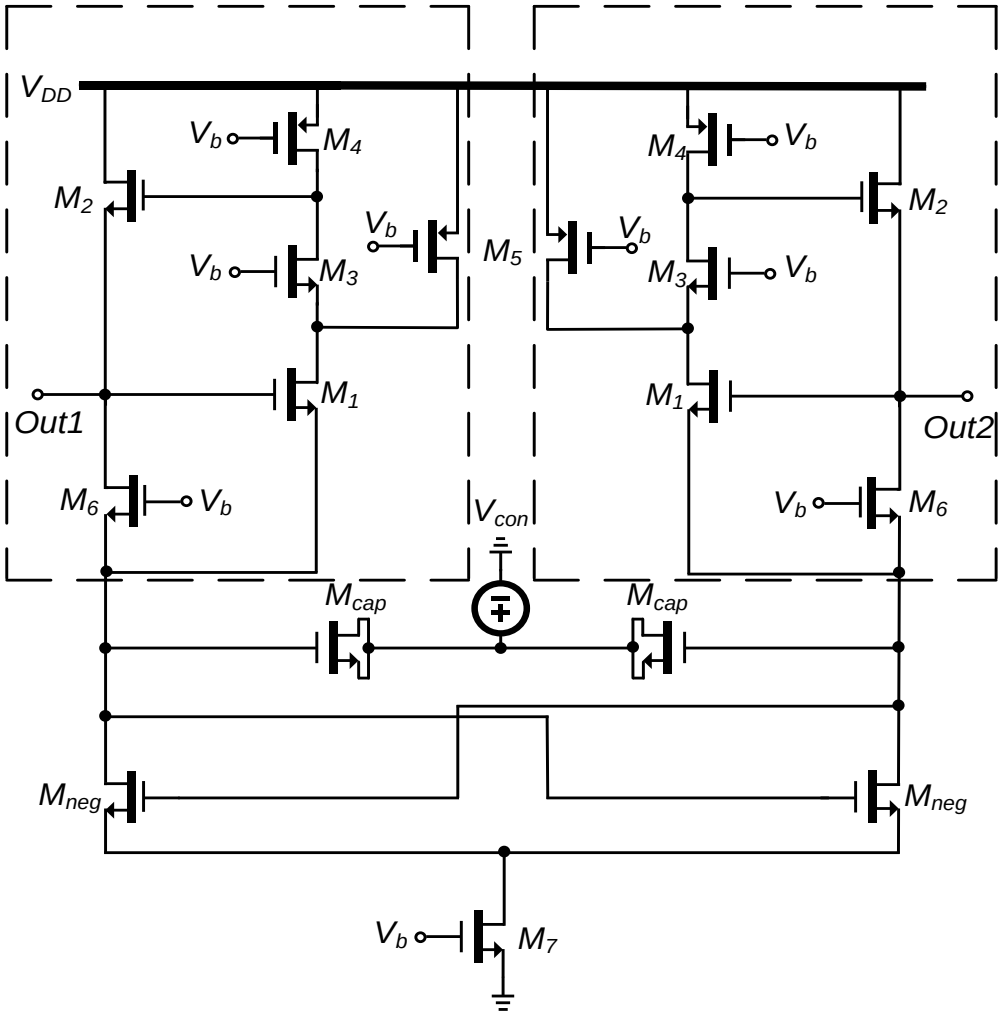


Figure 7.5: Proposed active inductor based VCO

7.2.2 Active Inductor simulation & performance analysis

The s parameter simulation was performed along with an ac source , a resistor of 50 ohm in series with capacitor of 100pF for dc isolation. The Q factor ranges from 12.3 (2.17 GHz) to 405(2.72GHz) within the frequency range achieving a value of 22.59 at 2.4 GHz which is eventually feasible for Bluetooth applications. In addition, the inductive range is (4.3 ~ 5.1)nH and 4.65 nH@ 2.4GHz. The quality factor of the active inductor is quite satisfactory within the frequency range for the designed VCO which indicates lower loss of energy. The plots given below depict the characteristics of the inductor such as quality factor, inductance and impedance.

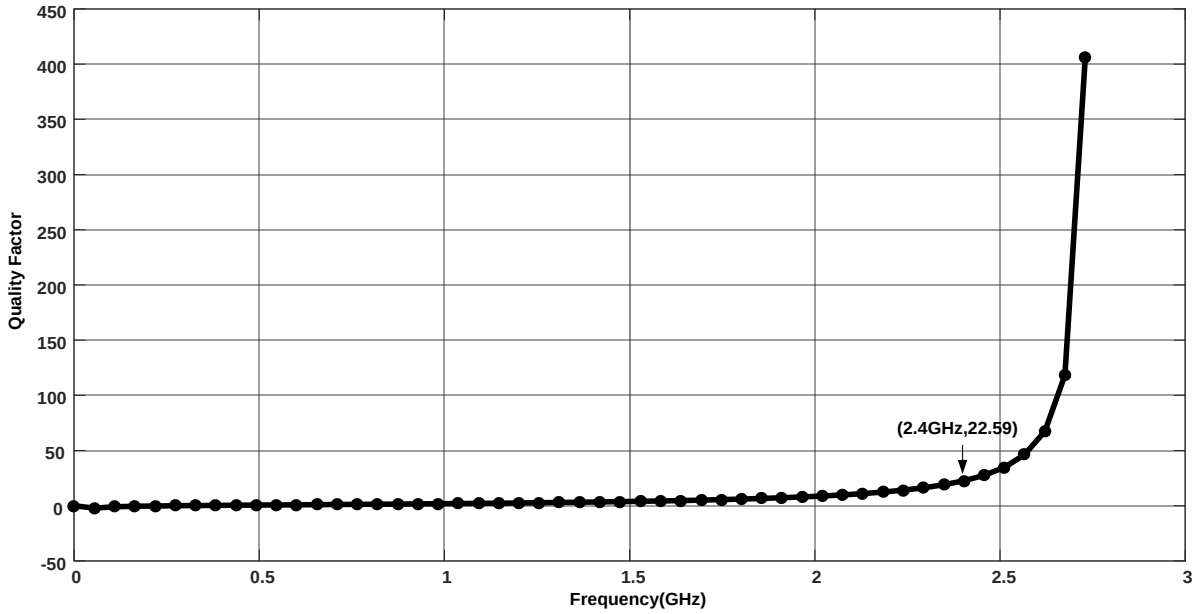


Figure 7.6: Quality factor vs frequency of inductor within the frequency range of VCO

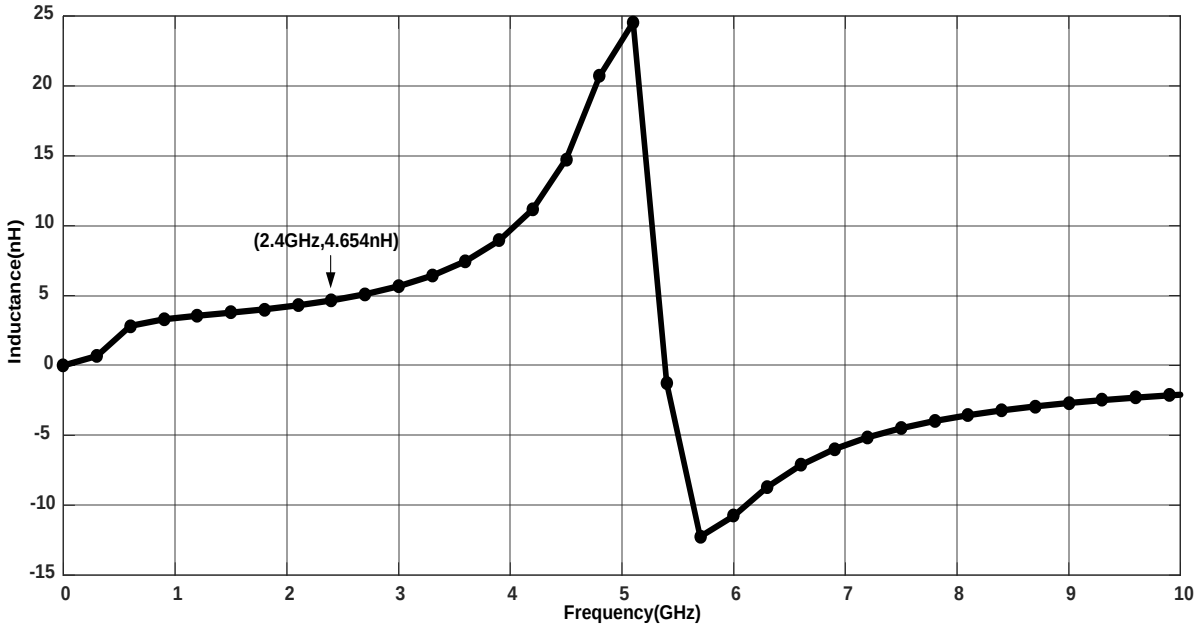


Figure 7.7: Inductance vs frequency of inductor within the frequency range of VCO

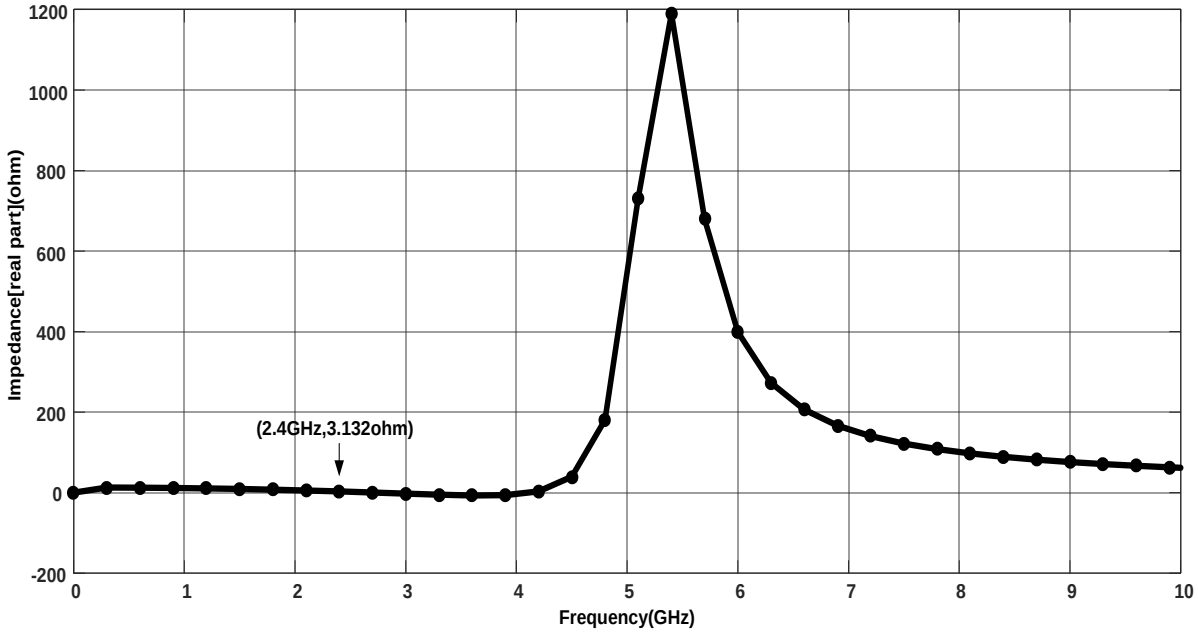


Figure 7.8: Impedance(real) vs Frequency of inductor for the designed VCO

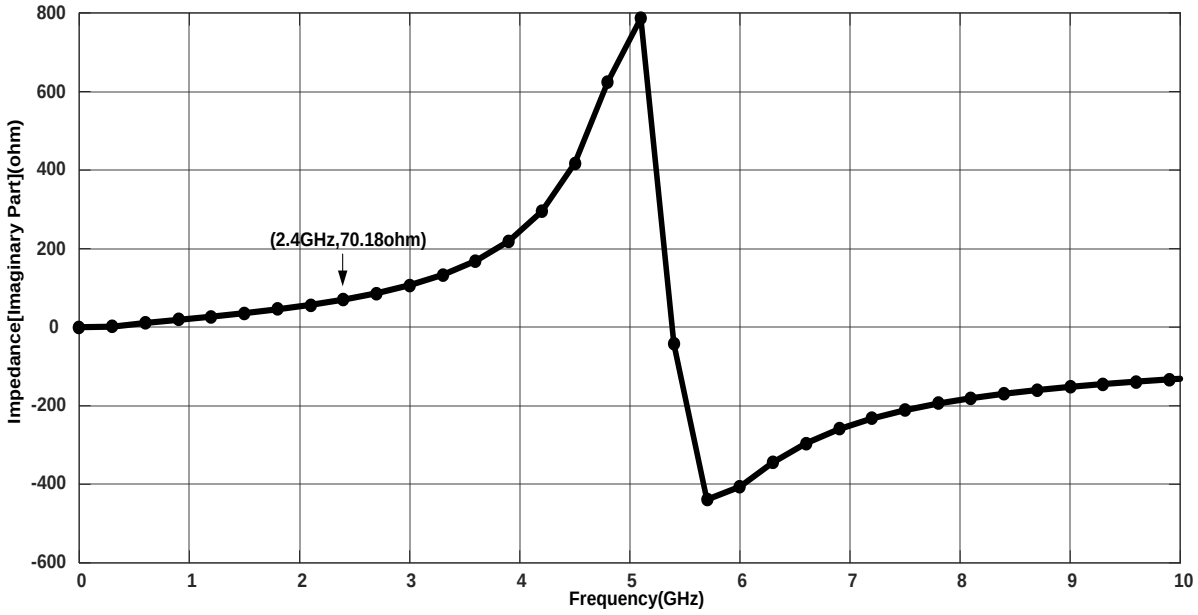


Figure 7.9: Impedance(imaginary) vs Frequency of inductor for the designed VCO

7.2.3 VCO simulation & performance analysis

For obtaining sinusoidal oscillation and determining the performance parameter, transient analysis , pss and pnoise with 5 harmonics have been performed.

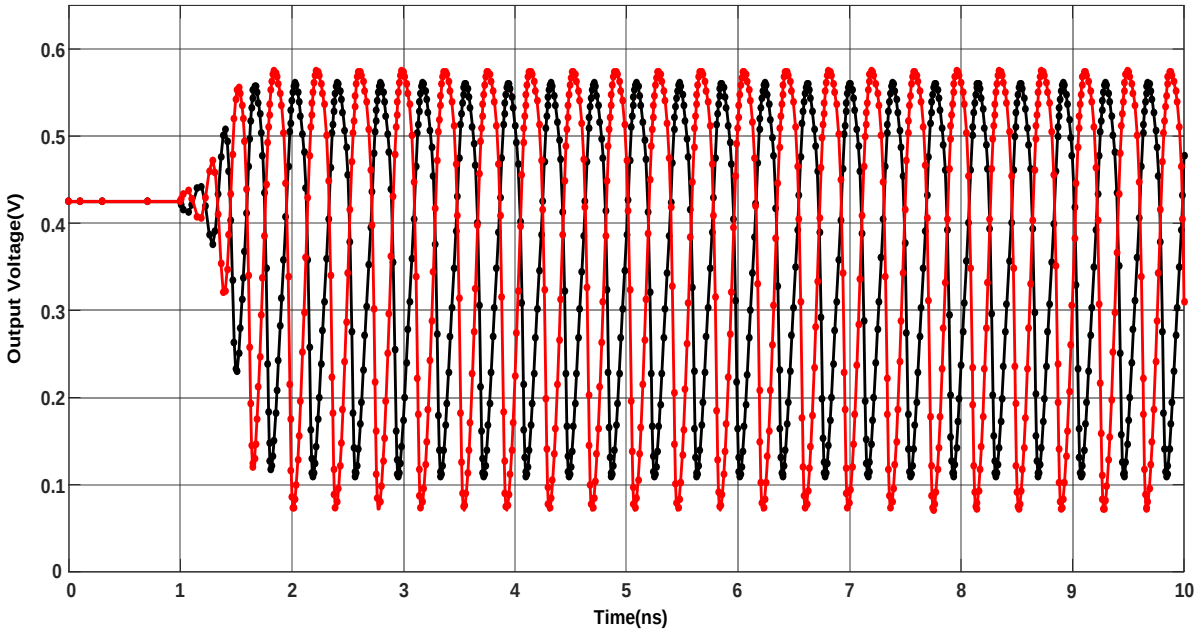


Figure 7.10: Voltage at Out1 and nOut2 vs time

Figure 7.10 demonstrates the differential output voltage of the oscillator while figure 7.11 & 7.12 depicts the phase noise performance at the specified frequency offset.

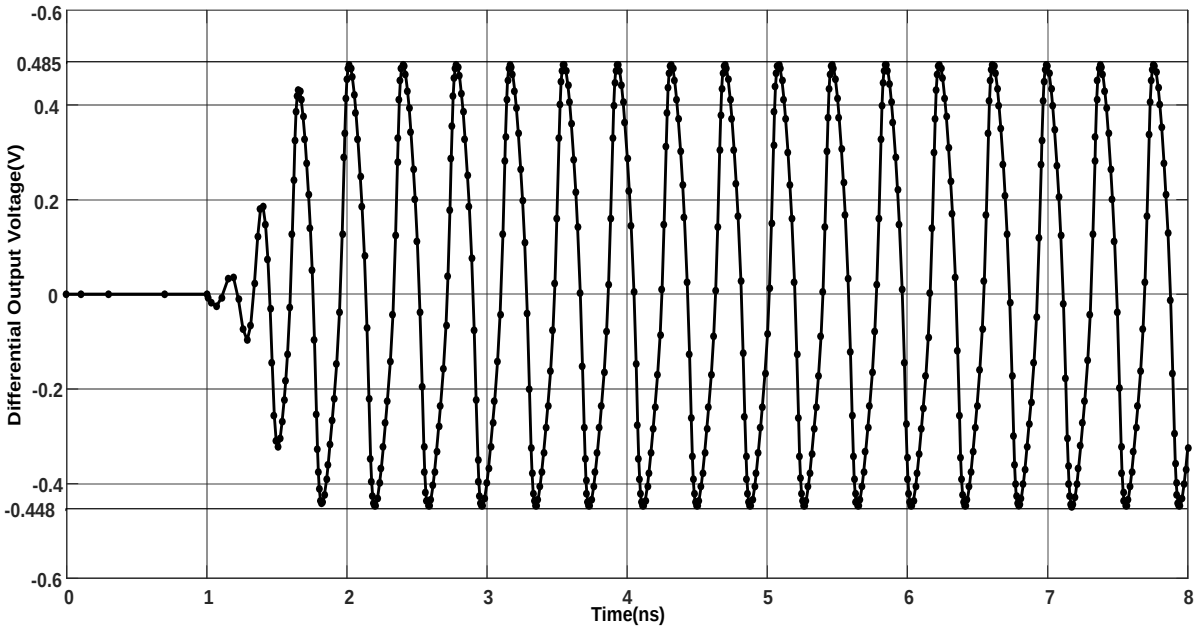


Figure 7.11: Differential output oscillation vs time

The oscillator yields a differential output of 0.48 to -0.448 mV @ 2.4GHz and a tuning range of 2.17 GHz to 2.72GHz with a variation of control voltage of 0 to 0.8 V. For $V_{control}$ =0.4V,

the frequency is 2.40887 GHz with a phase noise of -82.34 dBc/Hz@1MHz offset. The power consumption is 4.18761 mW. A parameter called figure of Merit (FOM) is introduced to characterize the performance of the VCO.

$$FOM = L(\Delta\omega) + 10lo\,g\left(\frac{powerDC}{1mW}\right) - 20log(\frac{\omega_o}{\Delta\omega})$$

Where ω_0 represents the oscillation frequency, $\Delta\omega$ is the offset frequency from the central carrier frequency. $L\Delta(\omega)$ is the phase noise at specified offset. DC power dissipation is powerDC. FOM can likewise be depicted in dBF as

$$FOM(dBF) = 20\ log(freq) - phase\ noise - 10log(powerDC)$$

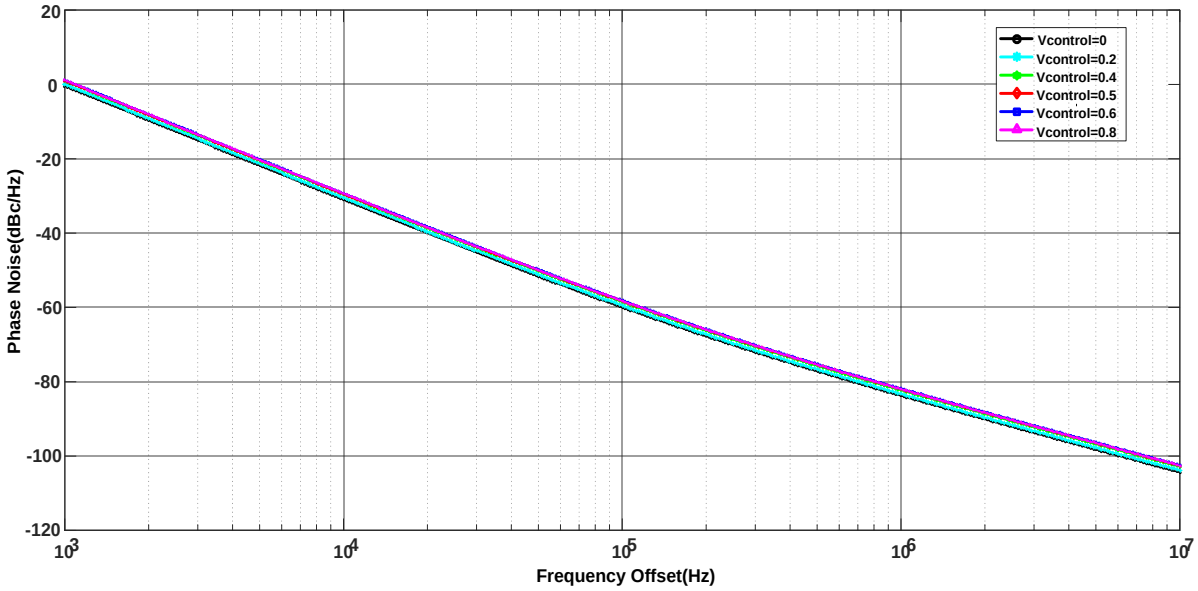


Figure 7.12: Phase noise vs frequency offset

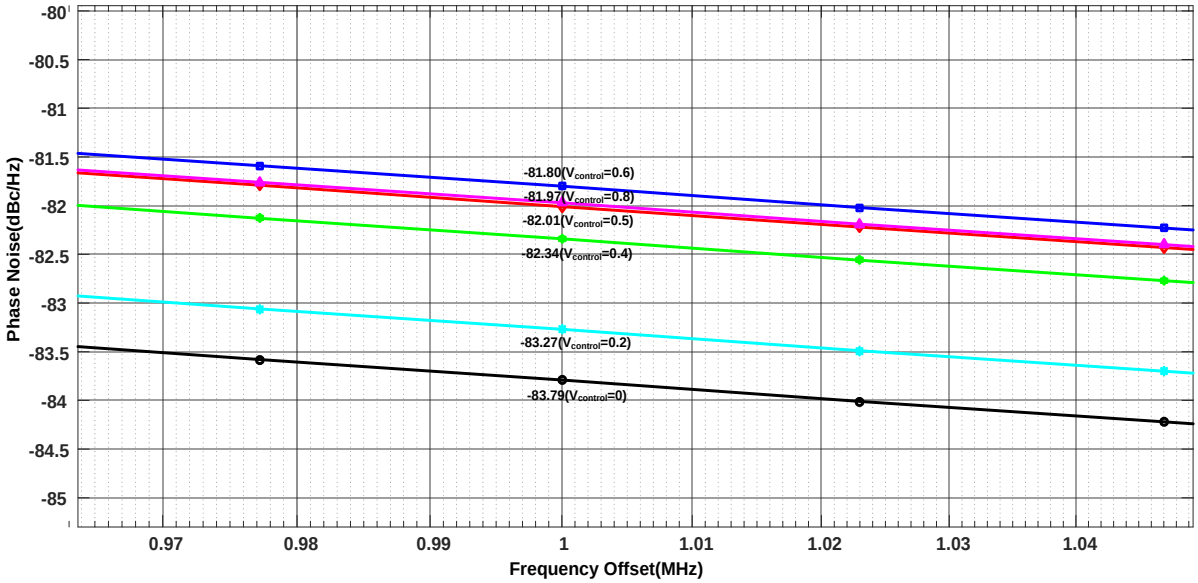


Figure 7.13: Zoomed view of phase noise vs frequency offset

Table 7.4: Performance parameters of VCO for different $V_{control}$

V_{con} (V)	Freq. (f) GHz (PSS)	Differ-ential Output (P-P) mV	Voltage (PSS) mV@f	Phase Noise @1Mz offset dBc/Hz	Power Diss. @1V (mW)	Differ-ential Output Power (50ohm R) @f (dBm)	Figure of merit (FOM)	
							@ 1MHz Offset	dBF
0	2.17115	450 to -420	405	-83.79	4.18761	2.158	-144.3	294.3
0.2	2.2019	470 to -436	416.1	-83.27	4.18761	2.384	-143.9	293.9
0.4	2.40887	483 to -447	450.5	-82.34	4.18761	3.073	-143.4	293.4
0.5	2.60495	485 to -448	458.5	-82.01	4.18761	3.227	-143.9	294.1
0.6	2.7216	483 to -447	457.9	-81.80	4.18761	3.227	-144.3	294.3
0.8	2.7214	481 to -446	455.1	-81.97	4.18761	3.162	-144.4	294.4

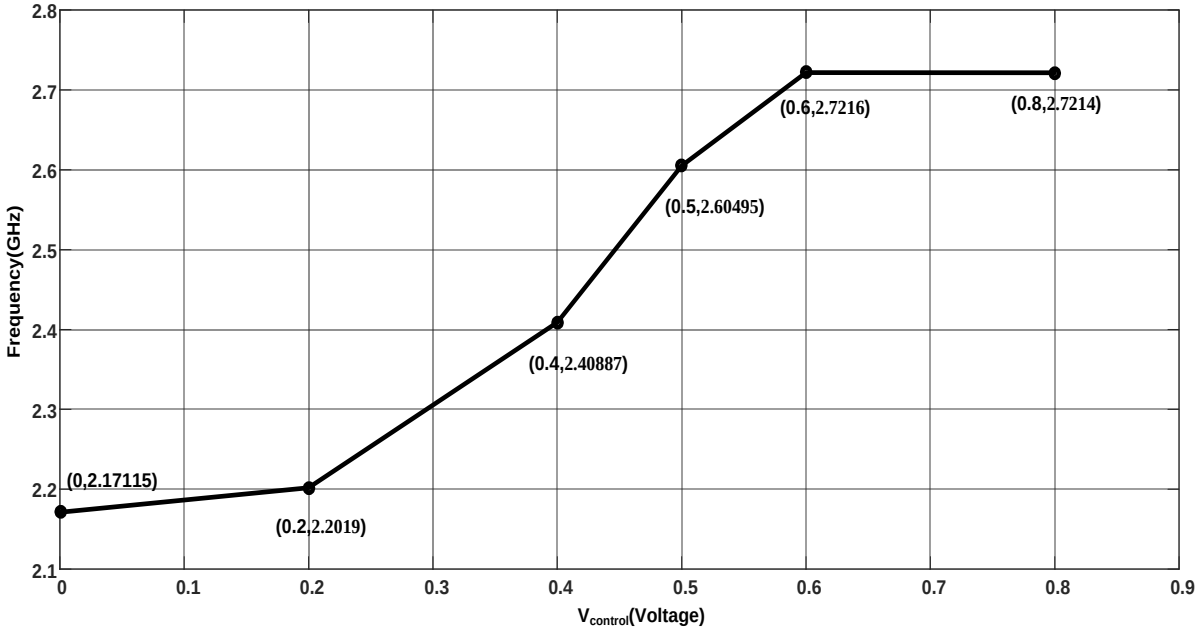


Figure 7.14: Frequency vs $V_{control}$ of VCO

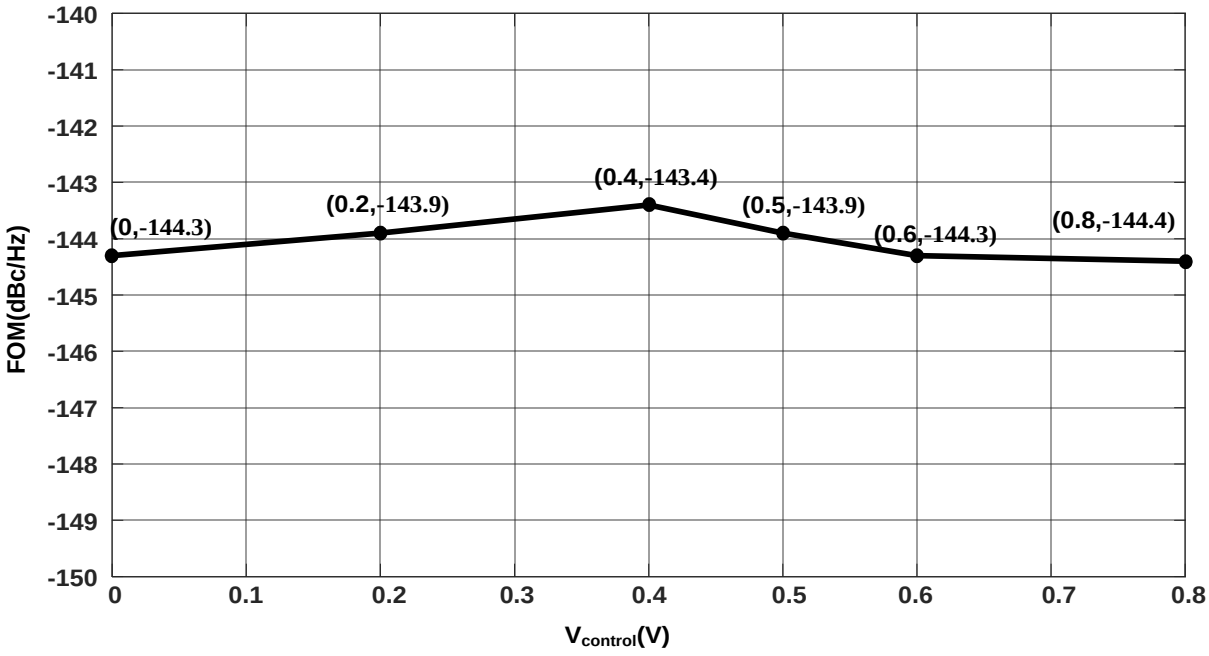


Figure 7.15: Figure of Merit(FOM) vs tuning voltage $V_{control}$

Table 7.3 shows the performance of the designed VCO at different tuning voltages ranging from 0V to 0.8V. The VCO yields a stable oscillation voltage along with a high output power which are the exceptional highlights of the VCO. Figure 7.14 depicts frequency at different control voltages while figure 7.15 represents the variation of FOM of the VCO. The frequency range includes the Bluetooth operating frequency and the low variety of FOM demonstrates the stability of the performance of the VCO.

Table 7.5: Performance summary of VCO

Parameters	This Work	
Technology	90nm	
Supply Voltage(V_{DD})	1 Volt	
Power Consumption	1Volt	4.18761mA
	4.18761mW	
Frequency Range	2.17115GHz to 2.7214GHz and 22.49%	
Phase Noise	-82.34 dBc/Hz @ 2.4GHz @ 1 MHz offset	
Figure of Merit @ 1MHz offset and 2.4 GHz	-143.7203	
Figure of Merit (dBF)	293.7246	
Output Power(dBm)	2.158 to 3.162 3.073 @ 2.4 GHz	

7.3 Performance comparison

Table 7.6: Performance comparison of VCO with other works

Parameters	[56]	[57]	[58]	This work
Technology	180nm CMOS	180nm CMOS	180nm CMOS	90nm CMOS
Supply Voltage,V_{DD}(V)	1.8	1.8	1.8	1
Power Consumption (mW)	29.38	44.6	13.8	4.18761
Frequency Range(GHz)	-	1.26 to 2.98	0.5-2	2.17115 to 2.7214
Frequency Range(%)	-	81.13	120	22.49
Output Power	0.211 @ 5.5GHz	-5.3 to -18.7	-29 to 20.8	2.158 to 3.162 (Differential)
Phase Noise @ 1 MHz offset (dBc/Hz)	-80.314	-90	-78 to -90	-82.34
Figure of Merit @1MHz offset	-140.433 @ ω_o =5.5GHz	-141.11 @ ω_o =2.4 GHz	-120.58 to -144.602 (0.5 GHz to 2GHz)	-143.7203 @ ω_o= 2.4 GHz

Table 7.5 shows the performance comparison of the proposed Weng-Kuo active inductor based VCO with referring active LC oscillators. The VCO has consumed low power and higher figure of merit (FOM) which outperforms the other cited designed VCOs. It also yields high differential output power with a tuning scope of 22.49%.

Table 7.7: Remarks on the performance characteristics of VCO

Parameters	This Work	Comment
Technology	90nm	
Supply Voltage(V_{DD})	1 Volt	Low supply voltage
Power consumption and variation with frequency	4.18761mW	Less and constant
Frequency Range	2.17115GHz to 2.7214GHz 22.49%	Covers Bluetooth range
Phase Noise variation	-83.79 to -81.97 dBc/Hz	Very Less variation
Oscillation Voltage Variation after 2.4GHz (Peak)	450mV to 458mV	Less Variation
Variation of Figure of Merit @1MHz offset	-143.4 to -144.4 (dBc/Hz)	Very Less and Constant
Output Power (dBm)	2.158 to 3.162 3.073 @ 2.4 GHz	High output power

CHAPTER 08

CONCLUSION

8.1 Analytical Observation

At the very beginning of our research, we focused on simulation and comparative analysis of different active inductor models based on gyrator C which for various applications. Inductors are significant part in communication systems like Voltage controlled oscillators, RF transceivers, low noise amplifier, clock generation circuits etc and the performance of these circuitry largely depends on different parameters of inductors like tunability, quality factor, silicon area consumption etc. As a result, before using inductors in various circuitry we need to analyze with respective to the demand of the desired device. For example, if someone wish to design an Voltage controlled oscillator, an inductor with good quality factor need to be inserted for effective design. Power consumption, frequency range are also considerable parameters for practical RF applications which depend on the frequency range, power consumption of inductors .As we are concerned about frequency range, tunability and power consumption of inductors, it was very effective to work on active inductor over spiral inductor. Therefore, in this paper we emphasized on selecting better active inductor model For this purpose, our research methodology was advanced forward considering various topologies like Yodprasit-Ngarmnil Active Inductor, Lin-Payne Active Inductor, Thanachayanont-Payne Active Inductor, Weng-Kuo Cascode Active Inductor. Among these configurations, from theoretical analysis, it seemed that Weng-kuo based active inductor would show better tunability for designing voltage controlled oscillator for inserting additional current source which ensured the tunability of quality factor and inductance independently. From the simulation results, we found that the quality factor of Weng-Kuo based active inductor was much higher than the other topologies. In addition, in case of the frequency range and inductive tunability, this topology shows much higher performance. From these analysis, we decided to use Weng-kuo based active inductor for designing a VCO, For obtaining sinusoidal oscillation and determining the performance parameter, transient analysis ,pss and pnoise with 5 harmonics have been performed. The oscillator yields a differential output of 0.48 to-0.448 mV @ 2.4GHz and a tuning range of 2.17 GHz to 2.72GHz with a variation of control voltage of 0 to .8 V. For $V_{control}$ =0.4V, the frequency is 2.40887 GHz with a phase noise of -82.34 dBc/Hz@1MHz offset. The power consumption is 4.18761 mW. The oscillator provides a very high differential power output ranging from 2.158 to 3.162 dBm and figure of merit is 143.4dBc/Hz. In our research, we performed comparison between different voltage controlled oscillators which was convincing to decide

our designed VCO superior to other ones due to low power consumption and suitable frequency range for Bluetooth applications. The performance stability of this high power oscillator makes it suitable various RF applications.

8.2 Frequency Range

The oscillator yields a tuning range of 2.17 GHz to 2.72GHz with a variation of control voltage of 0 to 0.8 V

8.2.1 Applications

- **Bluetooth Application:** Bluetooth devices intended for use in short-range personal area networks operate from 2.4 to 2.4835 GHz. To reduce interference with other protocols that use the 2.45 GHz band, the Bluetooth protocol divides the band into 79 channels (each 1 MHz wide) and changes channels up to 1600 times per second. Newer Bluetooth versions also feature *Adaptive Frequency Hopping* which attempts to detect existing signals in the ISM band, such as Wi-Fi channels, and avoid them by negotiating a channel map between the communicating Bluetooth devices.

  The USB 3.0 computer cable standard has been proven to generate significant amounts of Electromagnetic interference that can interfere with any Bluetooth devices a user has connected to the same computer. Various strategies can be applied to resolve the problem, ranging from simple solutions such as increasing the distance of USB 3.0 devices from any Bluetooth devices to purchasing better shielded USB cables.
- **ZigBee/IEEE Data Networks:** Many ZigBee / IEEE 802.15.4-based wireless data networks operate in the 2.4–2.4835 GHz band, and so are subject to interference from other devices operating in that same band. To avoid interference from IEEE 802.11 networks, an IEEE 802.15.4 network can be configured to only use channels 15, 20, 25, and 26, avoiding frequencies used by the commonly used IEEE 802.11 channels 1, 6, and 11.

- **Video devices:** Video senders typically operate using an FM carrier to carry a video signal from one room to another (for example, satellite TV or closed-circuit

television). These devices typically operate continuously but have low (10 mW) transmit power. However, some devices, especially wireless cameras, operate with (often unauthorized) high power levels, and have high-gain antennas Amateur Radio operators can transmit two-way Amateur television (and voice) in the 2.4 GHz band - and all ISM frequencies above 902 MHz - with maximum power of 1500 watts in the US if the transmission mode does not include spread spectrum techniques. Other power levels apply per regions. In the UK, the maximum power level for a full license is 400 watts. In other countries, maximum power level for non-spread spectrum emissions are set by local legislation. Although the transmitter of some video cameras appears to be fixed on one frequency, it has been found in several models that the cameras are actually frequency agile, and can have their frequency changed by disassembling the product and moving solder links or dip switches inside the camera. These devices are prone to interference from other 2.4 GHz devices, due to the nature of an analog video signal showing up interference very easily. A carrier to noise ratio of some 20 dB is required to give a "clean" picture.

Continuous transmissions interfere with these, causing "patterning" on the picture, sometimes a dark or light shift, or complete blocking of the signal.

Non-continuous transmissions, such as Wi-Fi, cause horizontal noise bars to appear on the screen, and can cause "popping" or "clicking" to be heard in the audio.

- **Wireless Microphones:** Wireless Microphones operate as transmitters. Some digital wireless microphones use the 2.4 GHz band (e.g. AKG model DPT 70).

- **Microwave ovens:** Microwave ovens operate by emitting a very high power signal in the 2.4 GHz band. Older devices have poor shielding, and often emit a very "dirty" signal over the entire 2.4 GHz band.

  This can cause considerable difficulties to Wi-Fi and video transmission, resulting in reduced range or complete blocking of the signal.

  The IEEE 802.11 committee that developed the Wi-Fi specification conducted an extensive investigation into the interference potential of microwave ovens. A typical microwave oven uses a self-oscillating vacuum power tube called a magnetron and a high voltage power supply with a half wave rectifier (often with voltage doubling) and no DC filtering. This produces an RF pulse train with a duty cycle below 50% as

the tube is completely off for half of every AC mains cycle: 8.33 ms in 60 Hz countries and 10 ms in 50 Hz countries.

This property gave rise to a Wi-Fi "microwave oven interference robustness" mode that segments larger data frames into fragments each small enough to fit into the oven's "off" periods.

The 802.11 committee also found that although the instantaneous frequency of a microwave oven magnetron varies widely over each half AC cycle with the instantaneous supply voltage, at any instant it is relatively coherent, i.e., it occupies only a narrow bandwidth.The 802.11a/g signal is inherently robust against such interference because it uses OFDM with error correction information interleaved across the carriers; as long as only a few carriers are wiped out by strong narrow band interference, the information in them can be regenerated by the error correcting code from the carriers that do get through.

8.3 Future Scope

1. In this research work, comparative analysis was performed among different active inductor models and all active inductor models were based on the basic gyrator-C topology following configuration 8.1 in which forward path is common source configured and feedback path is common drain configured. But the active inductors could be configured in another way like forward path with common source configuration and feedback path with common gate configuration as shown in figure 8.2 and in this case there would have been performance variations. In future the simulation of the later basic gyrator-C active inductor can be performed for analyzing its performing parameters like power consumption, quality factor, frequency range etc and for this configured active inductor, a new design of VCO can be accomplished whether to check comparative performance with the previously designed voltage controlled oscillator models with the new one.
2. We could not complete Layouts and subsequent design steps due to time limitation. Therefore, the next steps of the design process, i.e. Layout, Extraction, Post Layout Simulation, Mask Generation, Fabrication and Testing are required for the completion of the process. We want to show that the active inductors will consume less silicon area in any chip.

3. More research can be performed with a view to enhancing the frequency range and thereby our design can be implemented for high frequency applications.

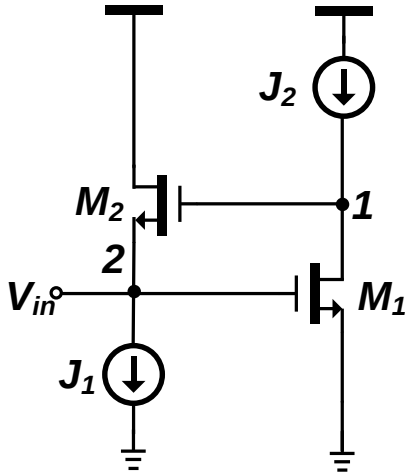


Figure 8.1: Currently used Basic Gyrator-C configuration.

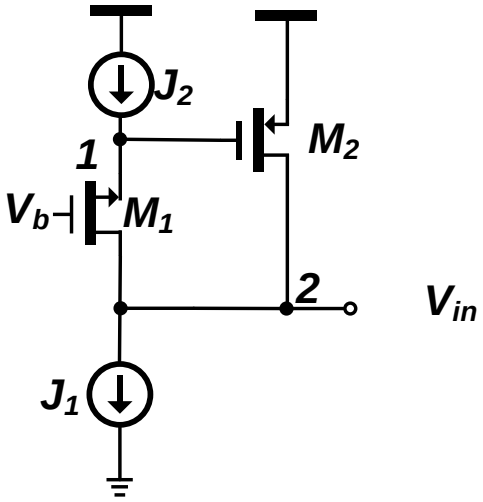


Figure 8.2: Basic Gyrator-C configuration for future work.

REFERENCES

[1] P. E. Allen and D. R. Holberg, “CMOS Analog Circuit Design.” p. 808, 2002.

[2] N. E. H. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, vol. 53, no. 9. 2013.

[3] N. E. H. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, vol. 53, no. 9. 2013.

[4] F. Y. Project, R. Y. Author, D. Rohan, S. Xavier, and A. Cervera, “Engineer (Electronic) Design of CMOS Active Inductors and their use in tuned narrowband and wideband-extension Low Noise Amplifier Final Year Project Escola Tècnica Superior d ’ Enginyeria Industrial de Barcelona,” no. June, 2014.

[5] M. Fillaud and H. Barthelemy, “Design of a wide tuning range VCO using an active inductor,” 2008 *Jt. IEEE North-East Work. Circuits Syst. TAISA Conf.* NEWCAS-TAISA, vol. 0, no. 2, pp. 13–16, 2008.

[6] B. Razavi, “Challenges in Design of Frequency Synthesizer WirelessApplications,” Cicc. pp. 1– 8, 1998.

[7] T. Amin, “On the Selection of Passive Elements for Low Phase Noise LC Tank VCO in 65 nm Process,” vol. 1, 2016.

[8] Krzysztof Iniewski, Advanced Circuits for Emerging Technologies, New Jersey: John Wiley & Sons, Inc, 2012.

[9] N. Nguyen and R. Meyer, “SI IC-compatible inductors and LC passive filters*,” IEEE Journal of Solid-State Circuits,* Vol. 25, No. 4, pp. 1028–1031, 1990.

[10] Md. T. Amin, “On the selection of passive elements for low phase noise LC tank VCO in 65 nm process,” *3rd International Conference on Electrical Engineering and Information & Communication Technology (iCEEiCT-2016),* Dhaka, Bangladesh, 2016.

[11] V. L. Belini and M. a. Romero, “Design of active inductors using CMOS technology,” Proceedings. *15th Symp. Integr. Circuits Syst. Des.*, no. February 2002, pp. 5–10, 2002.

[12] S. Vallabhbhai and P. Polytechnic, “Quality-Factor Improvement of 0 . 18-μm Active Inductor by a Current Reuse Design,” pp. 202–205, 2015.

[13] Wai-Kai Chen, “Passive, Active and Digital Filters”, Boca Raton : CRC Press LLC, 2005

[14] T. Deliyannis, Yichuang Sun and J.K. Fidler, Continuous-Time Active Filter Design, Boca Raton: CRC Press LLC, 1996

[15] H. U. Uyanik and N. Tarim, “Compact low voltage high-Q CMOS active inductor suitable for RF applications,” Analog Integr. Circuits Signal Process., vol. 51, no.3,pp.191–194,2007.

[16] R. L. Geiger and E. Sânchez-sinencio, “Active Filter Design Using Operational Transconductance Amplifiers: A Tutorial,” 1985.

[17] R. M. Weng and R. C. Kuo, “An 0-Q tunable CMOS active inductor for RF bandpass filters,” Conf. Proc. Int. Symp. Signals, Syst. Electron., pp. 571–574, 2007.

[18] Fei Yuan, CMOS Active Inductors and Transformers: Principle, Implementation, and Applications , New York: Springer, 2008

[19] C. Yue and S. Wong. “On-chip spiral inductors with patterned ground shields for Si-based RF IC”. *IEEE J. Solid-State Circuits*, 33(5):743–752, May 1998.

[20] A. Zolfaghari, A. Chan, and B. Razavi. “Stacked inductors and transformers in CMOS technology”. *IEEE J. Solid-State Circuits*, 36(4):620–628, Apr. 2001.

[21] B. Owens, S. Adluri, P. Birrir, R. Shreeve, K. Mayaram S. Arunachalam, and T. Fiez. “Simulation and measurement of supply and substrate noise in mixed-signal ICs”. *IEEE J. Solid-State Circuits*, 40(2):382–391, Feb. 2005

[22] T. Soorapanth and S. Wong. “A 0-dB IL 2140±30 MHz bandpass filter utilizing Q enhanced spiral inductors in standard CMOS”. *IEEE J. Solid-State Circuits*, 37(5):579–586, May 2002

[23] S. Mohan, S. Hershenson, M. Boyd, and T. Lee. “Simple accurate expressions for planar spiral inductances”. *IEEE J. Solid-State Circuits*, 34(10):1419–1424, Oct. 1999.

[24] W. Kuhn, F. Stephenson, and A. Elshabini-Riad. “A 200 MHz CMOS Q-enhanced LC bandpass filter”. *IEEE J. Solid-State Circuits*, 31(8):1112–1122, Aug. 1996.

[25] C.Yue, C. Ryu, J. Lau, T. Lee, and S.Wong. “A physical model for planar spiral inductor on silicon”. In *Proc. Int’l Electron Devices Meeting*, pp 155–158, Dec.1996.

[26] O. Kenneth. “Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies”. *IEEE J. Solid-State Circuits*, 33(8):1249–1252,Aug. 1998.

[27] Y. Cao, R. Groves, X. Huang, N. Zamdmer, J. Plouchart, R. Wachnik, T. King, and C. Hu. “Frequency-dependent equivalent-circuit model for on-chip spiral inductors”.

IEEE J. Solid-State Circuits, 38(3):419–426, Mar. 2003.

[28] Y.Wu, X. Ding, M. Ismail, and H. Olsson. "RF band-pass filter design based on CMOS active inductors". *IEEE Trans. Circuits and Systems II*, 50(12):942–949, Dec. 2003.

[29] A. Thanachayanont and A. Payne. "CMOS floating active inductor and its applications to band-pass filter and oscillator design". *IEE Proceedings, Part G - Circuits, Devices, and Systems*, 147(1):42–48, Feb. 2000.

[30] A. Thanachayanont. "A 1.5-V high-Q CMOS active inductor for IF/RF wireless applications".In*Proc. IEEE Asia-Pacific Conf. Circuits Syst.*, volume 1, pages 654–657,2000.

[31] T. Lin and A. Payne. "Design of a low-voltage, low-power, wide-tuning integrated oscillator". In *Proc. IEEE Int'l Symp. Circuits Syst.*, volume 5, pages 629–632, Geneva,Switzerland, May 2000.

[32] Y. Wu, M. Ismail, and H. Olsson. "CMOS VHF/RF CCO based on active inductors". *IEE Electronics Letters*, 37(8):472–473, Apr. 2001.

[33] A. Thanachayanont. "Low-voltage low-power high-Q CMOS RF bandpass filter". *IEEE Electronics Letters*, 38(13):615–616, June 2002.

[34] H. Xiao and R. Schaumann. "Very-high-frequency low-pass filter based on a CMOS active inductor". In *Proc. IEEE Int'l Symp. Circuits Syst.*, vol 2, pages 1–4, May 2002.

[35] H. Xiao, R. Schaumann, and W. Daasch. "A radio-frequency CMOS active inductor and its application in designing high-Q filters". In *Proc. IEEE Int'l Symp. Circuits Syst.*,volume 4, pages 197–200, Vancouver, May 2004.

[36] L. Lu, Y. Liao, and C.Wu. "A miniaturized Wilkinsonpower divider with CMOS active inductors". *IEEE MicrowaveWireless Components Letters*, 15(11):775–777, Nov. 2005.

[37] J. Liang, C. Ho, C. Kuo, and Y. Chan. "CMOS RF band-pass filter design using the high quality active inductor". *IEICE Trans. on Electron*, E88-C(12):2372–2376, Dec. 2005.

[38] F. Mahmoudi and C. Salama. "8 GHz tunable CMOS quadrature generator using differential active inductors". In *Proc. IEEE Int'l Symp. Circuits Syst.*, volume 3, pages 2112–2115, May 2005.

[39] L. Lu, H. Hsieh, and Y. Liao. “A wide tuning-range CMOS VCO with a differential tunable active inductor”. *IEEE Trans. on Microwave Theory Appl.*, 54(9):3462–3468, Sept. 2006.

[40] H. Xiao and R. Schaumann. “A 5.4-Ghz high-Q tunable active-inductor bandpass filter in standard digital CMOS technology”. *Analog Integrated Circuits and Signal Processing*, 51(1):1–9, Apr. 2007.

[41] R.Weng and R. Kuo. “An *ωo*-Q tunable CMOS active inductor for RF bandpass filters”.In *Proc. Int’l Symp. Signals, Systems, and Electronics*, pages 571–574, Aug. 2007.

[42] A. Tang, F. Yuan, and E. Law. “CMOS class AB active transformers with applications in LC oscillators”. In *IEEE Int’l Symp. Signals, Systems and Electronics*, pages 501– 504, Montreal, Aug. 2007.

[43] A. Thanachayanont and S. Ngow. “Class AB VHF CMOS active inductor”. In *Proc. IEEE Mid-West Symp. Circuits Syst.*, volume 1, pages 64–67, Aug. 2002.

[44] D. DiClemente and F. Yuan. “Current-mode phase-locked loops : a new architecture”. *IEEE Trans. on Circuits Syst. II.*, 54(4):303–307, Apr. 2007.

[45] A. Tang, F. Yuan, and E. Law. “A new constant-Q active inductor with applications in low-noise oscillator”. *IEE Electronics Letters*, Oct. 2007

[46] Y. Wu, M. Ismail, and H. Olsson. “CMOS VHF/RF CCO based on active inductors”. *IEE Electronics Letters*, 37(8):472–473, Apr. 2001

[47] B. Razavi. Design of CMOS integrated circuits for optical communications. McGraw Hill, Boston, 2003.

[48] U. Yodprasit and J. Ngarmnil. “Q-enhanced technique for RF CMOS active inductor”. In Proc. *IEEE Int’l Symp. Circuits Syst.,* volume 5, pages 589–592, Geneva, May 2000.

[49] T. Floyd, Electronic devices, Upper Saddle River, NJ: Prentice Hall, 2005.

[50] B. Razavi, Design of analog CMOS integrated circuits, New York: McGraw-Hill, 2000.

[51] B. Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice Hall, 1998.

[52] R. L. Boylestad and L. Nashelsky, Electronic Devices and Circuit Theory,NJ:Pearson, 2012.

[53] A.S. Sedra and K. C. Smith, Microelectronic Circuits: Oxford University Press, USA, 2007.

[54] B. Razavi, Fundamentals of Microelectronics, River Street, Hoboken,NJ: Wiley, 2006.

[55] M. Tiebout, Low Power VCO Design in CMOS, Berlin Heidelberg: Springer, 2006.

[56] E. Abiri and R. Hamzehyan N. C. Shirazi, "A 5.5 GHz Voltage Control Oscillator (VCO) with a Differential Tunable Active and Passive Inductor," *International Journal of Information and Electronics Engineering*, vol. 3, no. 5, pp. 493-497, September 2013.

[57] S. K. Hsieh and P. J. Tsai J. T. Yang, "A wide tuning range voltage-controlled oscillator with active inductors for bluetooth applications," *in Proceedings of the 4th international conference on Circuits, systems and signals,*Corfu Island, 2010, pp.39-42

[58] Y. Park,P. Sen, N. Srirattana, J. Lee,C. Ho Lee, S. Nuttinck, A. Joseph,John D. Cressler and J. Laskar R. Mukhopadhyay, "Reconfigurable RFICs in Si-Based Technologies for a Compact Intelligent RF Front-End," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 81 - 93, JANUARY 2005.

[59] D. Leeson. “A simple model of feedback oscillator noise spectrum”. Proceedings of IEEE, 54(2):329–330, Feb. 1966.