DESIGN AND ANALYSIS OF LOW NOISE LOW POWER FREQUENCY SYNTHESIZERS FOR WIRELESS COMMUNICATIONS USING 90 NM CMOS TECHNOLOGY

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APPROVAL CERTIFICATE

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DEDICATION

To my parents and family

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All praise to The Almighty. First of all, I would like to express my solemn gratitude to Almighty Allah.

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ABSTRACT

Phase-Locked Loop (PLL) based frequency synthesizer is one of the most crucial components in mobile or wireless communications. It is mainly used for frequency multiplication with the help of a PLL. With the development of RFICs in the wireless communication sector, researchers are trying their best to improve IC's specifications. Their main concerns are area and power consumption. So for a highly efficient frequency synthesizer design, a highly efficient PLL is required to sustain this challenge. The main focus of this thesis work is to design a PLL that is comprised of voltage controlled oscillator (VCO), charge pump with low pass filter (LPF), phase-frequency detector (PFD), and frequency divider (FD) in such a way that the circuit consumes less power as well as require a small area.

In this thesis, a power-efficient LC VCO model for D band wireless applications in 90 nm CMOS technology is developed and presented. An area-efficient design of the proposed model is ensured by avoiding the requirement of additional capacitor for an LC tank and varactor utilizing the parasitic capacitance of MOSs. An oscillation frequency of $(163.25 - 172.77)GHz$ is obtained with the applied tuning voltage while it consumes a low DC power $(2.822.96)mW$. The proposed VCO provides relatively high output power on its differential terminal and the simulated phase noise varies from $-92.99dBc/Hz$ to $-75.81dBc/Hz$. Additionally, an area-efficient and low phase noise charge pump, frequency divider and, two GDI (Gate Diffusion Input) cells based simple PFD have been developed and presented in this thesis. For charge pump design, instead of using an op-amp, the cascade technique is applied to reduce current mismatch, nonlinear effect, and complicity. The proposed charge pump occupied $275.28\mu m^2$ silicon area in layout design with dc power consumption $34.1\mu W$ from the supply voltage of 1V. This simple structured PFD dissipates layout area of $26.95\mu m^2$ and it consumes DC power of $2.391fW$. The Dynamic D FF FDs dissipated layout area and DC power are $101.74\mu m^2$ and $4153.893nW$ respectively. Finally, from the post-layout simulation for each design, it is found that the parasitic components didnt change the circuit performances drastically from the schematic based simulations.

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LIST OF ABBREVIATIONS

AM	Amplitude Modulation
BER	Bit Error Rate
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
FD	Frequency Divider
FF	Flip-Flop
FM	Frequency Modulation
FOM	Figure of Merit
GDI	Gate Diffusion Input
GSM	Global System for Mobile
IC	Integrated Circuit
ILD	Injection-locking divider
LPF	Low Pass Filter
MS	Master-Slave
PFD	Phase Frequency Detector
PLL	Phase Locked Loop
RF	Radio Frequency
TSPC	True-Single-Phase-Clock
VCO	Voltage Controlled Oscillator

LIST OF SYMBOLS

A_v	Voltage gain
C_{gd}	Gate to drain capacitance
C_{gs}	Gate to source capacitance
C_{ox}	Oxide capacitance
f_D	Divider frequency
f_{in}	Input frequency
f_{out}	Output frequency
f_{REF}	Reference frequency
g_m	transconductance
I_{dn}	Down current
I_p	Pump current
I_{up}	Up current
K_{VCO}	Tuning gain or the sensitivity of the circuit
M	Multiplication factor
N	Number of delay cells
R	Shunt resistance
R_{out}	Output resistance
t_d	Propagation delay
V_b	Biasing voltage
V_{DD}	Power supply
V_p	Pump voltage
ω_o	Resonant frequency
Z	Impedance

CHAPTER 1

INTRODUCTION

1.1 Background

From the mid-1930s, PLL was used as a part of the Synchronization of the level and vertical outputs of TV. Nowadays, ascertained PLL uses in legion different applications. Around 1965, the primary PLL ICs were accessible; which was containing simple parts. Later on with the advancement in coordinated circuit outline methods, digital PLL has been developed, which is more efficient and trustworthy. Presently, an entire PLL circuit can be comprised as a piece of a bigger circuit on a single chip.

PLL is the heart of the electronics and Communication Systems. A lot of research work are done on the outline of Phase Locked Loop (PLL) [1–3] circuit and still research is going on this subject to improve its performance in modern technology. The major portion of the research work have desire to design a higher lock range PLL with lesser lock time and have decent stage noise. The most common use of PLL is for clock locking and check recuperation in microchip, microprocessors, microcontrollers, and recurrence synthesizers. In digital systems, PLLs are normally used to produce very much timed clock on chip. Presently communication systems utilize Phase Locked Loop (PLL) basically for synthesis of clock, synchronization, skew and jitter lessening [4]. PLL being a blended sign circuit includes outline challenge at high recurrence.

1.2 Problem Statement and Research Motivation

The Phase Locked loop (PLL) has been a highly popular control system in the broad area of electronic communication. However, its further development still continues with its more efficient design considerations and better performance. A PLL

consists of a phase-frequency detector, low pass filter (LPF), charge-pump, voltage controlled oscillator (VCO) and a frequency divider. It is a negative-feedback closed-loop system that minimizes the phase error between the feedback and reference signals. The PLL circuit has a wide application in synchronization and synthesis of clock, jitter reduction in mobile or wireless communications.

The development of designing PLL can achieved by the efficient design of voltage controlled oscillator, phase-frequency detector, charge pump and low pass filter and frequency divider, i. e. VCO is one of a major block of PLL system which is having two types, one is LC VCO and the other is ring VCO. The LC VCO provides a better phase noise but consume large area where ring VCO provides a large tuning range but the phase noise is more. Although numerous systems have already existed for several years, the challenge of designing a PLL with low noise, low power consumption and lower area is tough to achieve.

A substantial number of literature related to phase locked loop or different schemes of voltage controlled oscillator, charge pump, low pass filter and phase frequency detector have been reviewed, which leads to identify the research gap and thus to formulate the research question: can a PLL be designed in an effective manner for wireless applications with low noise as well as low power with a very lower area? To answer this question all the building blocks of PLL need to study and analyzed.

1.3 Research Objectives

In light of the identified gap in the area of the proposed research aims to design a PLL having low noise, lower silicon area and low power requirement with higher frequency range. Specific aims with the individual blocks of the PLL are as follows:

a) To design low noise, low area and low power VCO for carrier frequency generation.

b) To analyze and design of low power PFD architectures for a fast locking PLL.

c) To design and analyze of charge pump with LPF and frequency divider for the desired PLL with specific specifications.

d) To validate the proposed PLL based frequency synthesizer, layout based performance will be compared with the state-of-the-art.

The expected outcome of the thesis work will be a smaller and more efficient PLL design for wireless applications that will have low noise, lower silicon area and low power consumption with a higher frequency range.

1.4 Organization of the Thesis

The remainder of this thesis is organized as follows.

Chapter 2 captures the background of the proposed research on the frequency synthesizer: Phase Lock Loop (PLL). It covers the state of PLL, and the block diagram of PLL. With the applications of PLL, problems are in each major components are also discussed.

Chapter 3 covers the literature review of PLL, VCO, CP, PFD and FD.

Chapter 4 presents the state of Voltage Control Oscillator (VCO) for different technologies and the development of the proposed VCO circuitry. The simulated results and performance are also discussed with comparing other designs in this chapter.

Chapter 5 presents the design of an efficient charge pump (CP) with Low Pass Filter for an efficient design of PLL. Performance analysis are evaluated in cadence and compared with other designs.

Chapter 6 presents an efficient Phase Frequency Detector (PFD) and Frequency Divider (FD). Both of them are simulated in cadence and the evaluation of performance of the implemented schemes are discussed comparing with technologies.

Chapter 7 presents the conclusion of the thesis with a summary of the original contributions and future work.

CHAPTER 2

FUNDAMENTALS OF PLL

2.1 Introduction

Historically, earliest research towards what became known as the phase-locked loop goes back to 1932, when British researchers developed an alternative to Edwin Armstrong's super heterodyne receiver, the Homodyne or direct-conversion receiver. The technique was described in 1932, in a paper by Henri de Bellescize, in the French journal L'Onde lectrique. Besides, in analog television receivers since at least the late 1930s, phase-locked-loop horizontal and vertical sweep circuits are locked to synchronization pulses in the broadcast signal. When Signetics introduced a line of monolithic integrated circuits that were complete phase-locked loop systems on a chip in 1969, applications for the technique multiplied. A few years later RCA introduced the "CD4046" CMOS Micropower Phase-Locked Loop, which became a popular integrated circuit.

Phase Locked Loop is a circular loop formed by the negative feedback. It locks the frequency and phase of the input signal. The main motive of this PLL is to generate a signal whose phase and frequency will be same as the reference signal. The output signal will be locked when the bandwidth of it come in the lock range of PLL. The reference or input clock is sent through different blocks and is fed back as feedback signal at the input of PLL. This loop will be continued until the phase and frequency of the signal is same as the reference signal.For the generation of high clock frequency from multiple low clock frequency Phase Locked Loop is used. In many electronic devices, PLL acts as a control system to control the working process.

The design of PLL circuit is depend on the requirement for the given system. But mostly there are five major components presents in the block to perform the properly. The block diagram of PLL circuit consisting of these blocks are shown in Figure 2.1. They are:-

– Phase Frequency Detector (PFD)

– Charge Pump (CP)

– Low Pass Filter (LPF)

– Voltage Controlled Oscillator (VCO)

– Frequency Divider (FD)

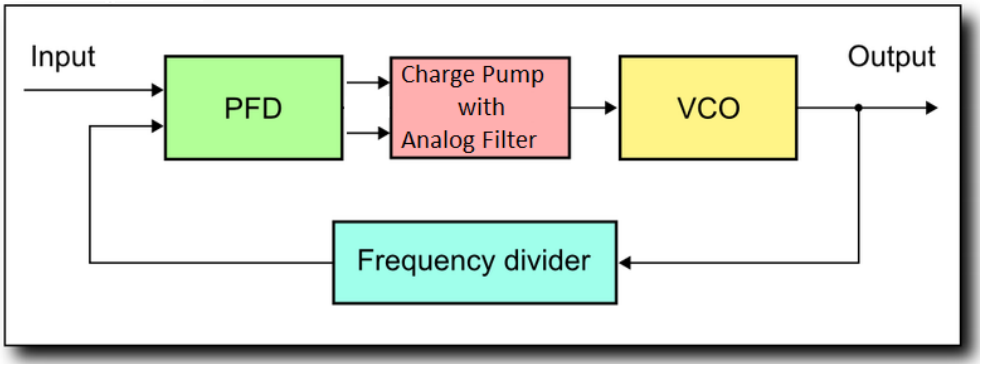

Figure 2.1: Block diagram of PLL.

An input signal or reference signal is given to Phase Frequency Detector [5, 6]. Depending upon the raising edges, PFD generates two signal outputs UP and DOWN. These output signals are sent to Charge Pump which generates both positive and negative current. The output of charge pump is fed to low Pass Filter. LPF allows only the signals with low frequencies blocking the higher frequency terms that are obtained in PFD. Voltage Controlled Oscillator [3,7,8] is the heart of PLL circuit takes the control voltage from the output LPF. The change in output of VCO depends on the DC control voltage i.e. the output of PFD. Phase and frequency values of VCO increases due to increase in error voltage of PFD by the generation of UP at the output of PFD. In contrast, The frequency and phase of VCO output decreases due to decrease in control

voltage obtained at LPF due to generation of DOWN at output of PFD.

2.2 Terminology of PLL

Lock range

The range of input signal frequencies over which the loop can maintain the lock is called as Lock Range or Tracking Range of PLL. The lock range is wider than the capture range.

Capture range

The range of input signal frequencies over which PLL can acquire a lock is called as Capture Range or Acquisition Range of PLL. It is the range of frequencies such that the initially unlocked PLL becomes locked.

On the amount of the gain present in a loop and the loop filter bandwidth, capture range depends. With the reduction of the loop filter bandwidth, the rejection of the out of band signals improves, but at the same time the capture range decreases, phase margin becomes poor and pull in time becomes larger.

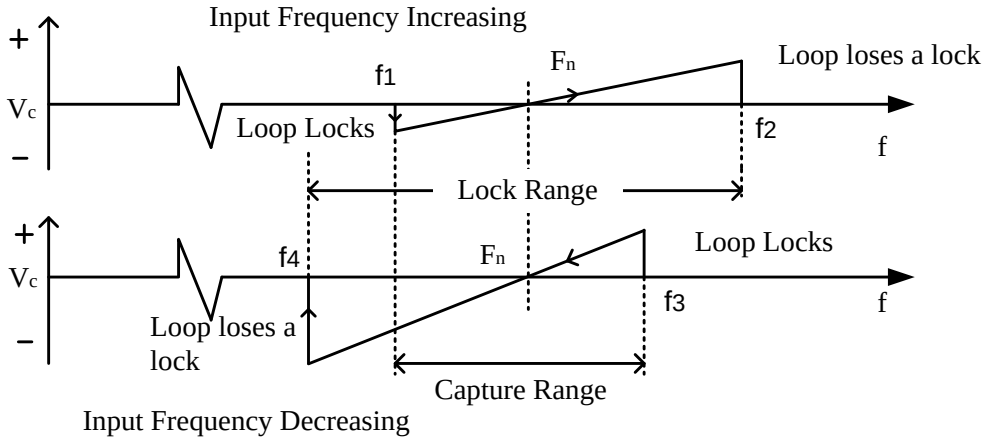

Figure 2.2: Illustration of terminologies of PLL.

Pull in time

The total time taken by the PLL to capture the signal (or to establish the lock) is

called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

Band width of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.3 Types of PLL

Various types of PLL architectures according to the application are accessible now. These different architectures of PLL are considered as different types of PLL. According to their application following types of PLL are classified .

Programmable PLL: For programming a wide range of signal this type of PLL are used.

Single and multi-phase PLL: In digital clock networks single and multi-phase PLL are used to control a single or many phases.

Digital Phase Locked Loop: They are used, digital input signals for application like Manchester coding.

PLL with lock detector: It uses a lock on one of the pins and is used in frequency modulation.

PLL frequency synthesizer: These are used to select the frequency from different range and band.

PLL FM/AM demodulator: This PLL are used for the modulation and demodulation of the radio frequencies.

Single RF/ Multi RF PLL: For controlling single or multiple radio frequencies it is used.

Super PLL: It is used for frequency synthesizing of networks of GSM, cordless phones, radios etc.

Another type of classification of PLLs are depends on the architecture of the loop filter. The order of loop filter is the type of PLL. For example, if 1^{st} order loop filter

is used, then it is called as type I PLL. If 2^{nd} order filter is used, it is called as type II PLL and so on.

2.4 Non Ideal Effects in PLL

So many imperfections are always persist in practical PLL circuit. These lead to high ripple on the control voltage, even when the loop is locked. These ripples regulate the VCO frequency, which generates non periodic waveform. This section considers as non ideal effects in PLL.

2.4.1 Jitter in PLL

A jitter is the short term-term fluctuation of a signal from its ideal position in time. This problem negatively affects the data transmission quality. Deviation from the ideal position can occur on either leading edge or falling edge of signal. Jitter may be induced with a clock signal from different sources and is not uniform over all frequencies. Excessive jitter can enhance bit error rate (BER) of communication signal. In digital system, Jitter leads to violation in time margins, for which circuits act improperly. Common sources of jitter induction:

- Internal circuitry of PLL
- Random Thermal noise from crystal
- Other resonation devices
- Random mechanical noise from crystal vibration
- Signal transmitters
- Traces and cables
- Connectors
- Receivers

Now consider a purely periodic waveform, $x_1(t)$, contains zero crossing, evenly spaced in time. Besides, consider another nearly periodic signal $x_2(t)$, whose period

undergoes a small changes, deviating the zero crossing from their ideal positions. Here, $x_2(t)$ suffers from jitter. If the instantaneous frequency of signal varies slowly from one period to next period, then it is called as "slow jitter", and if the variation is fast, it is called as "fast jitter". In PLL, two types of factors are considered.

a) The input demonstrates jitter and

b) The VCO produces jitter.

2.4.2 Phase noise

Phase noise occurs due to the random variation of phase of the signal. It is the frequency domain representation of rapid, short term variations in the phase of the wave, caused by time domain instabilities (jitter). Generally the phase noise and jitter are closely related. Phase noise is very much concern item in PLL, since it directly affects the entire performance of the system. Following are the common sources of phase noise in PLL.

Oscillator noise: In PLL, two oscillators contribute to the phase noise. One is the reference oscillator and other is the VCO. Although both oscillators can be structured similarly, but the effects on the output noise are distinct just due to their different positions in the loop. Suppose a noise less VCO is added with AWGN with DSPSD of No/2. Then the output power spectrum is given by $KVCO^2(No/2\omega^2)$. This equation represents the presence of output noise in PLL due to the presence of VCO noise. Similarly, the reference oscillator will also added some phase noise.

Frequency Divider noise: The excess noise of a digital divider can be considered as additive noise source at the output of PLL. This noise directly appears at the input of phase detector and experiences the same transfer function as the noise on the input terminal.

Phase detector noise: Generally phase detectors are not major sources of noise in PLLs. As the function of PD is to detect the phase difference, any random fluctuation

in the phase of input signal moderate the phase detector to generate wrong output, which will transfer through filter and tunes the VCO wrongly.

2.4.3 Reference spur

Reference spurs are spurious emissions that occur from the carrier frequency when the offset is equal to the channel spacing. Due to the leakage and mismatch in charge pump these spur occurs in PLL. Though they occur outside the band of interest, they can enter the mixers and be translated back onto band of interest.

Reference spur mainly produced in Charge Pump PLL. At the locked state, when no phase difference between reference and feedback signal, the phase detector (or phase frequency detector) produces very narrow pulse width error voltage which drives the charge pump. Although these pulses have a very narrow width, the fact that they exist means that the dc voltage driving the VCO is modulated by a signal of frequency equal to input reference frequency. This produces reference spurs in the RF output occurring at offset frequencies that are integer multiples of input reference frequency.

2.5 Applications of PLL

From the innovation, PLL continues to increase new applications in electronics, communication and instrumentation. Like memories, hard disk drive electronics, microprocessors, RF and wireless transceivers, clock recovery circuits on microcontroller boards and optical fibre receivers everything have PLL. Some of the applications are as follows.

Frequency multiplication and synthesis

A PLL can be implemented as multiplier, where it multiplies its input frequency by factor of M. Figure 2.3 shows basic frequency multiplication concept.

Just like a voltage divider is used in feedback in voltage amplifier, as shown in Figure 2.3, output frequency of PLL is divided by M and applied to the phase detector,

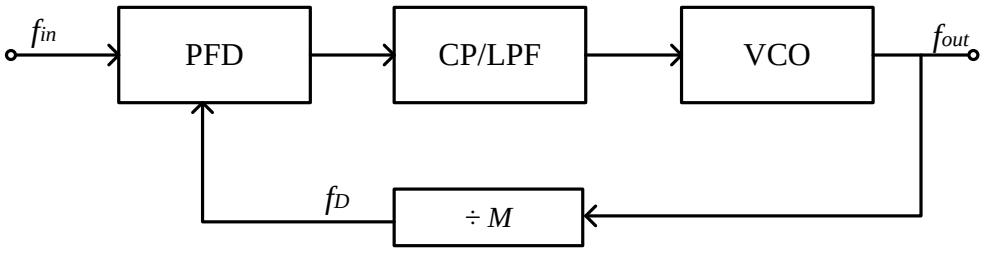

Figure 2.3: Frequency Multiplication.

here, $f_{out} = Mf_{in}$. Also, since f_{in} and f_D must be equal, PLL multiplies f_{in} by M. Some systems require a periodic waveform whose frequency (a) must be very accurate and (b) can be varied in very fine stapes. Hence to synthesise a required frequency, a channel control word (digital) is applied to divider block in feedback that varies the value of M. Since $f_{out} = Mf_{REF}$, the relative accuracy of f_{out} is equal to that of f_{REF}. It is also notable that f_{out} varies in stapes equal to f_{REF} if M changes by one each time.

Skew reduction

Presence of skew is the prime issue in PLL. Suppose synchronous pair of data and clock lines enter into a large digital chip. Since clock typically runs a large number of transistors and logic interconnects, it is first applied to large buffer. Thus, the clock may suffer from substantial skew (delay due to buffer insertion) with respect to data. This will effect the operation timing of the chip.

Now consider the circuit as shown in Figure 2.4. Here input clock CK_{in} is applied to on PLL and a buffer is placed inside the loop. Since PLL generates a nominally zero phase difference between CK_{in} and CK_B, the skew is eliminated. That is, the constant phase shift introduced by the buffer is divided by infinite loop gain of the feedback system. Alignment of V_{VCO} with CK_{in} is not important since V_{VCO} is not used.

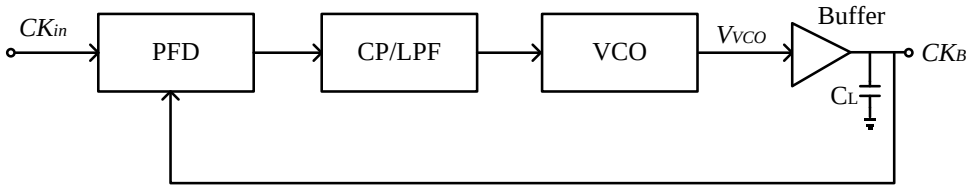

Figure 2.4: Use of PLL to eliminate Skew.

2.6 Basic Infrastructures of PLL

Phase Locked Loop circuits are designed in many ways i.e. depending on their requirement their structure and number of blocks changes . Most commonly used are five to obtain the basic PLL circuit. The design of PLL circuit is shown in Figure 2.1. The main blocks of PLL are Phase Frequency Detector, Charge Pump, Low Pass Filter, Voltage Controlled Oscillator and Frequency Divider. A detailed explanation of all the blocks are given below.

2.6.1 Phase frequency detector (PFD)

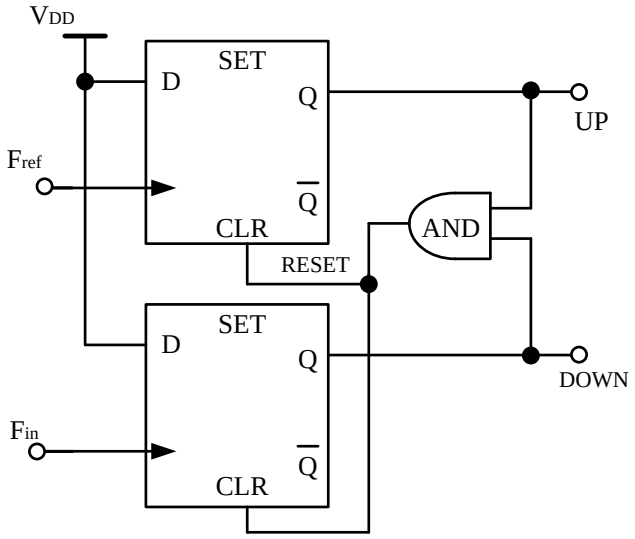

Figure 2.5: Conventional PFD.

The block diagram of PLL as shown in Figure 2.1,where it has two input ports, one input or reference signal, whose phase and frequency will be compared with the

feedback signal coming through another port and fed to charge pump. Depending upon the necessity in the particular filed, different types of PFDs are available. Some of them are Conventional PFDs, PFDs with N transistors, where N is integer and PFD with variable delay element etc. The circuit diagram of conventional PFD is shown in Figure 2.5. Here, PFD produces two signals, UP and DOWN depending on the change in Phase and frequency. If the raising edge of feedback signal is lead by the raising edge of input signal, then UP terminal gets output. Similarly, if the raising edge of input signal is lead by the raising edge of feedback signal, then DOWN terminal gets output of the PFD. This result of the PFD is fed to Charge Pump to proceed the further process.

Problems in the conventional PFD

To improve the operating speed of PFD, both the pulse width and the propagation delay of reset signal need to be reduced. In the previous design, the reset signal is structurally affected by the DFF delay. To improve the operating speed of PFD, both the pulse width and the propagation delay of the reset signal need to be reduced.

According to that, the way to decrease the width pulse and the delay of the reset signal (and so, increase the speed of operation) is to reduce these two delays, avoiding its dependence with the DFF device.

PFD with dynamic CMOS logic

This improvement attempt consists on redesign the D-FF device using dynamic logic instead static one. Dynamic CMOS logic circuits are constructed with small transistor number and also, reduce parasitic node capacitance compared with static CMOS logic.

This new design could be over twice as fast as with static logic. It uses only fast N transistors, and is amenable to transistor sizing optimizations. Static logic is slower because it has twice the loading, higher thresholds, and actually uses slow P transistors to compute things.

In it, propagation delay and pulse width of the reset signal are shorter than in the conventional one and it can improve the frequency limit of the PFD. The only disadvantage of the dynamic CMOS circuit is its high power consumption. In this thesis, in chapter 5 a low power, low area PFD is simulated and discussed with the present typologies of PFD.

2.6.2 Charge pump (CP)

The function of a Charge Pump is to works as DC to DC converter. In PLL, the position of it is between PFD and Low Pass Filter. It generates both positive and negative currents. So it is also called as current synthesizer or voltage generators. This generated voltage will control the output of the VCO. It receives two input signals from PFD and converts it to single output value to fed the VCO.

A charge pump works as a three position electronic switch which depends on the three states of PFD. When switch is set in UP or DOWN position, it delivers a pump voltage $\pm V_p$ or a pump current $\pm I_P$ to the loop filter. When both UP and DOWN of PFD are off, i.e. N position, the switch is open, thus isolating the loop filter from the charge pump and PFD.

Figure 2.6 shows the combined architecture of the charge pump and loop filter. Current sources I_{up} and I_{dn} are identical. Two outputs of PFD Q_A and Q_B are given to the UP and DOWN inputs of charge pump (CP) respectively. Capacitor C_p serves the purpose of loop filter.

Many charge pumps are developed as per requirement. Some of them are Gain-Boosting CP, Transmission Gate CP, Ratio current CP etc. All these CPs strive to reduce current mismatch, reference spur and fluctuations in the input of VCO.

The advantage of Gain Boosting charge pump is to reduce the current mismatch which may generate fluctuations in PLL. While ratio current charge pump may suppress the magnitude of reference spur. To obtain this the size of source and drain are

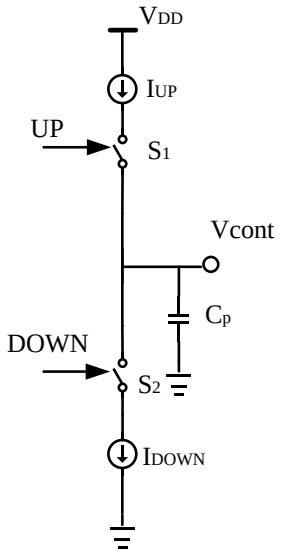

Figure 2.6: Basic Charge Pump.

need to change. A simplified design of charge pump is proposed in this thesis, which is analyzed and compared with other present works.

2.6.3 Low pass filter (LPF)

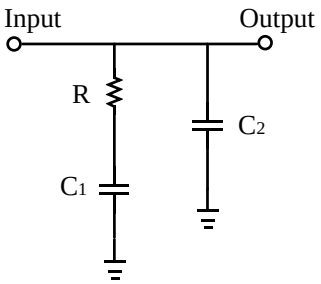

Figure 2.7: Simple Low Pass Filter.

Low Pass Filter is used to block the high frequency signals from the PFD and allows only low frequency signals. It generates DC voltage by which the output is varied. This DC voltage is used to control the output frequency of the Voltage controlled oscillator. The output of LPF is fed to VCO input. The DC voltage of LPF depends on input and reference frequency. If both are same and so they are locked then it maintains constant value. A simple low pass filter circuit is shown in Figure 2.7.

2.6.4 Voltage controlled oscillator (VCO)

Voltage Controlled Oscillator is the heart of Phase Locked Loop. It take a DC voltage as input and gives the corresponding frequency. The output voltage of LPF is fed to VCO based on that controlled VCO generates frequency. The general tuning characteristics of a VCO is shown in Figure 2.8.

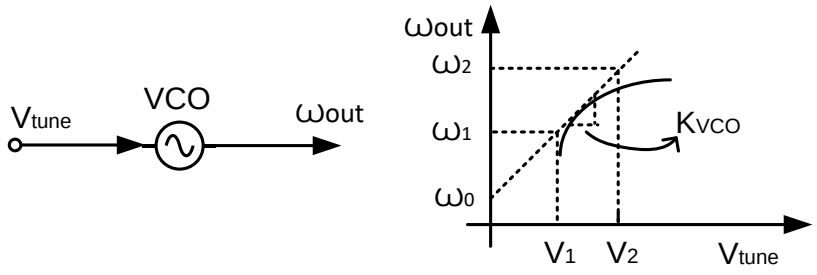

Figure 2.8: Tuning characteristics of Voltage-Controlled Oscillators.

Here, from the figure it can say, that the output frequency varies from ω_1 to ω_2 (the required tuning range) as the control of the tuning voltage is tuned from V_1 to V_2. For an ideal VCO, the output frequency can be expressed in Eq. 2.1.

$$\omega_{out} = \omega_0 + K_{VCO}.V_{tune} \tag{2.1}$$

Where, ω_0 represents the intercept corresponding to $V_{tune} = 0$ and K_{VCO} is the tuning gain or the sensitivity of the circuit. The achievable frequency range is called the tuning range of the circuit.

Performance parameters of VCO

Center Frequency: The center frequency is the midrange value in the characteristics curve shown in Figure 2.8 which is determined by the particular application the VCO is designed for.

Tuning Range: For most applications it is better for the VCO to provide a wide tuning range to make sure the output of the circuit can be driven to the desired value

for process and temperature variation. Wide tuning range in oscillators has a direct conflict with the phase noise performance. To optimize phase noise, the VCO should be designed to have minimum sensitivity to the control lines which reduces the gain of the circuit and degrades the tuning range.

Tuning Linearity: The output frequency of the VCO must be linearly proportional to the control voltage. It is desirable to minimize the variation of Kvco across the tuning range.

Output Amplitude: It is desirable to have large output amplitude which makes the oscillator less sensitive to noise. The output amplitude has trade-offs with power dissipation, power supply and tuning range. The amplitude is desired to be constant across the tuning range.

Power Dissipation: The design of oscillators is a tradeoff process that involves power consumption, speed and phase noise performance. Depending upon application some metrics need to be traded for the others. Sometimes if the power consumption of an oscillator is to be optimized, its phase noise performance degrades.

Phase noise performance: The output signal of the oscillator is not perfectly periodic as generally assumed. The intrinsic noise of the devices and the sensitivity if the oscillator results in random variation in output phase and frequency leading to undesirable effects. These effects are characterized by phase noise and determined by the requirements of each application.

VCO topologies

Phase noise, power dissipation and tuning range are the most important performance metrics to consider in VCO design. Due to the co-existence of multiple communication standards, multi-standard transceivers are needed to address the market requirements. The choice of VCO topologies depend on the performance parameters that the application needs to be focused. LC and ring VCO are the primary VCO

topologies circuits which are used for signal generation purpose.

LC VCO

LC oscillators have low phase noise which makes them appropriate for use in radio frequency frameworks. They have a larger area when contrasted with ring oscillator. LC-VCOs are utilized to give input for mixers to up-convert and down-convert signals and have primary significance in fully-integrated transceivers. The best combination of very low phase noise specifications with very low power utilization (battery operation) urges the VLSI planners to use LC-VCOs in different areas. Inductor and capacitor combined together with active circuit to compensate the passive elements losses build the LC VCOs. The LC resonator forms feedback mechanism to obtain steady oscillations and determines the frequency of oscillation. The oscillation frequency will be-

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{2.2}$$

Voltage dependent capacitors called "varactors" are employed for frequency tuning. In CMOS technology, a varactor can be realized by a regular MOS transistor where the source and drain terminals are tied together as discussed in chapter 3.

Ring VCO

Ring oscillator (RO) is formed by using an even and odd number (N) of open loop inverting amplifiers (A) or delay cells (or stages) coupled in a feedback loop with positive value. To accomplish oscillation, open loop gain of the oscillator should be higher than unity and the ring requires a phase shift of 2π. If the propagation signal passes twice over the chain of N no of delay cells with propagation delay t_d, the oscillation frequency of the ring oscillator would be

$$f_{osc} = \frac{1}{2Nt_d} \tag{2.3}$$

Ring oscillators can be designed with single-ended or differential structures. The

total number of inversions in the loop must be odd so that the circuit doesnt latch up. Single-ended structures can be implemented only with odd number of delay stages. Differential structures can be designed also with even number of delay stages simply by configuring one stage such that it doesnt invert.

2.6.5 Frequency divider (FD)

In modern integrated transceivers operating at microwave frequencies, one of the most critical parts is the frequency divider chain of the PLL frequency synthesizer. Being the VCO output frequency in the order of several GHz, the problem of actually implementation of the frequency division at such high frequencies is a non trivial one. In fact, depending on the frequency that needs to be divided, different approaches can be used. The simplest way to implement a clock frequency division is to design a digital counter, with a digital logic resetting the counter after a number of input clock cycles equal to the division ratio have been counted. The drawback of this kind of solution is the limited maximum frequency of operation due to the digital logic with which the counter is implemented. Usually, such a frequency divider will operate up to few GHz (typically no more than 3-4 GHz). On the other side, such a frequency divider has the advantage of low power consumption, and the possibility of being programmable by dynamically changing the resetting logic (and thus the division ratio). When a higher frequency division is necessary, a purely analog solution has to be taken into consideration. The two main solutions to multi-GHz frequency division are: master-slave (MS) latch divider, and injection-locking divider (ILD). The MS divider employs a two stage regenerative divider based on analog differential latch to perform a divide-by-2 frequency divider stage.

The divider network divides the high frequency output clock such that the reference clock matches the feedback clock in phase and frequency in locked condition. The number of divider units (D flip-flops) gives the division factor. A divide by N divider

will have log2N stages. This thesis implements a true-single phase clock (TSPC) based D flip-flop. This topology is used because it avoids racing condition. Detail of the frequency divider design is discussed in chapter 5 of this thesis book.

2.7 Chapter Summary

The Phase-locked loop frequency synthesizer is a critical component in communication devices. It works as a local oscillator for frequency translation and channel selection in wireless transceivers and broadband cable tuners. It also plays an important role as the clock synthesizer for data converts in the analog-and-digital signal interface. In this chapter all the components are discussed in brief, that are required to design an efficient PLL.

CHAPTER 3

LITERATURE REVIEW

3.1 Introduction

Several recent works on PLL-based FMCW modulators employ the so-called two-point injection technique to over-come the limited bandwidth of a standard PLL [9–11]. The technique is based on the additional injection of the modulating signal in a point of the loop featuring a highpass transfer function to the output. The combination of the two injection points, the low- and the high-pass one, allows achieving wider modulation bandwidth. Obviously, the twopoint injection technique to properly operate needs a good matching between the two injection paths. An alternative solution is based on the pre-emphasis of the digital modulation signal, this technique was originally exploited by Perrott et al. [12] to modulate at high rate the output frequency of a PLL. In practice, a pre-emphasis filter is introduced to approximate the inverse frequency response of the PLL. Like in the two-point injection scheme, good matching between pre emphasis filter and inverse PLL response is required in this case. The key issue of both approaches is therefore to guarantee matching between two different transfer functions within a certain degree. The least mean squares (LMS) algorithm has been already demonstrated to allow background calibration of building blocks variations and correction of mismatches [13,14] and this makes digital phase-locked loops (DPLLs) the natural candidates to implement such systems. Unfortunately, in any PLL, the characteristics of the building blocks are not only unpredictablele and dependent on process, voltage and temperature variations, but they are also nonlinear. Both the gain of a standard voltage controlled oscillator (VCO) and the gain of a digitally controlled oscillator (DCO) can substantially change

over the tuning range. Even in structure that are optimized to this purpose it is difficult to maintain the gain variation below 5%, [9], while in standard structures the gain can change by 100% over the tuning range, [15]. A typical value of the gain error that can be considered is about 20 $\%$ across the tuning range. This is usually not an issue in a PLL that works at a fixed output frequency, but it is relevant when the PLL is employed to frequency-modulate the carrier over a wide range. In that case, the calibration algorithm cannot track gain variations, giving rise to gain estimation errors.

3.2 Literature Review on VCO

Different techniques have been developed to design an area efficient and wideband tuning range LC VCO. For example, the fourth-order oscillator was used to improve the phase noise and higher tuning range in VCO implementations [16]. The oscillator drew $1.89mA$ current of $1.8V$ supply and its phase noises at 1 MHz offset for f_1 = 2.4 GHz and f_2 = 4.7 GHz were $-122.4dBc/Hz$ and $-123.4dBc/Hz$, respectively. Borremans *et al*. [17] used a single-inductor and dual band VCO for a very low-area multi standard direct down conversion receiver front-end in $90nm$ digital CMOS. The area size of their VCO is reduced by reusing the single inductor.

Besides, without recurring to switched inductors, switched capacitors, or varactors, Bevilacqua *et al*. [18] designed a transformer-based resonator to build a dual-mode oscillator, e.g., a system capable of oscillating at two different frequencies. A typical phase noise performance at 1-MHz offset of $-104dBc/Hz$ was predicted, while the power consumption ranged from 1 to 8 mW for different VCO configurations. A triple-mode VCO using a 6th-order resonator was designed in [19]. The resonator constituted three coupled inductors with a compact common-centric layout, banks of switched varactors, and continuously-tuned varactors.

Other techniques can also be tracked for improving the phase noise and size of

VCOs in the literature. Safarian *et al*. have designed a wideband Multi-Mode CMOS VCO design using Coupled Inductors [20]. A VCO with adjusting the size of the negative resistance transistors and a switched active core was designed in [21]. A Magnetically Tuned Quadrature Oscillator was designed by Cusmai *et al*. [22] to achieve a figure of merit of 176.5 dB at 3.2 GHz and 170.5 dB at 6.4 GHz. A Multi-Mode CMOS VCO was designed by using Coupled Inductors for an automatic adjustment of the VCO current consumption with a low phase noise throughout the frequency range.

Recently, a complete tuning of frequency of VCOs is investigated without varactors to achieve a wide tuning range with a high figure of merit. Techniques employed in these varactorless LC VCOs include using a transconductance-tuned resonant tank [23], coupling factor adjustment [24], voltage-controlled inductors [25], and tunable negative inductance cell [26]. However, generally the figure of merits, tuning range, and phase noise and size of the existing design of VCOs can further be developed with a more effective use of the MOS parasitic capacitance.

In this thesis, an improved LC VCO is designed and presented by tuning transistor capacitance instead of varactor. A more effective use of the MOS parasitic capacitance is ensured for the low power consumption with high tuning range and high figure of merit and low silicon area for fabrication compared to the relevant techniques reported in the literature. The earlier LC VCOs constitute an LC circuit with a variable capacitor that increase the layout area of the design. Unlike that earlier designs, the proposed LC VCO architecture employs MOS varactor (with low W/L ratios) with high D band frequency range along with low dc power consumption.

3.3 Literature Review on CP

Different design frameworks of CP have been investigated in the literature to improve its performance. A fully differential charge pump circuit is implemented by Zeng *et al*. [27] for the performance improvement of the output spur. The problem with conventional charge pump configuration and limited output swing of a charge pump was addressed by using two current sources in [28]. David *et al*. [29] explicated and evaluated the power efficiency in Dickson and voltage doubler charge pump topologies. Differential input and outputs were adopted and the NMOSFET was used to form up and down switches so that they can solve the problem of current mismatch along with noise reduction capability. The voltage doubler was demonstrated to provide higher power efficiency comparing with Dickson charge pump. Furthermore, in Dickson topology, higher parasitic capacitance aids to reduced output voltage and power efficiency. Conversely, in voltage doubler, lower parasitic capacitance maintains the same driving capability and reduces the silicon area.

To solve the problem of phase offset due to the current mismatch in the charge pump, Ha *et al*. [30] developed the TYPE-1 and TYPE-2 charge pumps. A duel compensation technique was illustrated by Hwang *et al*. [31], where the current mismatch is 3.2% and the output spur of PLL is reduced efficiently. To reduce current mismatch Lee *et al*. [32] designed a charge pump with an error amplifier and reference current source, where the reference spur $<$ -75dBc. Yang *et al*. [33] presented a fully differential charge pump that has a better output currents mismatch where the effect of channel-length modulation is swept by using the replica technique and a rail-to-rail common-mode feedback circuit. In another design, for reducing the channel length modulation effect in the transistors, Miin-Shyue Shiau et. al [34] has designed a charge pump with two differential amplifiers. To recompense the DC current CP calibration technique is used by Manikandan et. al [35].

The improved design of both the single-ended and the differential charge pumps are presented in [36]. In the differential charge pump, two loop filter and common mode feedback circuitry are additionally required. So considering the additional circuitry, more silicon area is required to design. Due to this extra transistor, the design leads to higher power consumption. On the other hand, single ended charge pump shows switch mismatch, clock feedthrough, charge sharing and limited range of output voltage compliance. Even though with all these disadvantages single ended charge pump is most popular than the differential one because of low power requirement and no additional circuitry. To minimize the limitations of single ended charge pump, different topologies like current mirror, transmission gate, self-biased, cascode are proposed by RFIC researchers.

In this thesis, an improved single-ended charge pump is designed by a cascade of transistor, avoiding the use of Op-Amp. For this reason, the designed circuit achieves the lower output spur and low power consumption with a small silicon area.

3.4 Literature Review on Frequency Divider

With the rapid development of coherent wireless communication systems, frequency synthesizers become indispensable. Internet of things (IoT) applications [37–39], for example, will be ubiquitous in the near future and integrate into our daily life.

IoT applications put unprecedented challenges on cost and battery size for IoT sensor nodes [40], in which phase-locked-loop (PLL) synthesizers play a key role in terms of performance as well as power consumption. Within PLL synthesizers, the high-speed divider is a power-hungry block, which transforms a high-frequency input signal into a relatively low one for the following stages. In particular, the prescaler inside dividers often operates at the highest frequency and determines the operating

frequency and power consumption of frequency dividers. For example, a divider which transforms a 4 GHz signal into a 40 MHz signal, a divide-by-4 prescaler could consume more than 50% power consumption of the entire divider. Conventionally, dividers with a division ratio of 2/3, 4/5 or larger ratios are usually implemented for prescalers. However, a divider with a 3/4 division ratio is favorable in some cases. A divide-by-2/3 prescaler or a divide-by-3/4 prescaler consists of two DFFs and some other logic to control the divide ratios. The output frequency of a divide-by-2/3 prescaler is higher than a divide-by-3/4 prescaler. If only one divider is used as a prescaler, the back-stage circuit of a divide-by-2/3 prescaler needs to process a higher frequency signal which is harder to design the back stages. A divide-by-4/5 prescaler usually consists of three or four DFFs. The extra DFFs lead to extra power consumption. However, there are few pieces of research about divide-by-3/4 prescalers. Study about divide-by-3/4 prescaler is valuable. There are several techniques to realize prescalers, including injection-locked frequency dividers [41–43], True single-phase clock (TSPC) D-flip flop (DFF) based dividers [44–47] and true single phase clock (E-TSPC) DFF based dividers [48, 49].In everywhere the basic block is divide-by-1/2. To design an area efficient and low power consumption basic frequency divider is must to design an efficient frequency synthesizer. From this requirement one simple design is implemented in this chapter and the performance of that frequency divider is compared with several works.

3.5 Literature Review on Phase Frequency Detector

The phase detector can be categorized into different types according to its function and realization: sinusoidal, combinational, and sequential. Phase recognition interval in the sinusoidal PFD is ($-\pi/2$ to $\pi/2$) where it operates as a multiplier [50]. Analog multiplier has high speed of operation as compared with other implementations nevertheless it suffers from large power consumption. The combinational phase de-

tector has difficulty in detecting the small phase difference between rising/falling edge of REF and BACK signal and suffers from dead zone problem. PLL locks in incorrect phase due to this problem. Sequential PFD has a memory element, and generally used in PLL structure, mainly in frequency synthesis as compared to the combinational phase detector. Sequential PFD has larger input range which enables increasing of locking speed and acquisition range [51]. Sequential PFDs can be constructed with the help of digital circuits and operate with binary input waveform. Hence, they are recognized as digital PFD. In order to reduce the circuit complexity, reduce the power consumption and increase the operating frequency, numerous design techniques have been reported [5, 52–56]. Here, a schematic of PFD is implemented which shows low power dissipation and can able to operate at higher frequencies. The major challenge in the design of PFD is to obtain high operating frequency with minimum power dissipation. The overall power consumption of PLL can be reduced mainly by minimizing the power consumption in PFD circuit.

3.6 Chapter Summary

Several research works are going on to improve the performance of the VCO, Charge pump, frequency divider and phase frequency detector for different applications of PLL. All of them are good in various aspects but after that they are suffering from high power consumption with larger fabrication area. By addressing this problems it is required to design a Phase Locked Loop which is comprised of Voltage Controlled Oscillator (VCO), Charge Pump with LPF, Phase Frequency Detector and Frequency Divider in such a way that the circuit consumes less power as well as require a small area.

CHAPTER 4

A HIGH FIGURE OF MERIT LOW POWER LC VCO DESIGN

4.1 Introduction

A voltage control oscillator (VCO) is widely and conventionally used in the electronics and communication systems. It becomes an essential part of electronic jamming equipment, function generators, computer disk drives and wireless equipment including cellular phones and other equipment, where the oscillation frequency is generated by an applied tuning voltage [57,58]. It is also an important block of phase locked loop (PLL), which is the heart of many modern electronics and communication systems. A VCO essentially determines the spectral quality of the PLLs, i.e., the efficiency of a PLL to synchronize the oscillators embedded in the integrated circuits. Additionally, with the high gain and high frequency range of the operation, a VCO is required for designing a PLL having a wider tuning range.

The recent development of VCOs is being steered by the rapid advancement of CMOS technology. The VCOs are broadly classified into two types, namely, LC-VCO and ring-VCO. An LC-VCO consists of an LC resonator, referred to as LC tanks that consist of an inductor, L and capacitor, C to generate the oscillation. A ring VCO, on the other hand, employs a ring with the back-to-back connected NOT gates without using any LC tank. Compared to a ring VCO, a LC VCO provides much better performance in phase noise. However, an LC VCO occupies a larger area and has a relatively lower tuning range, which has been investigated in the literature for further improvement.

4.2 Conventional Cross Coupled NMOS LC VCO

According to Barkhausen criteria for sustaining oscillation, the oscillator network must have vast voltage gain with phase shift 0° or 360°. Now the equation of voltage gain for LC oscillator is $A_V = g_m Z$, where Z is the impedance. The value of this gain will be more significant if the impedance is larger and ideally, it is larger at the self-resonant frequency. At the resonant frequency, this impedance is ideally infinite, i.e., $Z(j\omega_o) = \infty$, where $\omega_o = 1/\sqrt{LC}$ is the resonant frequency. However, for a lossy tank, as shown in Figure 4.1, this impedance $Z(j\omega_o) = R$, where R is the shunt resistance. For common source amplifier this voltage gain is $A_v = -g_m R$ with that phase shift is -180 degree. So to fulfill the Barkhausen criteria, two common source amplifier, needs to be connected consecutively with the LC tank and with that, it will also contribute to compensate for the ohmic loss to sustain the oscillation.

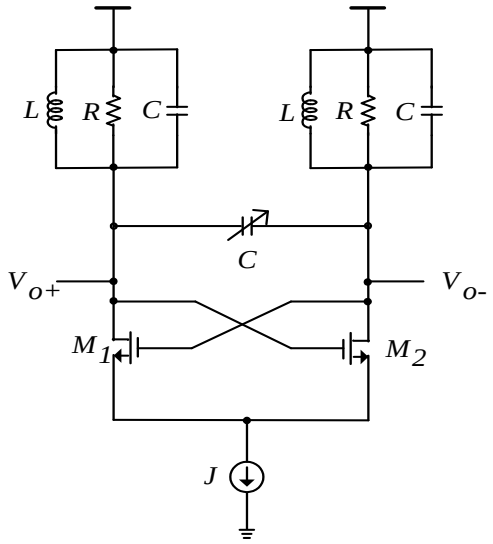

Figure 4.1: Cross coupled nMOS LC VCO.

In Figure 4.1, two cross-coupled transistors ($M_{1,2}$), along with the tail biasing current source J provide the differential negative resistance. The tail current source provides dc biasing current to the cross-coupled transistor for tuning the resistance of the negative resistor. The resistance of the negative resistor is as tuned so that it can

compensate for the resistance of the LC tank [59].

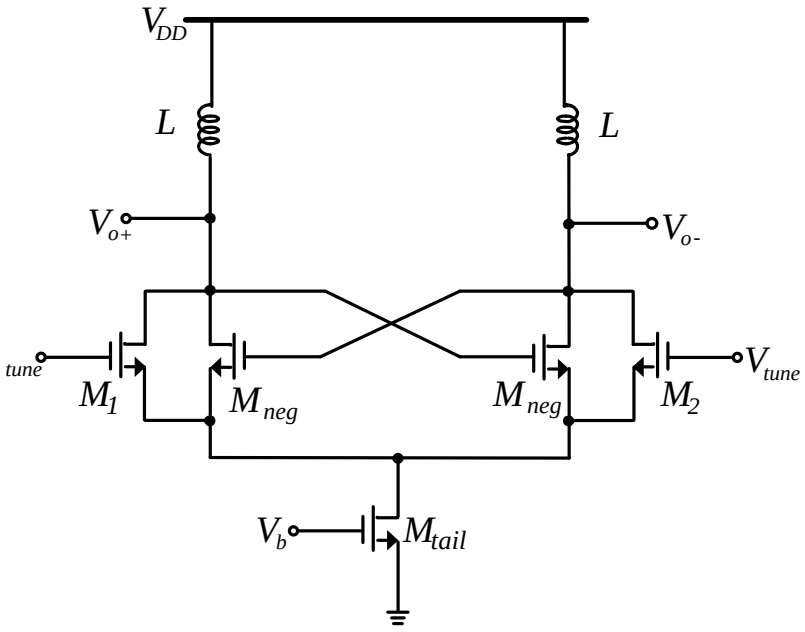

Figure 4.2: Proposed nMOS LC VCO.

4.3 Proposed LC VCO

Figure 4.2 represents the proposed design where inductor, $L_1 = L_2 = 10$ pH is used to design the LC tank and the capacitance of the LC tank is provided by the MOS transistor capacitance (C_{gd}) of MOS $M_{1,2}$ and M_{negs}. Required negative resistance will be provided by the MOSs (M_{neg}) to overcome the resistive loss. Oscillation will sustain with the desired voltage gain and phase shift, which will also be provided by these MOSs. To control the transconductance, g_m=$\sqrt{(2\mu_n C_{ox}(W/L)I_D)}$ of the M_{neg} a tail current source (M_3 operated in a saturation region) is used.

For tuning in general with the LC tank, varactor is used which is implemented by $M_{1,2}$ (W/L ratios are $20\mu/100n$) connected in parallel to M_{negs}. In most cases, the implementation of varactor consumes a noticeable amount of silicon area with respect to the total circuit. As only $M_{1,2}$ are used for the varactor tuning purpose, so in that

case, the total silicon area due to varactor will be reduced. Table 4.1 shows the W/L ratios for all MOSs used in the proposed design. The power supply, V_{DD} and biasing voltage, V_b is fixed at 1V.

Table 4.1: W/L ratios for the used MOSs.

MOS	W/L Ratio
M_1	20 $\mu/100n$
M_2	20 $\mu/100n$
M_{neg1}	20 $\mu/100n$
M_{neg2}	19.9 $\mu/100n$
M_3	5 $\mu/100n$

Figure 4.3 represents the change of gate to source capacitance with the change of tuning voltage. From, this figure we see that with the increasing of tuning voltage gate to source capacitance is increased. The gate to source capacitance does not affect oscillation frequency as they are not linked to the LC tank of the oscillator.

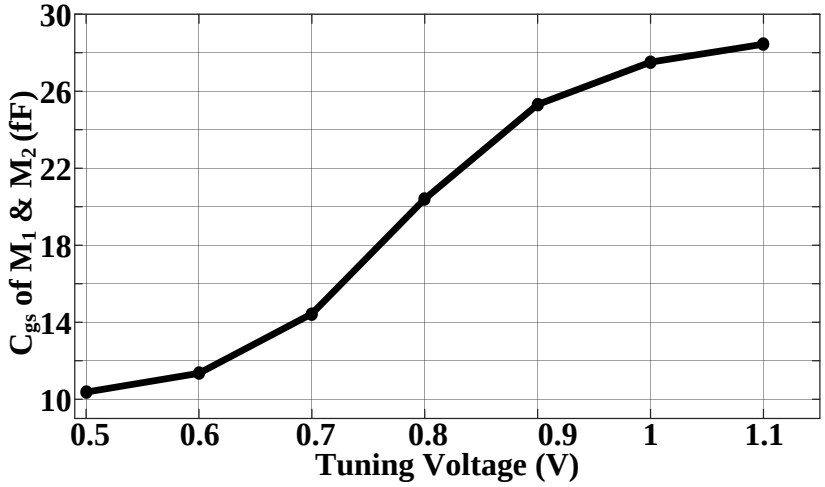

Figure 4.3: Gate to source capacitance vs tuning voltage of MOS M_1 and M_2.

Figure 4.4 shows the change of the gate to drain capacitance with the variation of tuning voltage. With the increased value of tuning voltage, the gate to drain capaci-

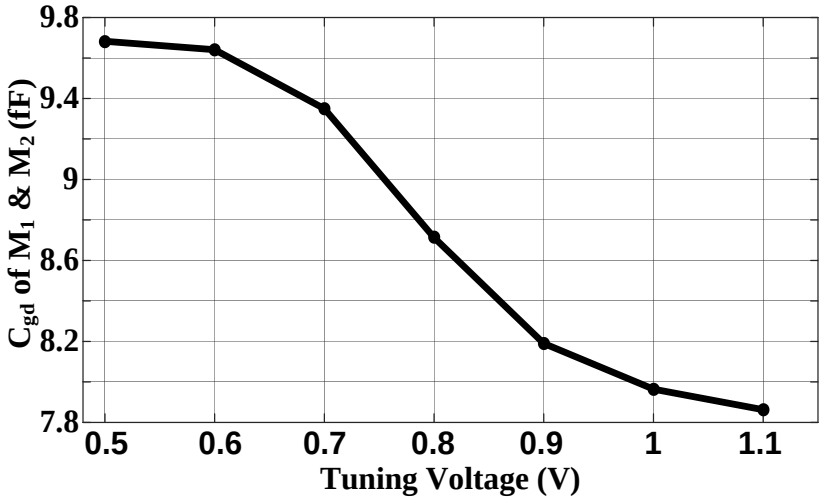

Figure 4.4: Gate to drain capacitance vs tuning voltage of the MOS M_1 and M_2.

tance is decreased. As gate to drain capacitance of MOS M_1 and M_2 are directly linked with the LC tank, so any change in C_{gd} will affect the capacitance of the LC tank. It can be anticipated from the graph that the oscillation frequency will be increased with the growth of the tuning voltage. This is because the decrement of capacitance will enhance the oscillation frequency according to the relation, $\omega_o = 1/\sqrt{LC}$.

4.4 Simulation Results

The proposed design has been simulated in virtuoso cadence environment using 90 nm CMOS process technology. Transient analysis, pss, pnoise and DC analysis have been conducted to determine the performance parameters such as oscillation frequency, oscillation's amplitude, output power, phase noise and DC power consumption. Furthermore, process corner analysis, temperature swept analysis, stability analysis and Monte Carlo analysis have been performed to evaluate the proposed design's sustainability. The tuning voltage of the VCO is varied from 0.5 V to 1.1 V and the oscillation frequency ranges from 163.25 GHz to 172.77 GHz. The tuning scope is 5.67% and the differential output power varies from 15.53 dBm to 6.43 dBm. The proposed VCO consumes a low power ranging from 2.82 mW to 2.96 mW with the change of tuning

frequency. The phase noise @ 1 MHz offset frequency alters from -92.99 dBc/Hz to -75.81 dBc/Hz. Finally, an overall performance parameter considering three performance parameters i.e. oscillation frequency, power consumption and phase noise has been calculated according to the Eq. 4.1.

$$FOM = L(\Delta\omega) + 10\ \log\left(\frac{P_{diss}}{1mW}\right) - 20\ \log\left(\frac{\omega_0}{\Delta\omega}\right) \tag{4.1}$$

Figure 4.5 represents the differential output oscillation for tuning voltage of 0.8 V. the output voltage has peak to peak value of 1.25 V to -1.25 V. Figure 4.6 represents the phase noise with respect to the frequency offset for different tuning voltages. The figure illustrates that high oscillation frequency degrades phase noise performance. Figure 4.7 depicts the frequency of oscillation when the tuning voltage is varied. The variation of frequency occurs from 163.25 GHz to 172.77 GHz along with a tuning range of 5.67%.

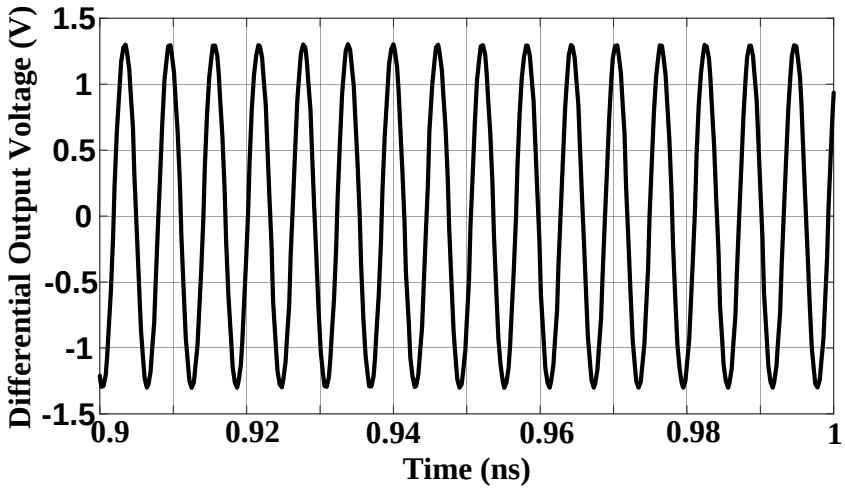

Figure 4.5: Differential output voltage vs time of the proposed VCO for V_{tune} = 0.8V.

The Figure 4.8 shows the figure of merits for the designed VCO with the change of tuning voltage. The figure of merit is almost flat with the tuning voltage from which we can say our proposed VCO is more stable. Table 4.2 summarizes the performance

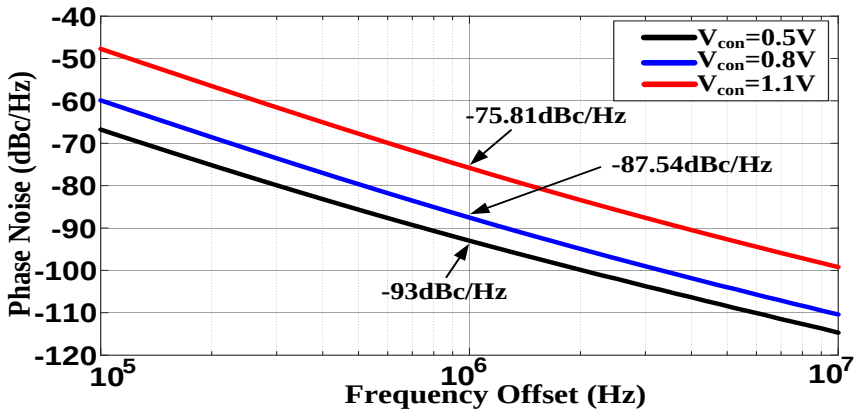

Figure 4.6: Phase noise vs frequency offset for various tuning voltages.

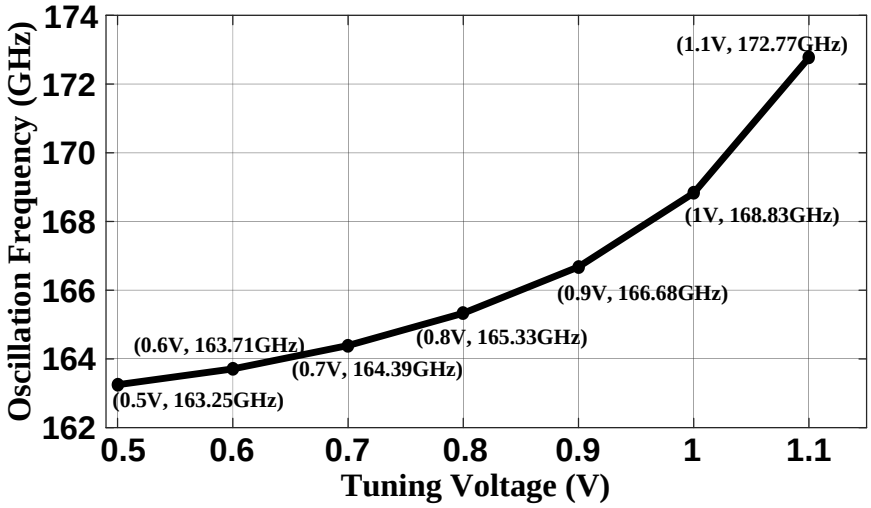

Figure 4.7: Frequency with the variation of tuning voltage for the designed VCO.

of the proposed VCO with different tuning voltages.

4.4.1 Process corner analysis

Due to the wavering of doping concentration, oxide thickness or the threshold voltage of MOSFET, these parameters can deviate from the typical values. Since the current passing through the MOSFET relies on the process parameters, so there may be evolvement of fast corner and slow corner. To ensure the sustainability of a circuit, it must be consistent with the process corner variations. CMOS technology comprises

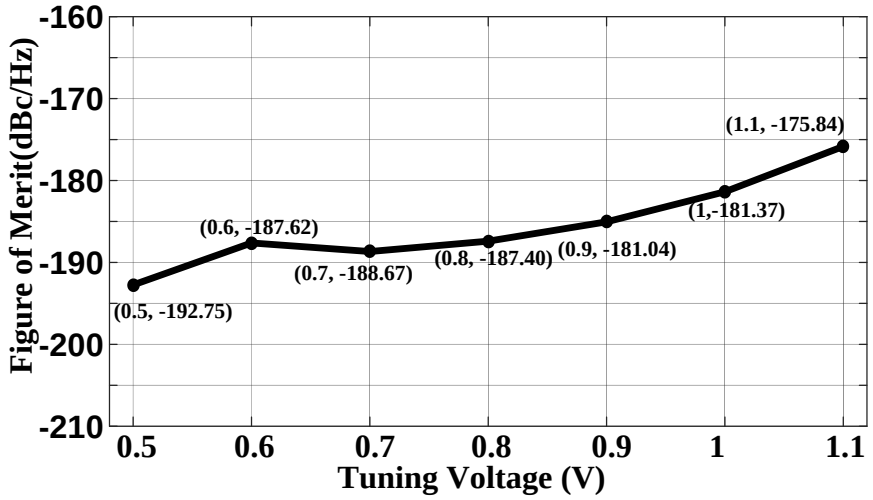

Figure 4.8: Figure of merit vs tuning voltage for the designed VCO.

Table 4.2: Performance parameter for different tuning voltages.

V_{tune} (V)	Freq. (GHz)	Volts (V)	Diff. output Power (dBm)	Power (mW)	PN @ 1MHz (dBc/Hz)	FOM (dBc/Hz)
0.5	163.25	1.89	15.53	2.82	-92.99	-192.75
0.6	163.71	1.72	14.72	2.82	-87.84	-187.62
0.7	164.39	1.53	13.71	2.82	-88.85	-188.67
0.8	165.33	1.34	12.52	2.82	-87.54	-187.40
0.9	166.68	1.13	11.08	2.85	-85.15	-185.04
1.0	168.83	0.92	9.24	2.90	-81.44	-181.37
1.1	172.77	0.66	6.43	2.96	-75.81	-175.84

of NMOS and PMOS where the process corner variation due to NMOS and PMOS are independent. So the process corner variation can be SS (slow NMOS and slow PMOS), SF (slow NMOS and fast PMOS), FS (fast NMOS and slow PMOS) or can be FF (fast NMOS and fast PMOS). The midpoint of the four corners represents the typical value. In this simulation, only NMOS is used so the results of the process corner only for the slow NMOS and fast NMOS will be found. Figure 4.9 shows the variation of DC power consumption with the tuning voltage for SS/SF and FS/FF process corner variation. For SS/SF corner the DC power consumption varies from 1.93 mW to 2.05

mW where for FS/FF corner it varies from 3.75 mW to 3.91 mW.

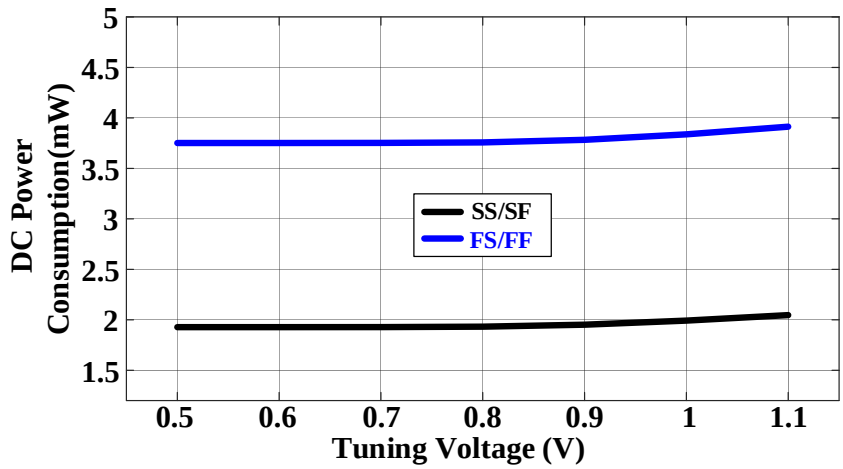

Figure 4.9: Simulated DC power consumption vs tuning voltage for process corner.

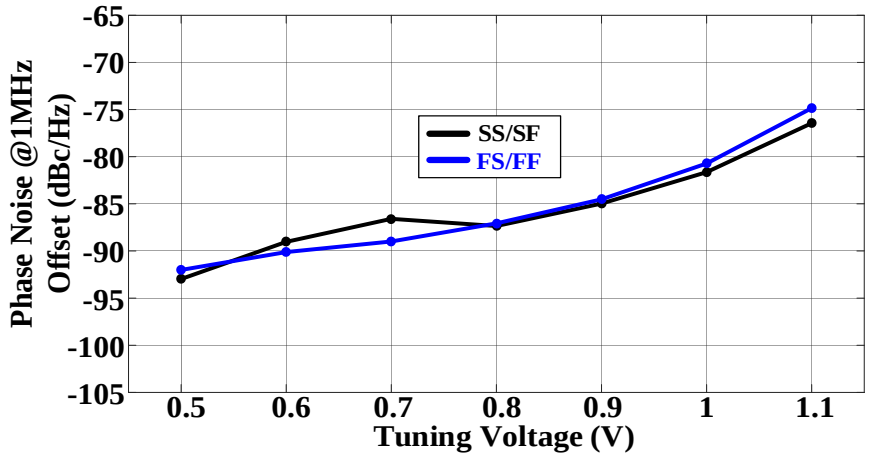

Figure 4.10: Phase noise @ 1MHz offset frequency vs tuning voltage with the process corner variation.

In Figure 4.10, with the process corner variation SS/SF and FS/FF the MOSFETs phase noise @1MHz offset is obtained for different tuning voltages. For the process corner variation SS/SF phase noise vary from -92.48 dBc/Hz to -76.44 dBc/Hz and for FS/FF the range is -91.96 dBc/Hz to -74.93 dBc/Hz. Figure 4.11 represents the process corner variation SS/SF and FS/FF for the oscillation frequency with respect to tuning voltage. The oscillation frequency varies from 165.7 GHz to 173.95 GHz for the SS/SF similarly for FS/FF 160.48 GHz to 171.39 GHz.

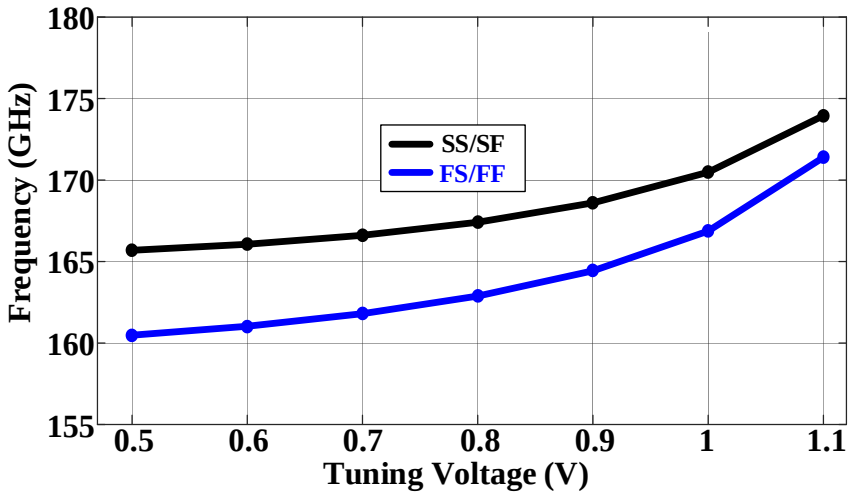

Figure 4.11: Oscillation frequency vs tuning voltage for the process corner.

4.4.2 Temperature swept analysis

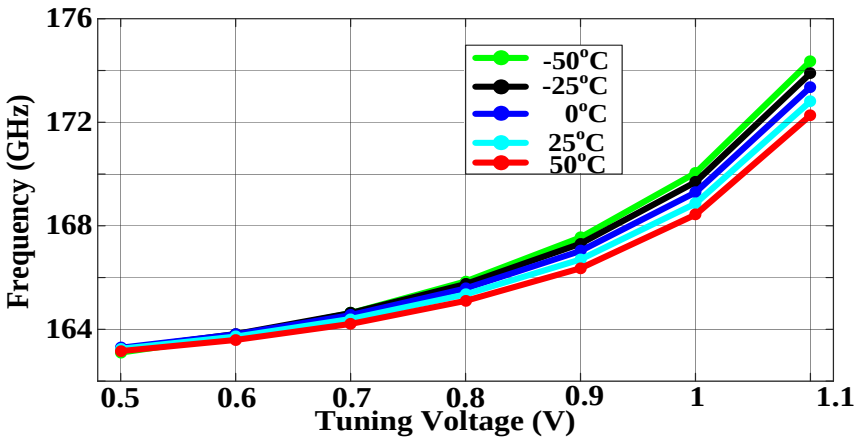

Figure 4.12: Oscillation frequency vs tuning voltage with the variation of temperature.

Since the variation of temperature influences mobility and the threshold voltage of MOSFET, the proposed VCO should have the ability to tolerate the temperature's variation. The VCO's performance parameters have been determined for five different environments of temperature ranges from -50°C to 50°C (with an interval of 25°C). It can be noticed from Figure 4.12 that the temperature increasing effect is aversive for higher frequency i.e. the higher the temperature the lower the values of oscillation

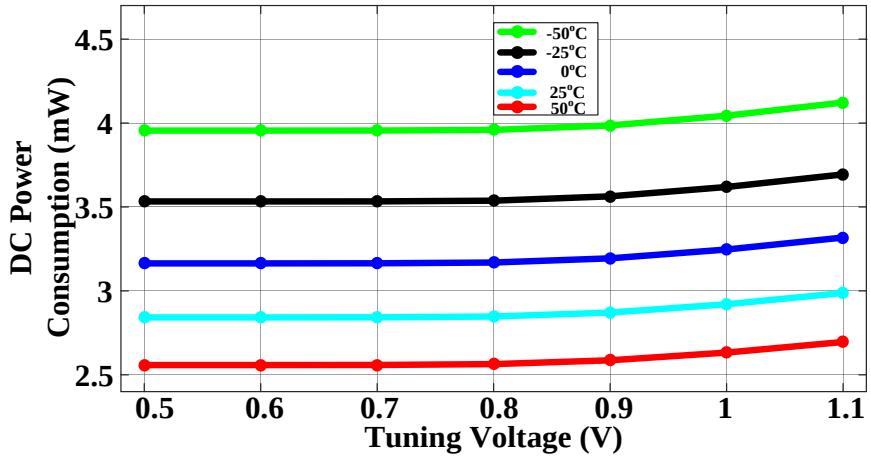

Figure 4.13: DC power consumption vs tuning voltage with the change of temperature.

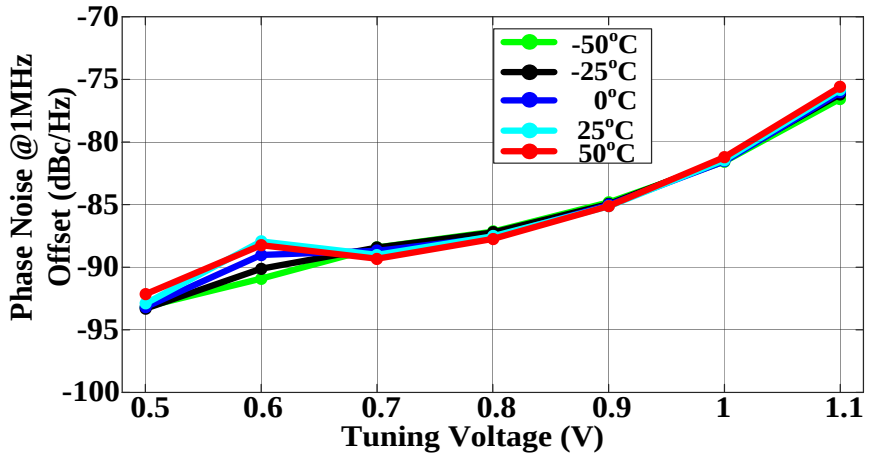

Figure 4.14: Phase noise @ offset frequency vs tuning voltage with the variation of temperature.

frequency. However, Figure 4.13 indicates that temperature rising effect is favorable to DC power consumption i.e. the higher the temperature the lower the dc power consumption. Finally, Figure 4.14 illustrates the effect of phase noise at different temperatures. It is clear from the figure that temperature variation hardly impacts the phase noise i.e. the phase noise is resistant to temperature variation.

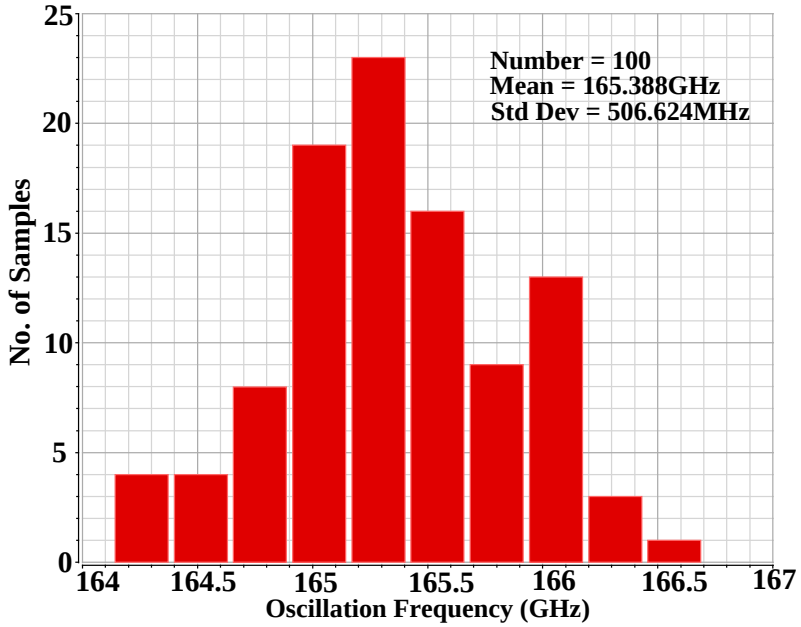

Figure 4.15: Statistical distribution of oscillation frequency for tuning voltage of 0.8V.

4.4.3 Monte Carlo analysis

The Monte Carlo analysis of the proposed design had been performed for both process variation and mismatch cases simultaneously for tuning voltage of 0.8V. During simulation 100 samples were considered for oscillation frequency, phase noise@1MHz offset and DC power consumption. Figure 4.15, Figure 4.16 and Figure 4.17 respectively show the statistical presentation of Monte Carlo Simulation results for frequency, DC power consumption and phase noise@1MHz offset respectively. The oscillation frequency has a mean of 165.388 GHz with a standard deviation of 506.624 MHz, where for the case of phase noise they are -87.5192 dBc/Hz (mean) and 210.203 mdBc/Hz (standard deviation). Finally, in the case of DC power consumption, the mean is 2.82005 mW having a lower valued standard deviation (76.5927μW).

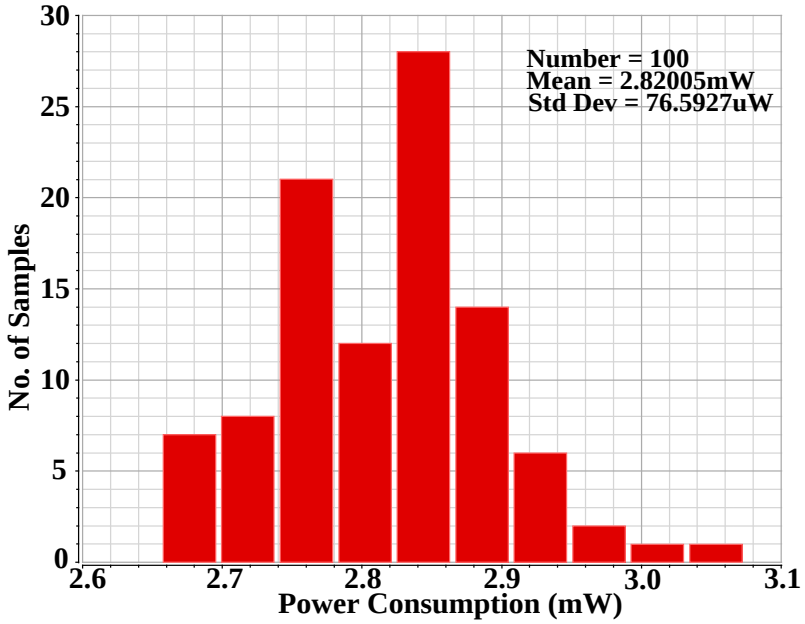

Figure 4.16: Statistical distribution of DC power consumption for tuning voltage of 0.8V.

4.4.4 Stability analysis

For an ideal oscillator, the loop gain at the oscillating frequency, f_0, should be 1, so the dB20 (loop gain) and the Phase (loop gain) both should be zero at f_0 and the phase should change abruptly at f_0. In practice, both dB20 (loop gain) and the Phase (loop gain) should be close to zero. For this simulation, the PSS analysis gives $f_0 = 165.33$ GHz for the tuning voltage 0.8 V. From Figure 4.18, the PSTB analysis gives dB20 (loop gain) = 0 and Phase (loop gain) = 0.

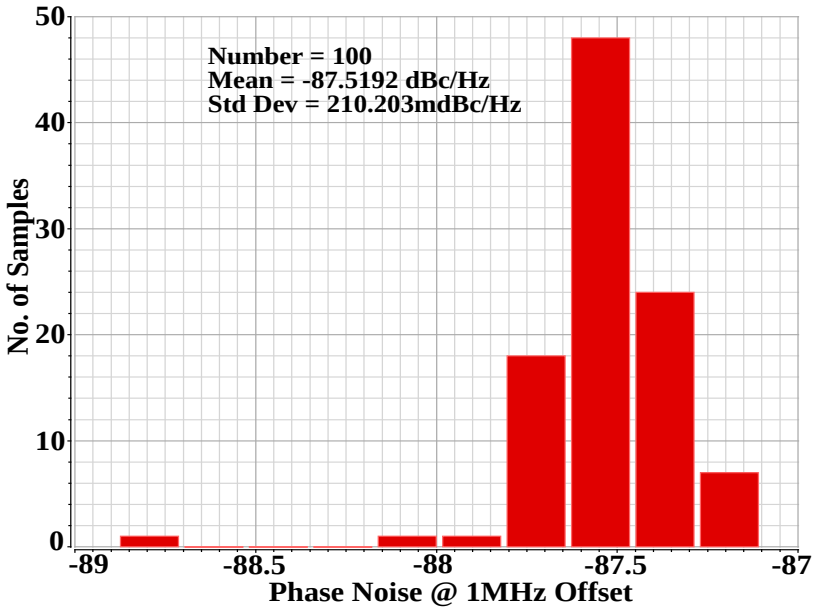

Figure 4.17: Statistical distribution of phase noise @ 1MHz offset for tuning voltage of 0.8V.

4.5 Performance Comparison

Comparisons have been made with the state-of-the-art and shown in Table 4.3. The proposed VCO shows a low power, high figure of merit and high output power compared with other reported references.

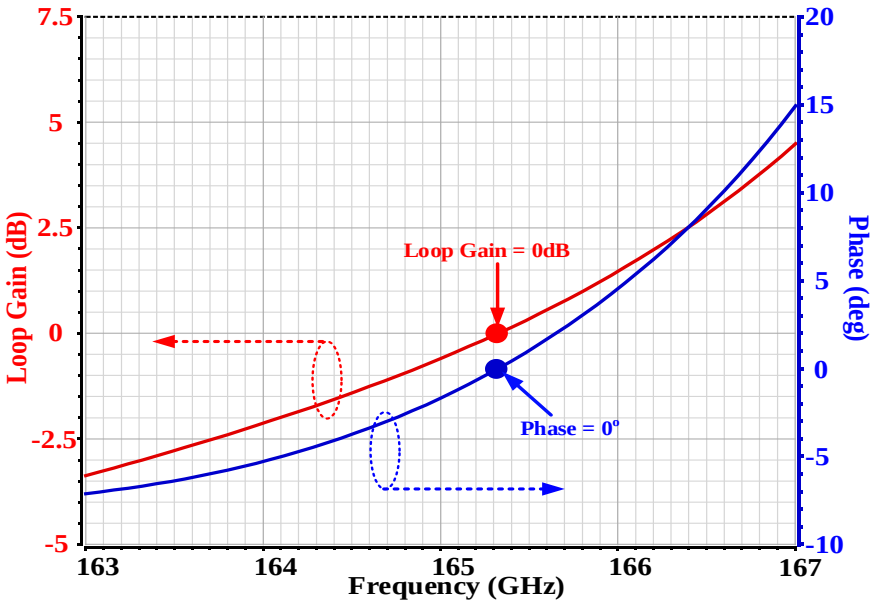

Figure 4.18: Loop gain vs frequency of the proposed VCO.

Table 4.3: Performance comparison of VCO with other designs.

References	**[57]**	**[60]**	**[61]**	**[62]**	**This work**
Technology	90nm CMOS	65nm CMOS	40 nm CMOS	65 nm CMOS	**90nm CMOS**
Supply Voltage (V)	1	1	1.8	1.5	**1**
Power (mW)	8.3	24	57.6	30	**2.82 - 2.96**
Tuning Range (GHz)	91 - 96	140.1 - 143.5	181.9 - 195.5	93.24 - 105.02	**163.25 - 172.77**
Tuning Range (%)	5.35	2.4	7.16	11.9	**5.67**
Output Power (dBm)	-8.2 - 14.1	-8	-7.26	–	**15.53 - 6.43 (differential)**
PN@1MHz (dBc/Hz)	98.3	-108.2 @ 10MHz	-97.18 @ 10MHz	-93.80 - -112.67 @ 10MHz	**-92.99 - -75.81**
FOM@1MHz (dBc/Hz)	-188.5	-140.43 @5.5GHz	-163.7	-178.6 - –177.5 @10MHz	**-192.75 - –175.84**

4.6 Chapter Summary

In this chapter, a low power, high FOM and high output power LC VCO has been proposed for D band frequency applications. In this proposed design, the transistor capacitance are used to remove the use of additional capacitor for the LC tank and varactor, which will lessens the overall silicon area consumption. The design has achieved high frequency range from 163.25 GHz to 172.77 GHz with a low power consumption of 2.8 mW to 2.9 mW for the applied tuning voltage. With the high differential output power 15.53 dBm 6.43 dBm, the VCO provides phase noise and FOM of -88.85 & -188.67 dBc/Hz@164.39 GHz. Lastly, the analysis and tabular comparison of performance's data prove the substantiality of the proposed design.

CHAPTER 5

AN AREA EFFICIENT LOW PHASE NOISE CHARGE PUMP WITH LOW PASS FILTER DESIGN

5.1 Introduction

Charge pump (CP) is a crucial building block in PLL architecture whose task is to convert the phase frequency detector (PFD) outputs, Up and Down signals to an analog signal. The output of the charge pump is fed to the loop filter to regulate the VCO frequency. A stable output voltage is a criterion when a charge pump is embedded in PLL, as the locking performance of PLL mostly depends on it. Besides, there are some significant issues in conventional charge pump like dead zone, charge sharing, current mismatch, leakage current, voltage compliance and high power consumption. CP has some prominent advantages like larger gain, perfect zero static phase error and faster frequency detecting reaction [63]. But due to some non-ideal effect charge pump shows lower performance in PLL.

One of the significant problems in PLL, as identified, is the current mismatch that is provided from PMOS and NMOS switches will create a random change in the control voltage, which as a result, leads to generate the reference spur in output. Also, the charge sharing between parasitic capacitance and filter capacitance creates a sudden change at the control voltage as a result of which VCO may become unstable. Additionally, the charge pump output voltage is still limited. Thus, for a higher voltage requirement, the current source needs to increase, which will increase power consumption.

5.2 Proposed Cascoded Single Ended Charge Pump

The basic block diagram of a standard CP is depicted in Figure 5.1. When the UP switch is active by the output of PFD, current I_{UP} charges the output node. It causes the increment of the voltage of the output capacitor, which will aid in raising the generated frequency of the VCO. Similarly, when the DN switch is active, current I_{DN} discharges the output node and with that output voltage also declines, which cause the lessening in the frequency of the VCO.

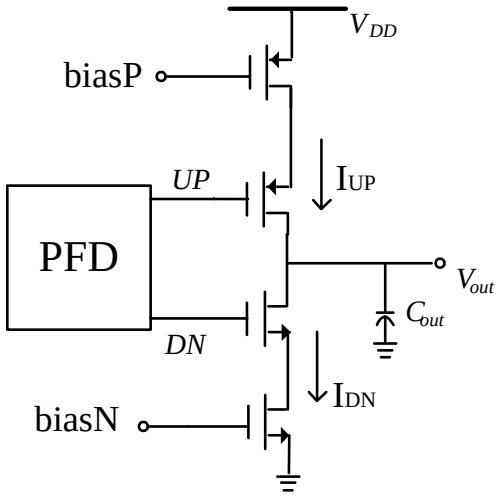

Figure 5.1: Conventional single ended charge pump.

While designing an efficient charge pump circuit, most of the researchers face a critical problem that is Current Mismatch between Up current and Down current. To overcome this problem, several techniques are applied in different topologies. One of the approaches is the employment of Op-Amp circuit, which has the problems of circuitry's complexity and excess area, power. Another approach is to embed a cascade technique that facilitates to raise output resistance along with a significant reduction of current mismatch. The simplicity of circuitry's configuration can be achieved by implementing the cascade technique with a limited number of transistors. Furthermore, overall silicon area and excessive power consumption can be abated in a noteworthy

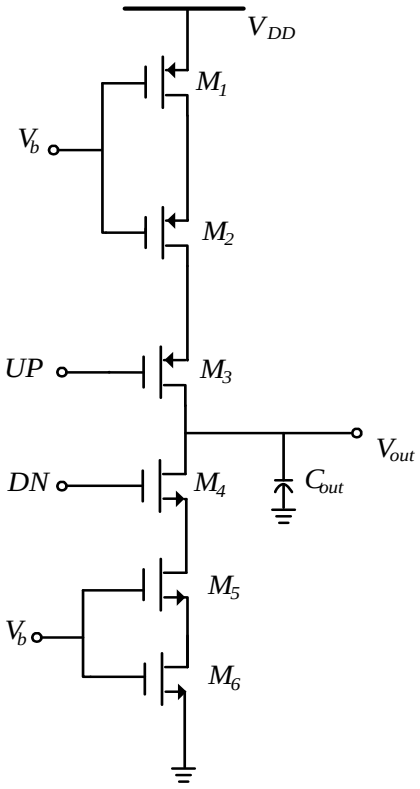

Figure 5.2: Proposed cascode single ended charge pump.

amount. In this proposed design shown in Figure 5.2, M_2 and M_5 MOSs are connected in cascade with M_1 and M_6 work as current source and M_3 & M_4 are the UP switch and DN switch, respectively. UP and DN signals are provided from the PFD outputs. When the UP signal is active, the charging current starts to flow and charge the output capacitor Cout. Similarly, when the DN signal is active, it discharges the output capacitance through M_4, M_5 and M_6. On this circuit, negative gain is provided by the cascade MOSs (M_2 & M_5). Table 5.1 provides the aspect ratios (W/L) for all the MOSFETs.

Table 5.1: W/L ratios for the used MOSs.

MOS	W/L Ratio
M_1, M_2 & M_3	6 $\mu/600n$
M_4, M_5, & M_6	4.2$\mu/810n$

The cascaded transistors (M_2 & M_5) helps to add additional output resistance as

well as reduce the current mismatch. The output resistance of the cascode is given in Eq. (5.1).

$$R_{out} = g_{m2} r_{02} r_{01} (1 + A) \tag{5.1}$$

Here, r_{01}, r_{02} are the resistance of MOS (M_1 & M_2), g_m is the trans conductance of the cascade transistor and A is the gain of the cascode circuit.

5.3 Simulation and Results Analysis

The proposed charge pump has been simulated in gpdk 90nm CMOS process technology within virtuoso cadence environment. To analyze the performance parameters such as current mismatch, transient up and down voltage, power consumption and phase noise DC analysis, transient analysis, pss, and pnoise analysis have been steered. Moreover, temperature swept analysis, process corner analysis and Monte Carlo analysis have been executed to appraise the proposed design's robustness. The proposed charge pump consumes 34.0965 μW power at 27°C with a phase noise -126.9dBc/Hz at 10MHz offset. The overall performance is discussed with the simulation graph in this section.

Figure 5.3 shows the current mismatch between UP current and DN current due to consecutive switching of M_3 and M_4 whose gate input is fed from the output of PFD. A trivial amount of current mismatch can be noticed from the 0.3V to 0.7V range is zero. So efficient performance with respect to the non-linear parameter i.e current mismatch, can be observed within this range. A mere cascade technique has propelled to achieve this inconsequent amount of current mismatch. In Figure 5.4, charging current is depicted, which is simulated by setting UP current active and deeming the down circuit open. As a results, the current stem from the supply voltage due to short circuited path of UP circuit will charge the output capacitor. It can be illustrated from the graph that upto 0.6V the charging current (34μA) is unwavering; however, a drastic

diminution of charging current can be noticed after the subsequent values of voltage.

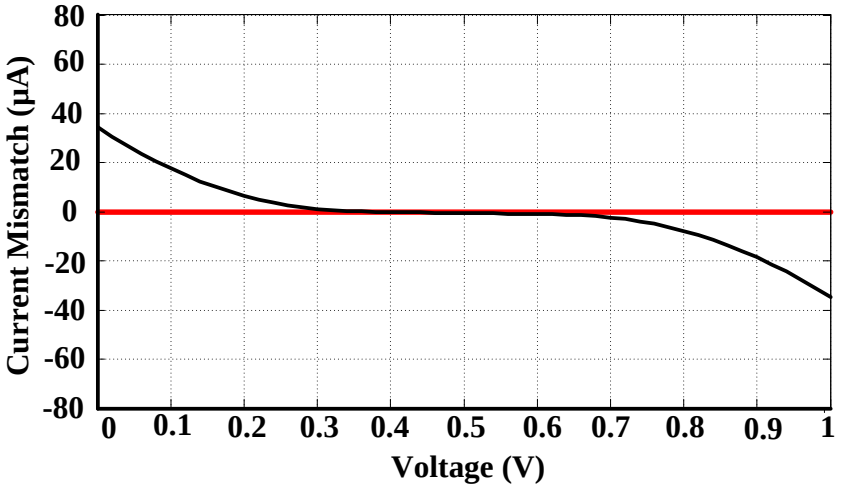

Figure 5.3: Current mismatch between UP and DN signal with the variation of voltage.

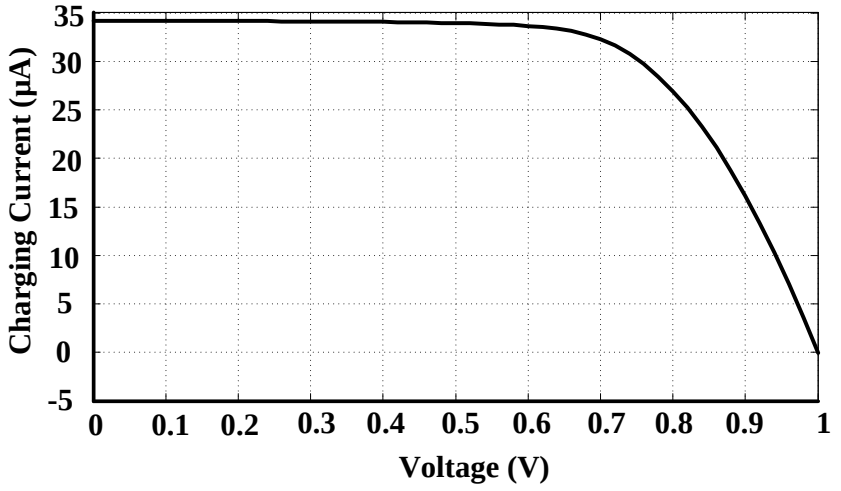

Figure 5.4: Charging current *vs* Voltage of the proposed charge pump.

Additionally, Figure 5.5 represents the discharging current due to the active DN circuit while the UP circuit is kept open. At that time the output capacitor starts to discharge through M_4 transistor. From the simulated graph, it is observed that up to $.4$V the DN circuit current is decaying; after that it starts to become more stable to -35μA.

Figure 5.6 represents the transient output voltage when pulse input is provided to the UP terminal - making it active, while the DN terminal is fixed at 0V to turn off the

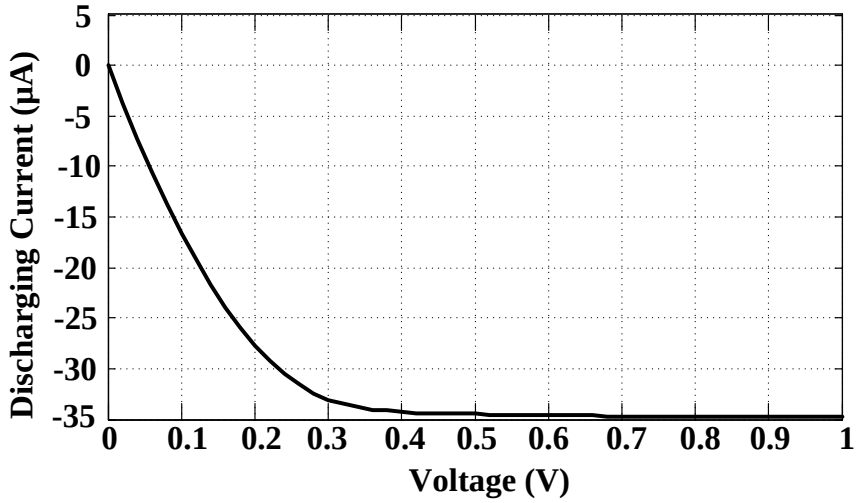

Figure 5.5: Discharging current *vs* Voltage of the proposed charge pump.

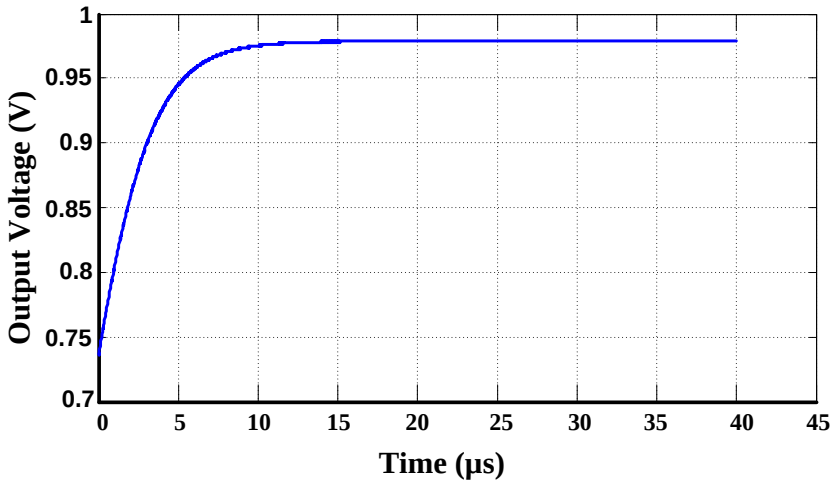

Figure 5.6: Output voltage with respect to time when UP signal active.

down circuit. After 10μS time, output voltage saturates to nearly 1V. Figure 5.7 also shows the output transient voltage when the state of the charge pump is in the converse situation of as previously considered. A stable value close to 0V after $15\mu s$ time is provided by the proposed charge pump circuit. Output noise is plotted in Figure 5.8 of the proposed CP where at 1GHz frequency output noise got the spur -116.1dBc/Hz.

Phase noise is observed for the proposed charge pump considering cascade and without cascade that is plotted in Figure 5.9. For both, the cases at 1GHz spur is

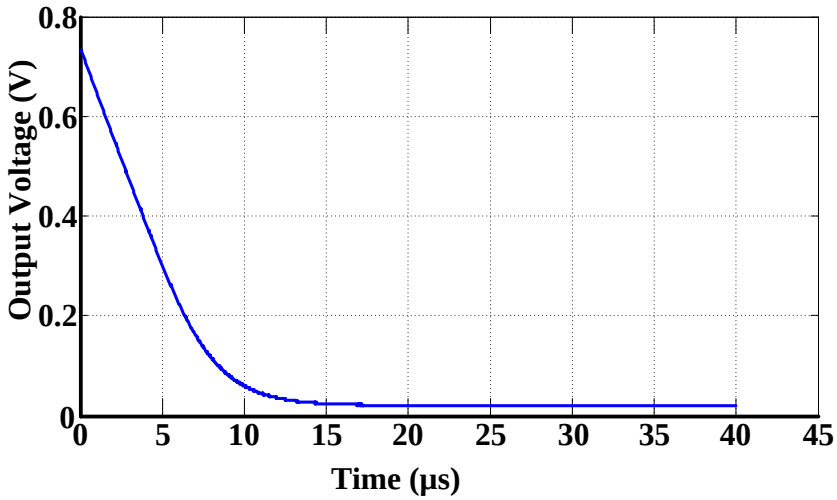

Figure 5.7: Output voltage with respect to time when DN signal active.

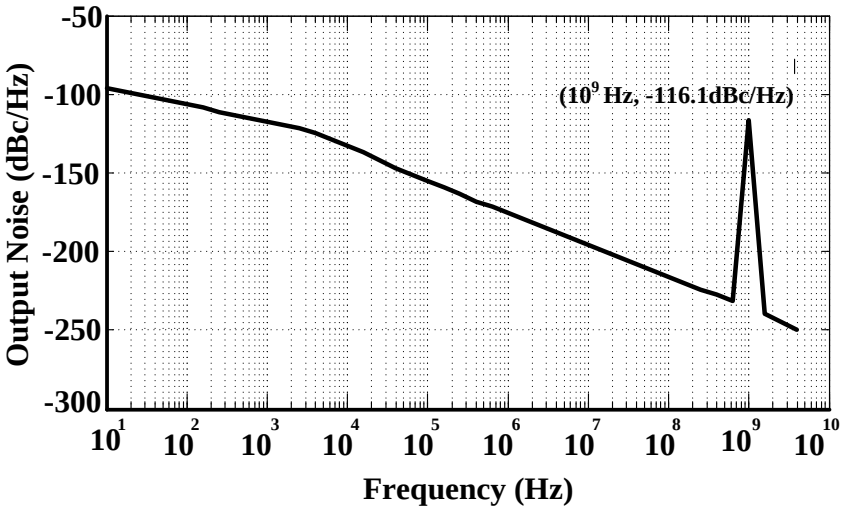

Figure 5.8: Output noise of the proposed Charge Pump.

observed. Phase noise is -126.9dBc/Hz @ 10MHz offset, which is significantly low. This is because the proposed design has tried to focus on a good outcome using a minimal number of the transistor, which are the source of phase noise.

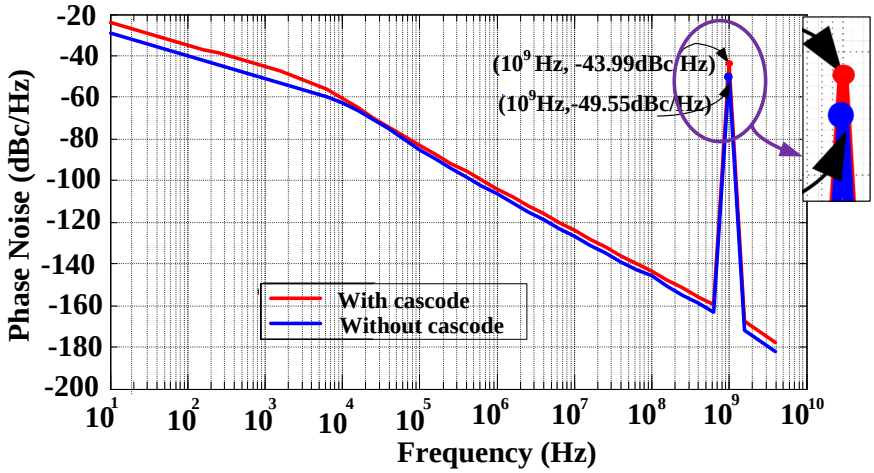

Figure 5.9: Phase noise of the proposed Charge Pump.

5.3.1 Temperature swept analysis

MOSFETs are sensitive to temperature due to their atomic structure. The mobility and threshold voltage of MOSFET will vary with the variation of temperature. So the proposed CP needs to be consistency with the temperature's variation. In this analysis, five different temperature environment ranges from -50°C to 50°C (with 25°C interval) is setup to evaluate the performance of the proposed CP. Fom Figure 5.10, 5.11, 5.12 and 5.13 it is obvious that the temperature variation hardly impacts the behavior of the CP. UP and DN current mismatch is almost the same for all the temperature environments with the variation of the supply voltage. The UP transient output voltage shows the similarity in spite of the variation of temperature. The state of DN transient output voltage has some deviation but at the time of stable, all the values are temperature invariant. Similarly, initially, the phase noise shows some aberration; after a certain frequency, the characteristics of CP shows the sustainability of phase noise with temperature variations. Power consumption is remaining almost the same with the variation of temperature illustrated in Table 5.2.

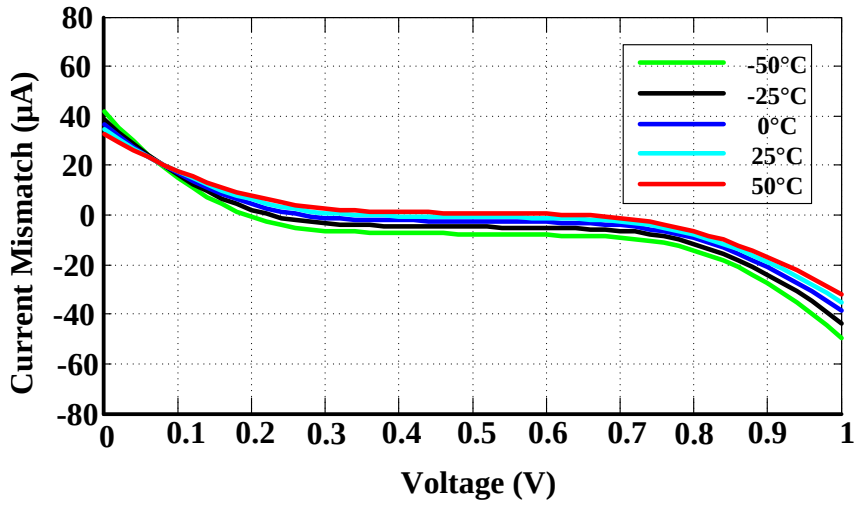

Figure 5.10: Current mismatch at different temperature.

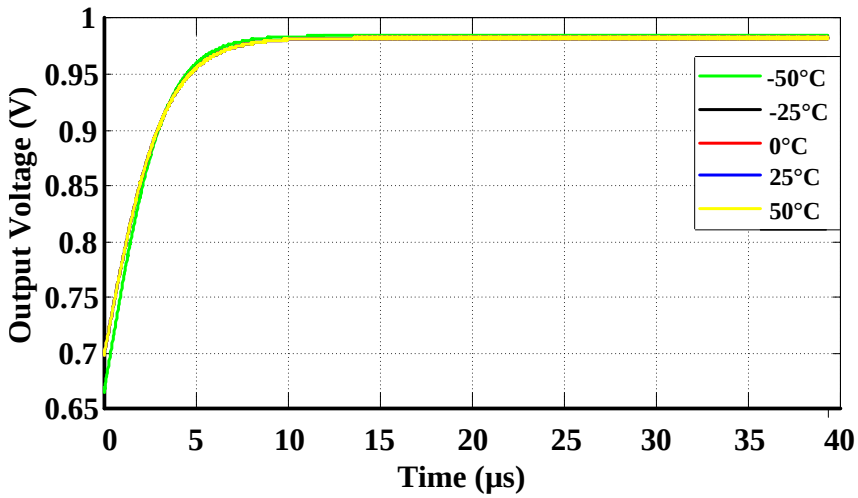

Figure 5.11: Output voltage at different temperature with active UP signal.

Table 5.2: DC power consumption with temperature

Temp(°C)	Power consumption
-50	41.6125 μW
-25	38.6112 μW
0	36.2221 μW
25	34.2463 μW
50	31.8162 μW

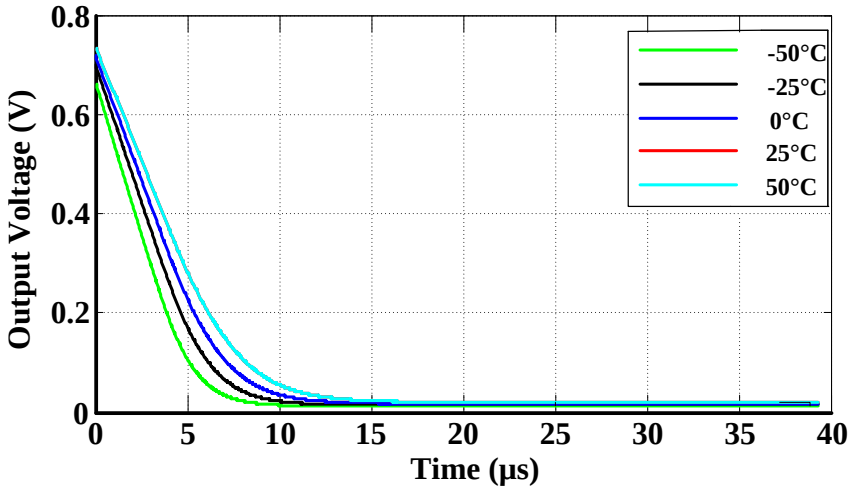

Figure 5.12: Output voltage at different temperature with active DN signal.

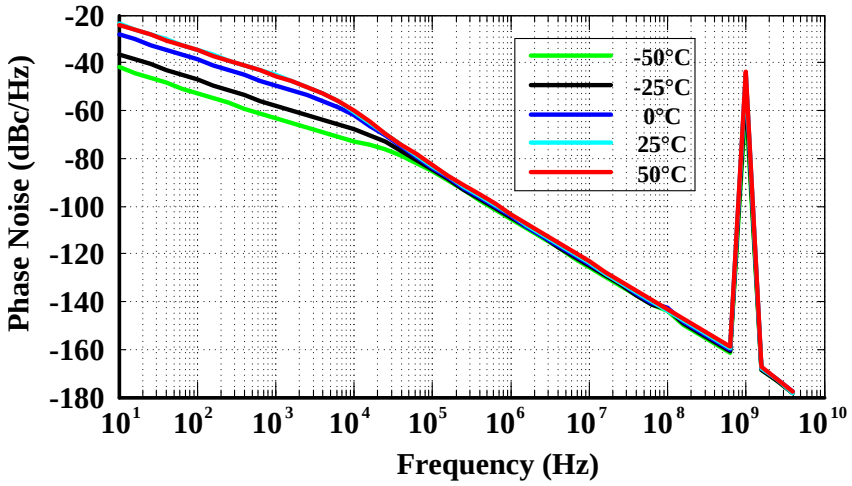

Figure 5.13: Phase noise at different temperatures.

5.3.2 Process corner analysis

To verify the robustness of a semiconductor device process corner analysis is a must. Deviation in doping concentration or oxide thickness parameters of MOSFET may have some non-linearity effect or change the process parameters. To ensure the sustainability of a circuit, it must be consistent with the variation of process corner (fast corner and slow corner). In CMOS technology process corner variation is taking place for NMOS and PMOS. With the variation of the speed of MOSs the process

corner variation can be SS (slow NMOS and slow PMOS), SF (slow NMOS and fast PMOS), FS (fast NMOS and slow PMOS) or can be FF (fast NMOS and fast PMOS).

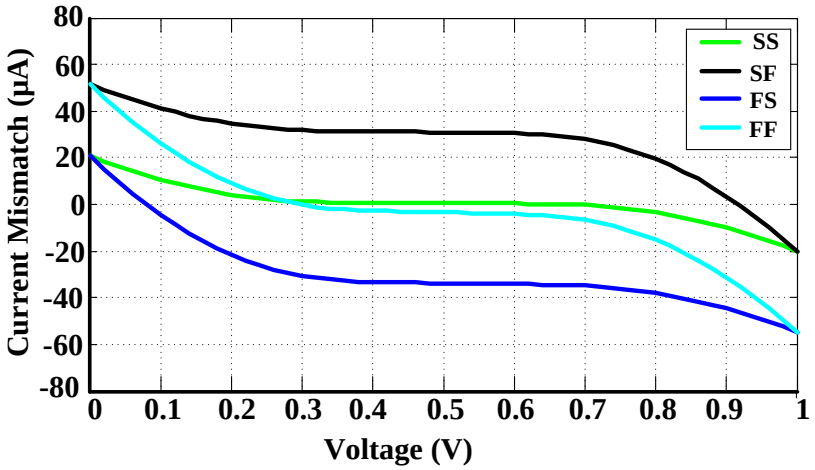

Figure 5.14: Simulated Current Mismatch at different corners.

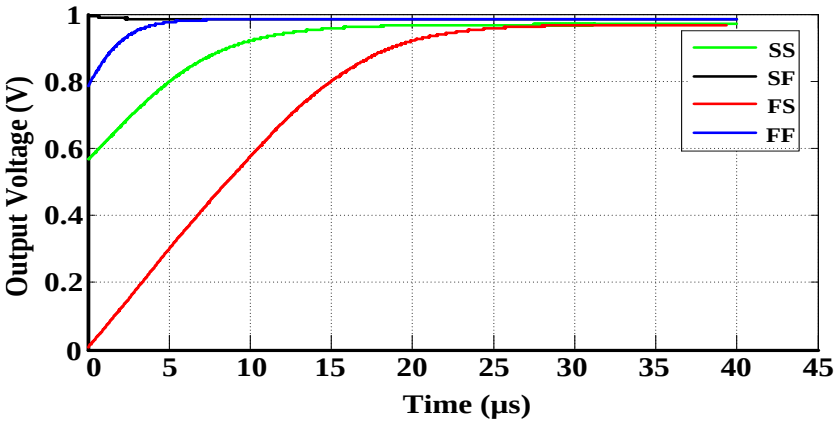

Figure 5.15: Output voltage with temperature at different corners for active UP signal.

To show the tolerance of the proposed CP simulated through all these process corner analyses. From Figure 5.14 it is noticed that for SS current mismatch is entirely zero and for FF current mismatch is near to zero. But for the other corners significant current mismatch is observed. Figure 5.15 and 5.16 also represent that at the initial time, the output voltage (due to charging current and discharging current) fluctuates for a different corner but after a certain time, a steady state value of output voltage

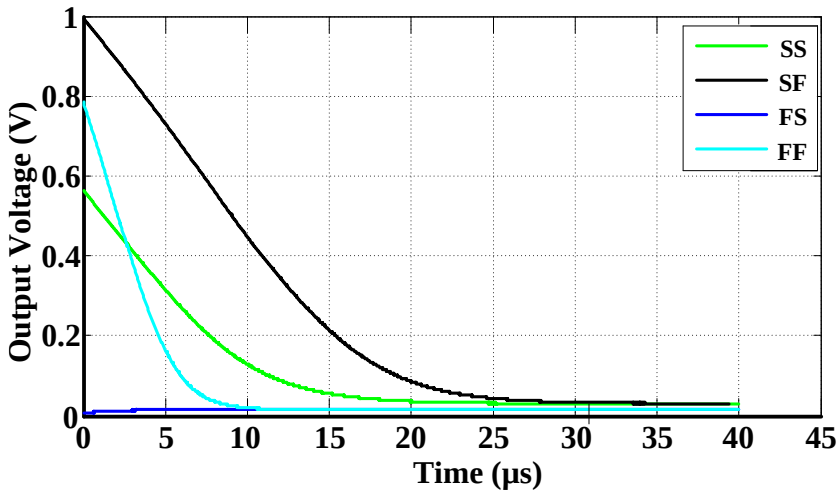

Figure 5.16: Output voltage with temperature at different corners for active DN signal.

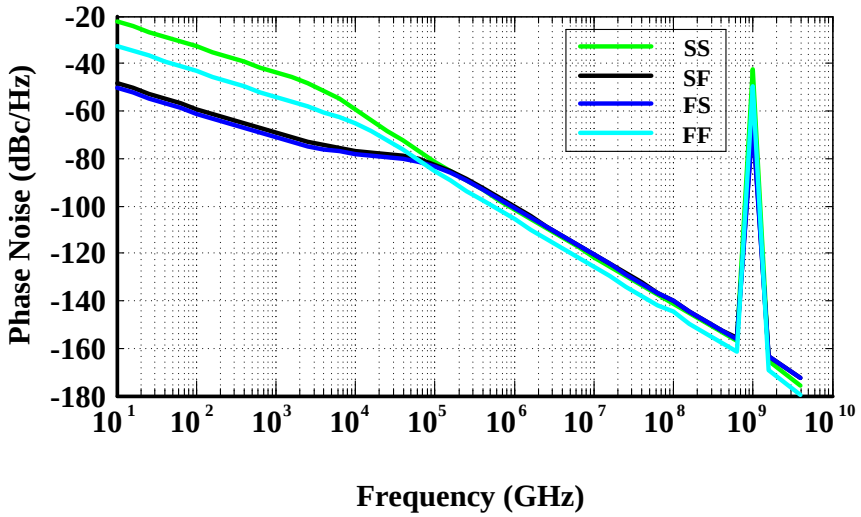

Figure 5.17: Phase noise of the proposed CP at different corners.

can be observed. The required time for steady state output voltage of UP transient is minimum for SF while FS for DN transient. Phase noise with the process corner variation (SF and FS) at lower frequency show similar behavior where SS and FF differ but with the increase of frequency all the process corner shows the similar graph in Figure 5.17. The poor spur is observed for SS process corner. Table 5.3 represents the variation of power consumption, considering all the process corner environment.

Table 5.3: DC power consumption with corners.

PVT	Power consumption
SS	20.0342 μW
SF	20.0645 μW
FS	20.6384 μW
FF	51.2216 μW

5.3.3 Monte Carlo analysis

The Monte Carlo analysis is a risk management technique that calculates the probability and distribution of risk or uncertainty. Considering both the process variation and mismatch cases, simulation performed for the proposed CP. Figure 5.18 and 5.19 show the statistical representation of phase noise at 1MHz offset and DC power consumption, respectively, for 100 no of samples. For the case of phase noise, mean value -103.856dBc/Hz observed where the standard deviation is 42.83mdBc/Hz. Similarly, for DC power consumption mean value 33.897μW having a lower standard deviation 270.4nW is achieved by the proposed CP.

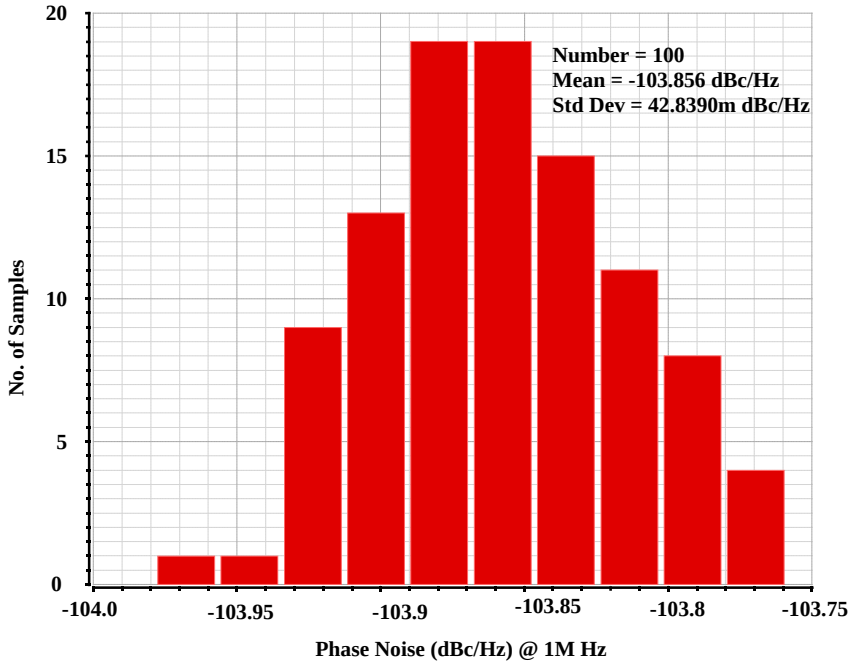

Figure 5.18: Statistical distribution of phase noise of the proposed design.

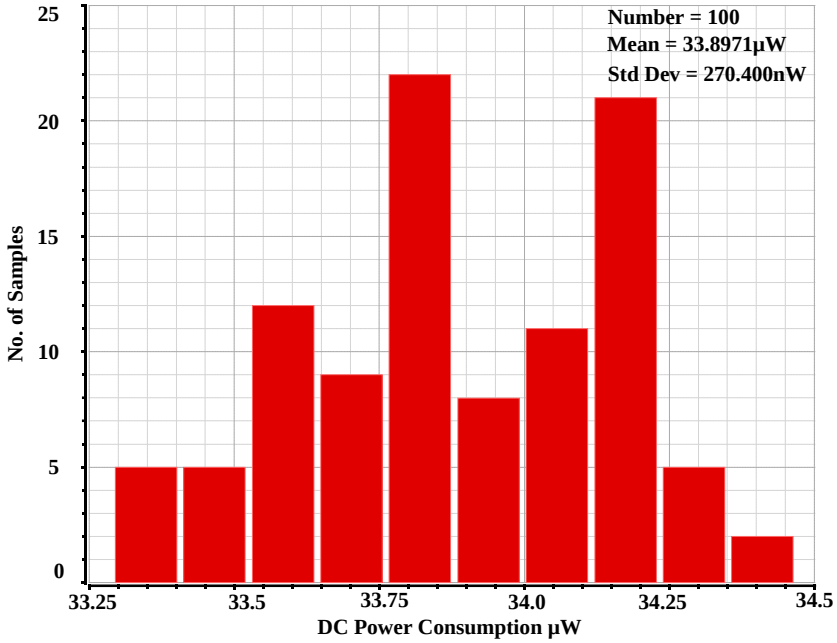

Figure 5.19: Statistical distribution of the parameters of the proposed design.

5.4 Performance Comparison

Finally, the proposed design has been compared with other referred models based on fundamental performance parameters in Table 5.4. It can be concluded that the proposed design outdoes other cited designs in terms of power dissipation, phase noise and silicon area.

Table 5.4: Performance Comparison of proposed CP.

References	Ref. [64]	Ref. [65]	**This work**
CMOS Technology	90nm	90nm	**90nm**
Supply Voltage (V)	1.2	1.2	**1**
Power Dissipation (μW)	134.7	404	**34.0965**
PN@ 10MHz (dBc/Hz)	-102.5	-104.601	**-126.9**
No of transistors	8	18	**6**
Layout Area(μm^2)	234.5	101.07	**275.28**

5.5 Layout

The layout view of the proposed charge pump is shown in Figure 5.20. Metal1 and pollysillicon has been used for interconnecting purpose. The input/output pins are also indicated. The entire layout shows that it has an area consumption of 15.83 μm$\times$ 17.39 μm. It can be concluded that the core charge pump circuit dissipates very small area with respect to whole PLL circuit.

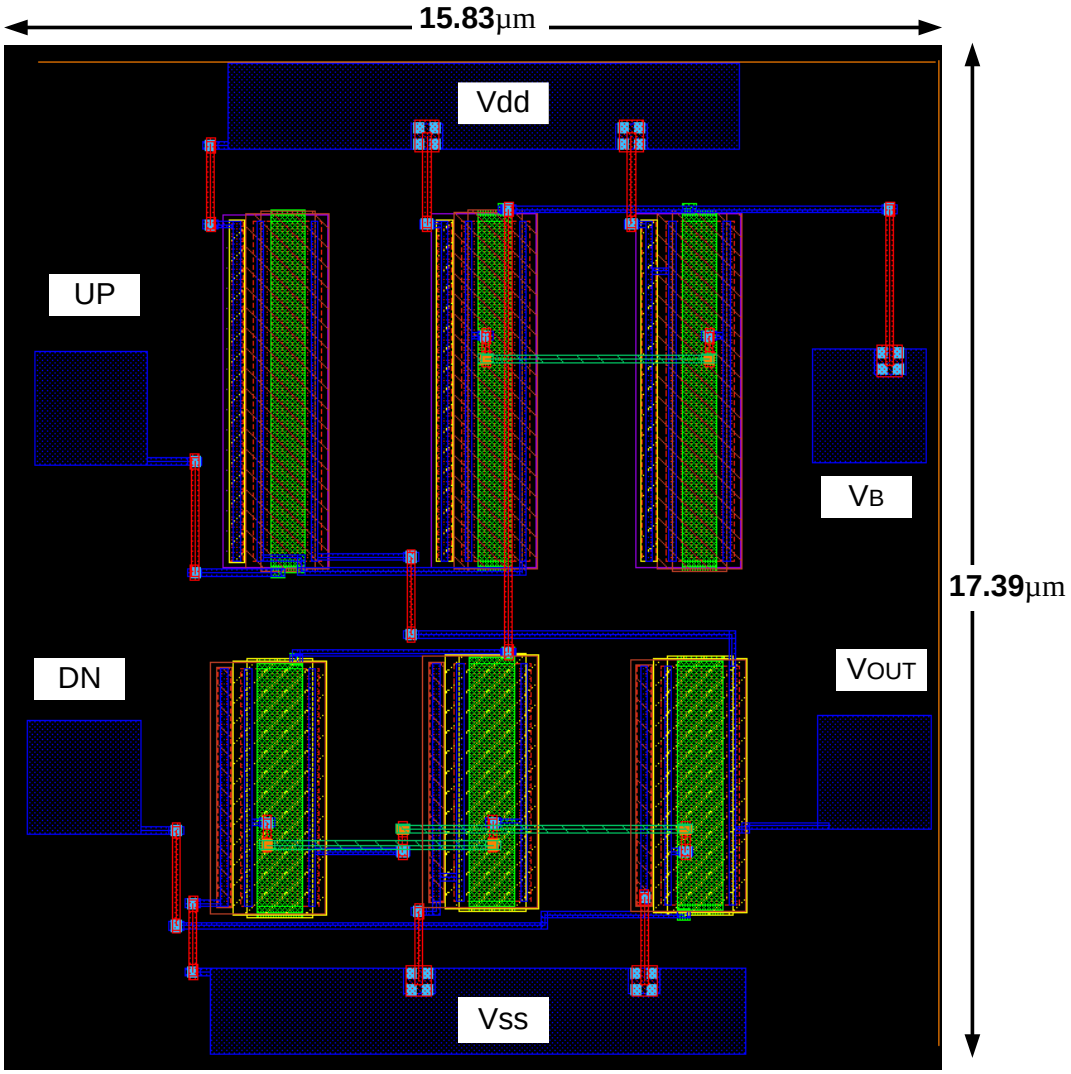

Figure 5.20: Layout of proposed charge pump.

5.6 Post Layout Simulation

To observe the real performance of a circuit Layout based simulation is required. In schematic simulation only transistors are considered, but at the time of fabrication some parasitic capacitance, inductance and resistance are generated. Due to the presence of these parasitic capacitance, inductance and resistance the performance of the circuit may vary from the schematic simulation.

In this proposed Charge Pump after the post layout simulation current mismatch,

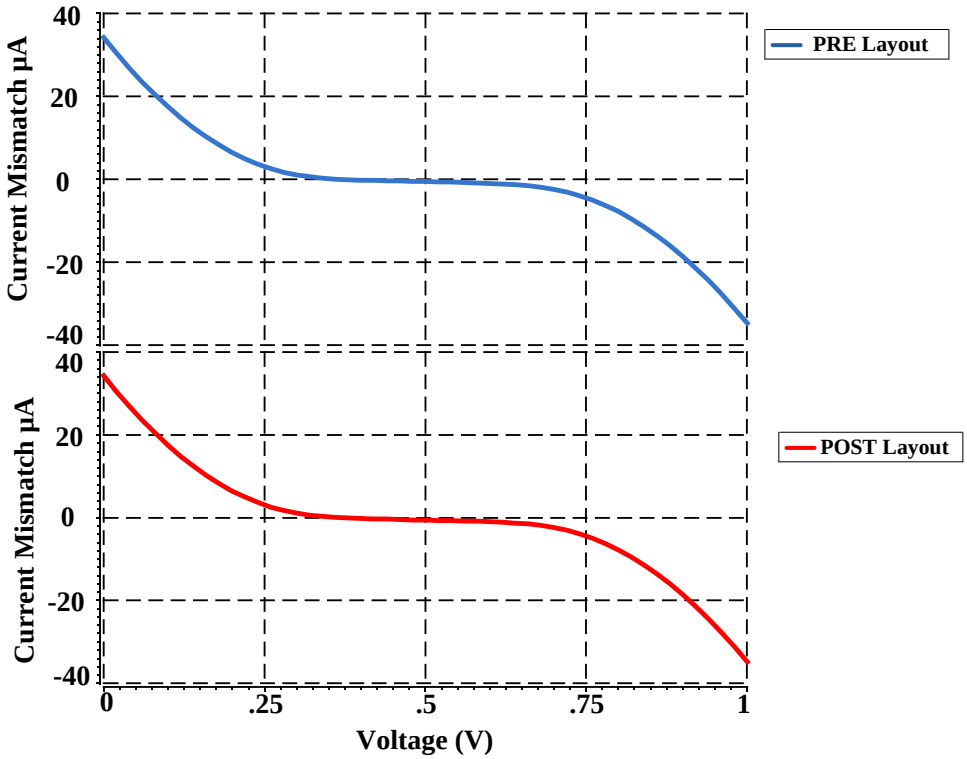

Figure 5.21: Current Mismatch from post Layout simulation

charging current and discharging current are same as the transistor based simulation which is shown in Figure 5.21, 5.22 and 5.23 respectively. A little deviation is observed in the case of output noise and phase noise at higher frequency which is depicted in Figure 5.24 and 5.25.

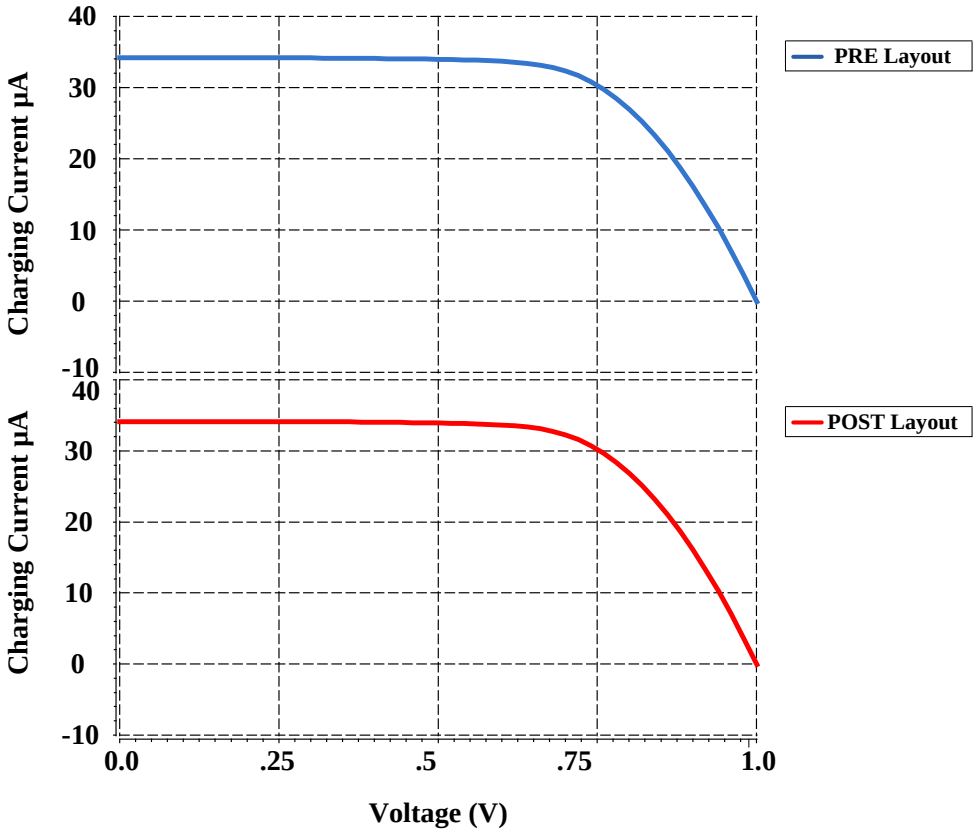

Figure 5.22: Charging Current from post Layout simulation

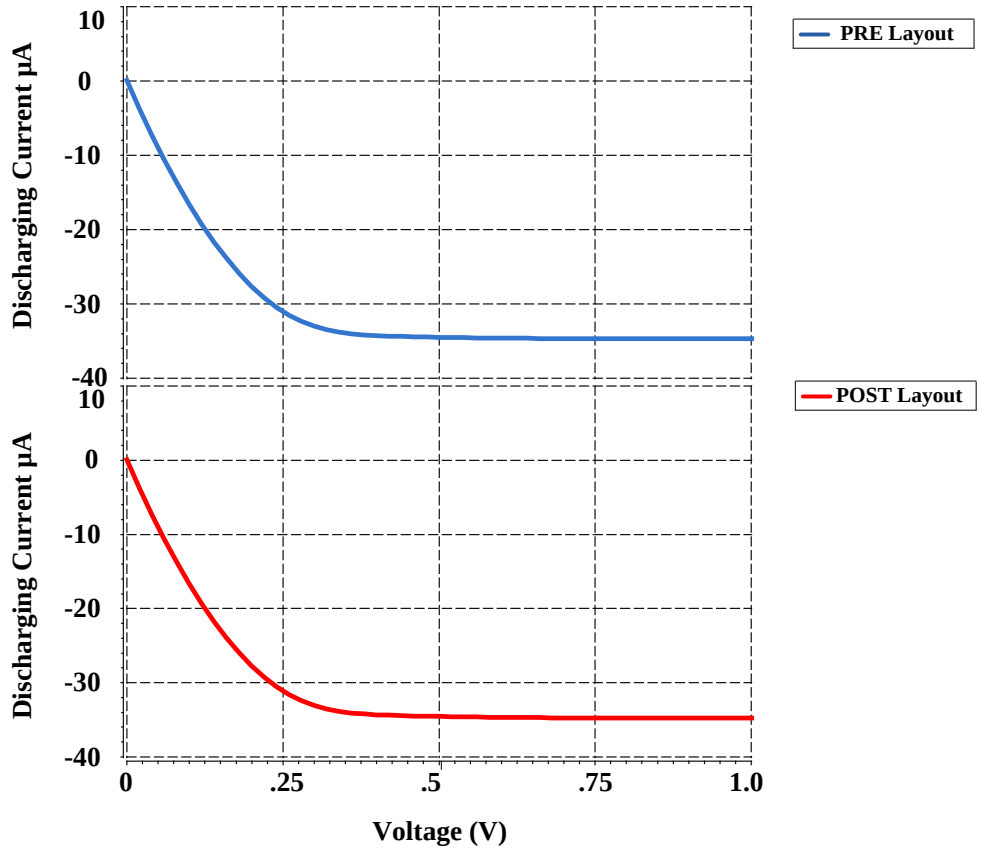

Figure 5.23: Discharging Current from post Layout simulation

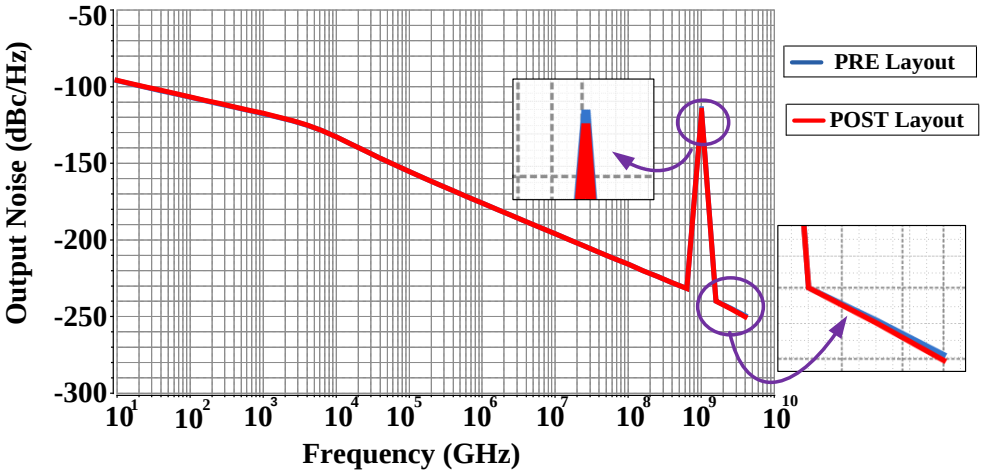

Figure 5.24: Output Noise from post Layout simulation

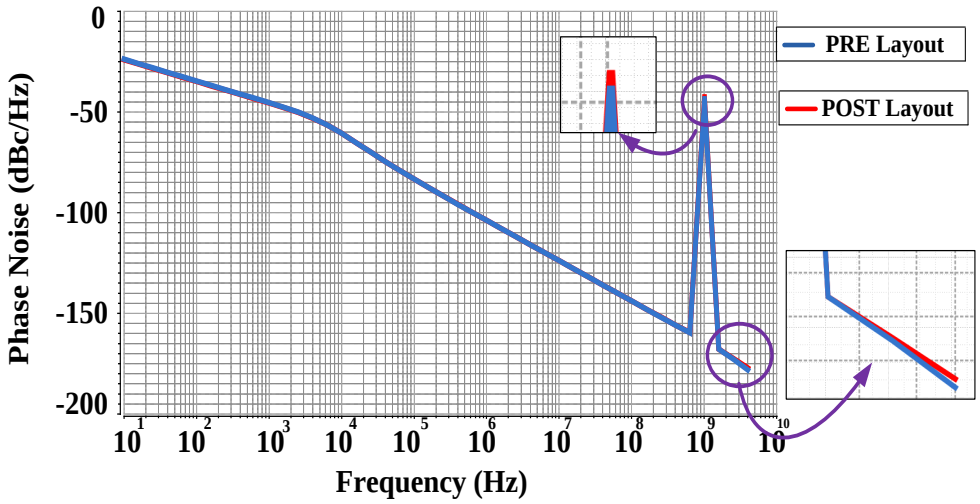

Figure 5.25: Phase Noise from post Layout simulation.

5.7 Chapter Summary

A simplified low power charge pump is presented in this chapter, which is capable of reducing the nonlinear effects *i.e.* current mismatch, power consumption and phase noise. Implementing a cascade technique, the proposed charge pump is simulated in gpdk $90nm$ CMOS cadence virtuoso environment. The simulation results demonstrate that the proposed circuit consumes $34.0965\mu W$ from 1V power supply. The design has achieved phase noise $-126.9dBc/Hz$ at $10MHz$ offset with a very small layout area $275.28\mu m^2$. Lastly, with all this analyzation and tabular comparison of performance data, the improvement of the proposed design is achieved.

CHAPTER 6

AREA EFFICIENT LOW POWER FREQUENCY DIVIDER AND PHASE FREQUENCY DETECTOR FOR PLL

6.1 Introduction

Another two indispensable blocks of PLL are frequency divider and phase frequency detector. Frequency dividers have promised many potential applications in microwave/millimeter wave systems. Among the classic examples are applications involving straight frequency counting as well as phase-locked loops. Further applications lie in the area of electronic ware; where the ability of the divider circuit to compress bandwidths can be exploited in the processing of wide band signals.

Similarly, phase-frequency detector is the principal block of phase locked loop and delay locked loop. PFD behaves as a comparator which correlates the phase of the input signal along the output signal of Phase locked loop. The purpose of phase detector is to produce a signal whose average value is analogous to the transformation between the phase of input signal and the output signal. PFD creates a signal that is the difference in terms of phase among two signals and is a DC voltage. PFD results are employed to restraint the output of a charge pump circuit. CP converts the phase detector output into a voltage controlled output. This chapter contains an efficient design of frequency divider and phase frequency detector which will be applied for further development of a highly performed PLL.

6.1.1 Frequency divider (FD)

There are several types of circuits that can perform frequency division according to the requirements, however, none of the circuits meet all the requirements simultaneously. Some of the basic requirements for designing Frequency Divider are listed below,

– high operating frequency,

– wide range of operation,

– high division ratio,

– variable and controllable division ratio,

– no RF signal in the absence of input signal,

– low cost

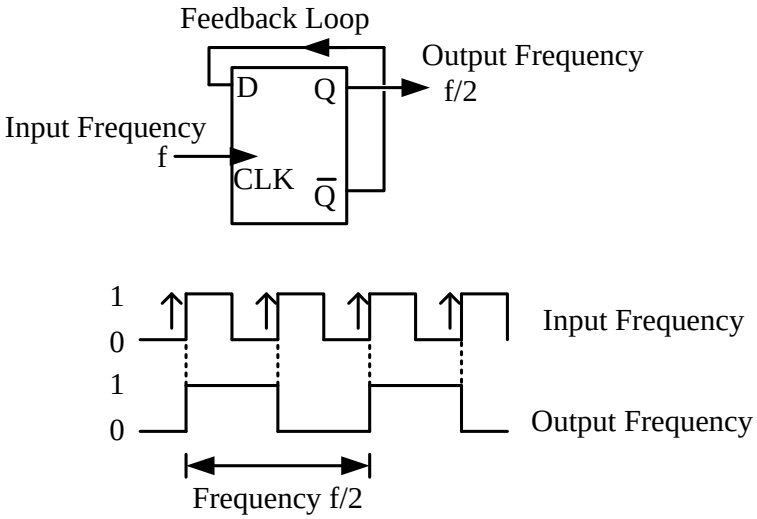

Figure 6.1: Basic Frequency Divider divide-by-2.

D FF based frequency divider circuit are widely used to generate f/N according to the requirement of frequency specified PLL. One of the most useful features of the D-type Flip-Flop is as a binary divider, for Frequency Division or as a divide-by-2 counter. Here the inverted output terminal Q (NOT-Q) is connected directly back to the Data input terminal D giving the device feedback as shown in the Figure 6.1.

In a PLL synthesizer, of all the PLL components, circuit design of the VCO and the frequency divider is very critical. The reason partly is these components operate at the highest frequencies within the PLL and also consume most of the power as compared to the other components. As part of this thesis, a digital frequency divider based on True Single Phase Clocking (TSPC) has been designed which generates half of the frequency received from the output terminal of PLL.

6.1.2 Phase frequency detector (PFD)

These special detectors are allowed to detect both phase and frequency difference proves extremely useful because it significantly increases the acquisition range and lock speed of PLLs. Unlike multipliers and XORs, sequential phase/frequency detectors (PFDs) generate two outputs that are not complementary. The operation of a typical PFD is illustrated in Figure 6.2.

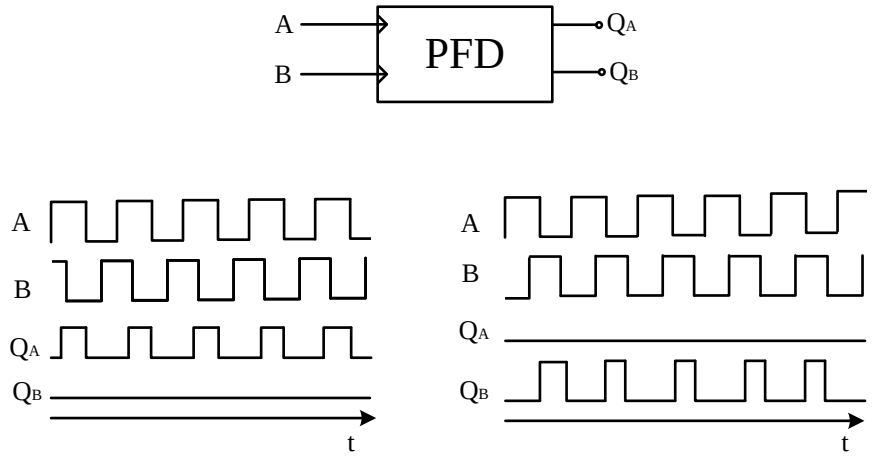

Figure 6.2: Operation of a typical PFD.

It works as follows: If the frequency of input A is greater than that of input B, then the PFD produces positive pulses at Q_A, while Q_B remains zero. Conversely, if frequency in input B is greater than in A, positive pulses appear at Q_B while Q_A= 0. If both frequencies are equal, then the circuit generates pulses at either Q_A and Q_B with

a width equal to the phase difference between the two inputs. Thus, the average value $Q_A - Q_B$ is an indication of the frequency or phase difference between A and B. The outputs Q_A and Q_B will be called UP and DOWN signal, respectively. According to all of this, in case that REF is a little bit higher than VCO, the subtraction UP-DOWN will be positive. And, the control signal that arrives at the VCO system, will force it to increase its output frequency. In contrast, if VCO is higher than REF, this subtraction will be negative and it will produce the contrary effect.

6.2 Implemented Frequency Divider

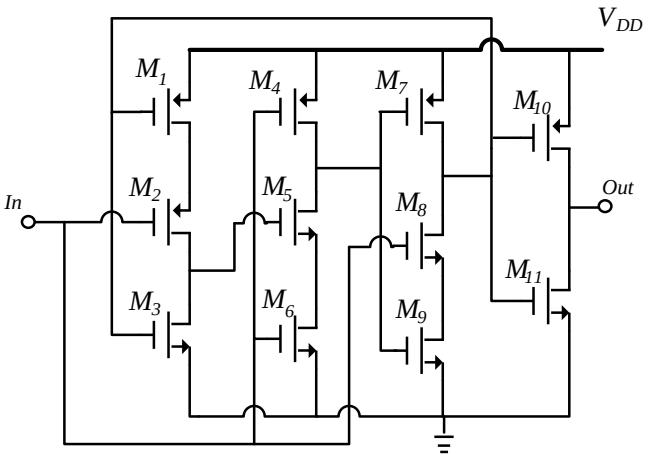

Figure 6.3: Schematic of the implemented Frequency Divider.

Frequency divider is used to divide down the frequency of local oscillation to reference signal. It is important because on-chip oscillation is much faster (GHz) than reference. The model is a D flip-flop. In any flip-flop, when a continuous train of pulse waveforms at fixed frequency is fed to it as an input signal, an output signal of approximately half the frequency of the input signal can be obtained. Here in Figure 6.3 the frequency divider by implementing a D-Flip-Flop with $\bar{Q}$ attached to D. The output (Q) frequency is then half the input (CLK).

The implemented D flip-flop has been constructed with dynamic circuits (where

information is stored in a capacitance) as long as it is clocked often enough; while not a true flip-flop, it is still called a flip-flop for its functional role. While the masterslave D element is triggered on the edge of a clock, its components are each triggered by clock levels. The ”edge-triggered D flip-flop”, as it is called even though it is not a true flip-flop, does not have the masterslave properties.

This design of dynamic flip flops also enables simple resetting since the reset operation can be performed by simply discharging one or more internal nodes. A common dynamic flip-flop variety is the true single-phase clock (TSPC) type which performs the flip-flop operation with little power and at high speeds. However, dynamic flip-flops will typically not work at static or low clock speeds; given enough time, leakage paths may discharge the parasitic capacitance enough to cause the flip-flop to enter invalid states. The selected W/L ratios for the implemented transistors are given bellow in Table 6.1.

Table 6.1: W/L ratios for the used MOSs in FD.

MOSs	W/L Ratio
M_1, M_2, M_4, M_7 & M_{10}	$360n/100n$
M_3, M_5, M_6, M_8, M_9 & M_{11}	$180n/100n$

6.2.1 Working principle of implemented FD as DFF

For the Figure 6.4, first consider the two cases of CLK = 0 and CLK = 1. Replacing the CLK transistors with ideal switches (Figure 6.5), the following two cases can be illustrated:

When CLK is Low:

$A = \bar{D}$

$B = 1$

$Q_b = hold$

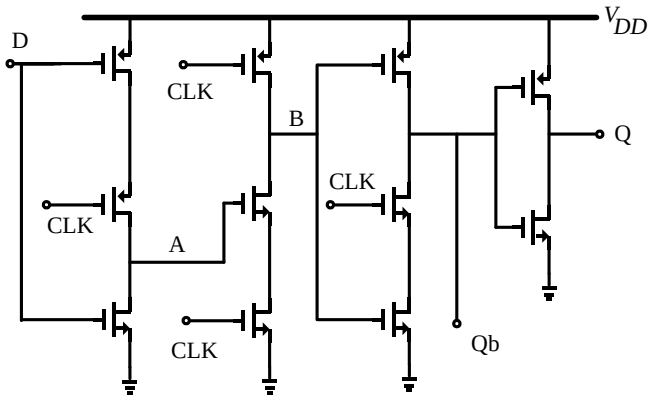

Figure 6.4: Circuit diagram of DFF using CMOS logic.

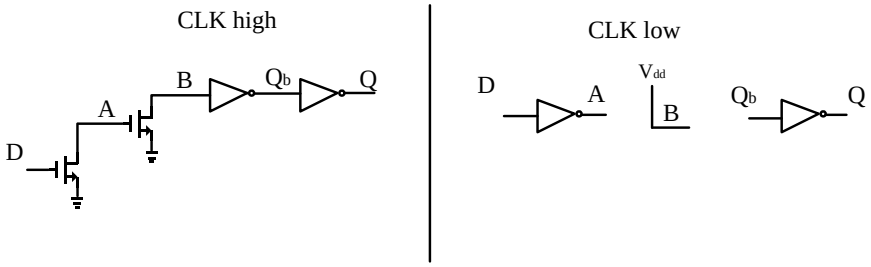

Figure 6.5: Operation of DFF.

$Q = \bar{Q_b}$

When CLK is High:

$Q_b = \bar{B}$

$Q = \bar{Q_b}$

if D $= 1$:

$A = 0$

$B = hold$

if D $= 0$:

$A = hold$

if $A = 1, B = 0$

if $A = 0, B = hold$

This matches the normal behavior of D flip flop It can be notice that changes to D

cannot affect Q when the clock is static high or static low. On the low-to-high transition of CLK (assuming D is steady), it can examine the two cases based on the state of D:

CLK $= 0 \rightarrow 1, D = 0$

$A = 1$

$B = 1 \rightarrow 0$

$Q_b = Q'_b \rightarrow 1$

$Q = \bar{Q}'_b \rightarrow 0$

CLK $= 0 \rightarrow 1, D = 1$

$A = 0$

$B = 1$

$Q_b = Q'_b \rightarrow 0$

$Q = \bar{Q}'_b \rightarrow 1$

So, this does appear to function as a normal flip-flop [66].

6.3 Implemented Phase Frequency Detector Circuit

The PFD functions by comparing the reference and VCO signal. It has 3 states-a hold state where neither the up or down signal is on, an up state to signal charging of the output control voltage, and a down state to signal discharging of the control voltage. The PFD closely follows the functionality of the state machine shown in Figure 6.6 (Here, 'out' is the VCO signal). When frequency of CK_{ref} is equal to frequency of CK_{out} both the outputs that is Up and Down are zero, if CK_{ref} is high compared to CK_{out} Then up signal is high else down signal is high indicating the phase error between CK_{ref} and CK_{out} The conditions of inputs and outputs are depicted in state machine diagram.

PFD compares the phase of local oscillation to that of reference signal. It detects the phase difference and output error voltage which is used to direct the charge pump to

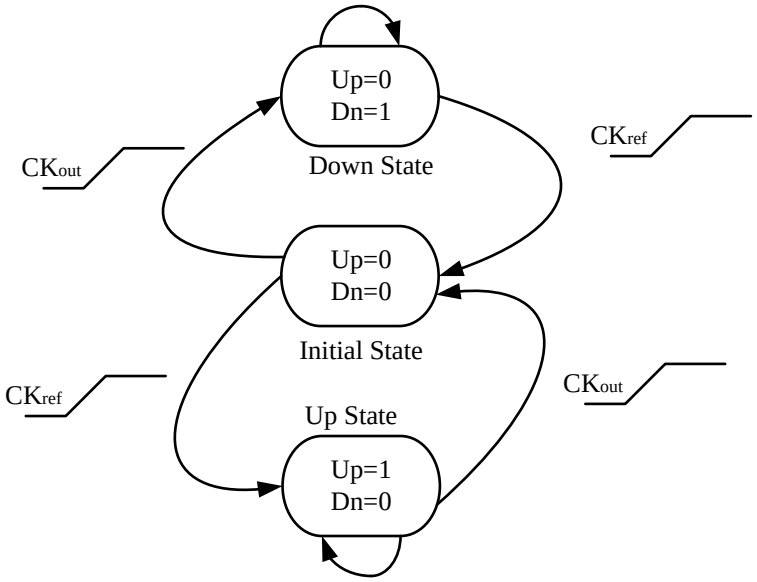

Figure 6.6: The Finite State Machine for the PFD.

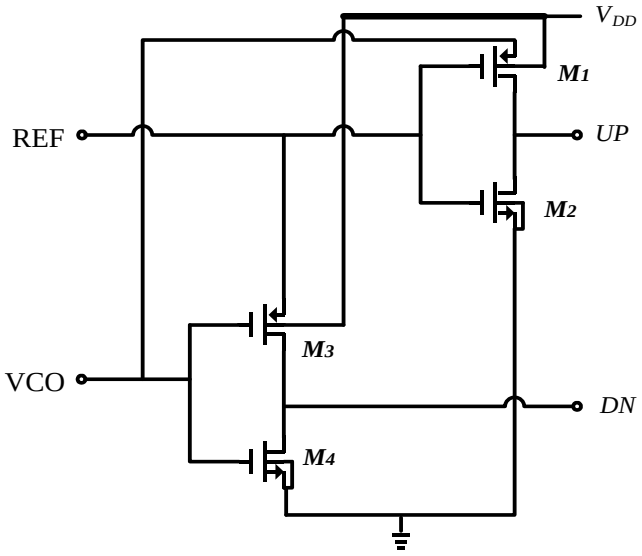

Figure 6.7: Implemented Circuit of PFD.

Table 6.2: W/L ratios for the used MOSs in PFD.

MOSs	W/L Ratio
M_1	$360n/100n$
M_2	$160n/100n$
M_3	$300n/100n$
M_4	$150n/100n$

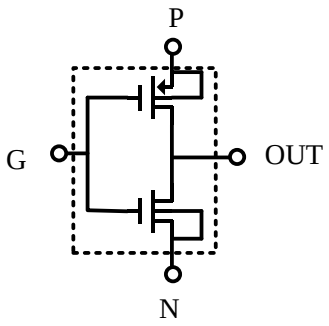

Figure 6.8: GDI cell.

charge/discharge loop filter. Implemented schematic of the PFD is shown in Figure 6.7 and the size of the transistors in this circuit is listed in Table 6.2.

Table 6.3: Logical function of GDI cell.

N	P	G	OUT	FUNCTION
0	B	A	$A'B$	F1
B	1	A	$A' + B$	F2
1	B	A	$A + B$	OR
B	0	A	AB	AND
C	B	A	$A'B + AC$	MUX
0	1	A	A'	NOT

This PFDs is basically constructed with two GDI (Gate Diffusion Input) cells. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low power circuits, using reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple Shannons theorem-based design by using small cell library. A basic GDI cell contains four terminals G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors). This technique allows reducing power consumption, propagation delay, and area of digital circuits. The GDI cell shown in Figure 6.8. Table 6.3 shows different logic functions implemented with it.

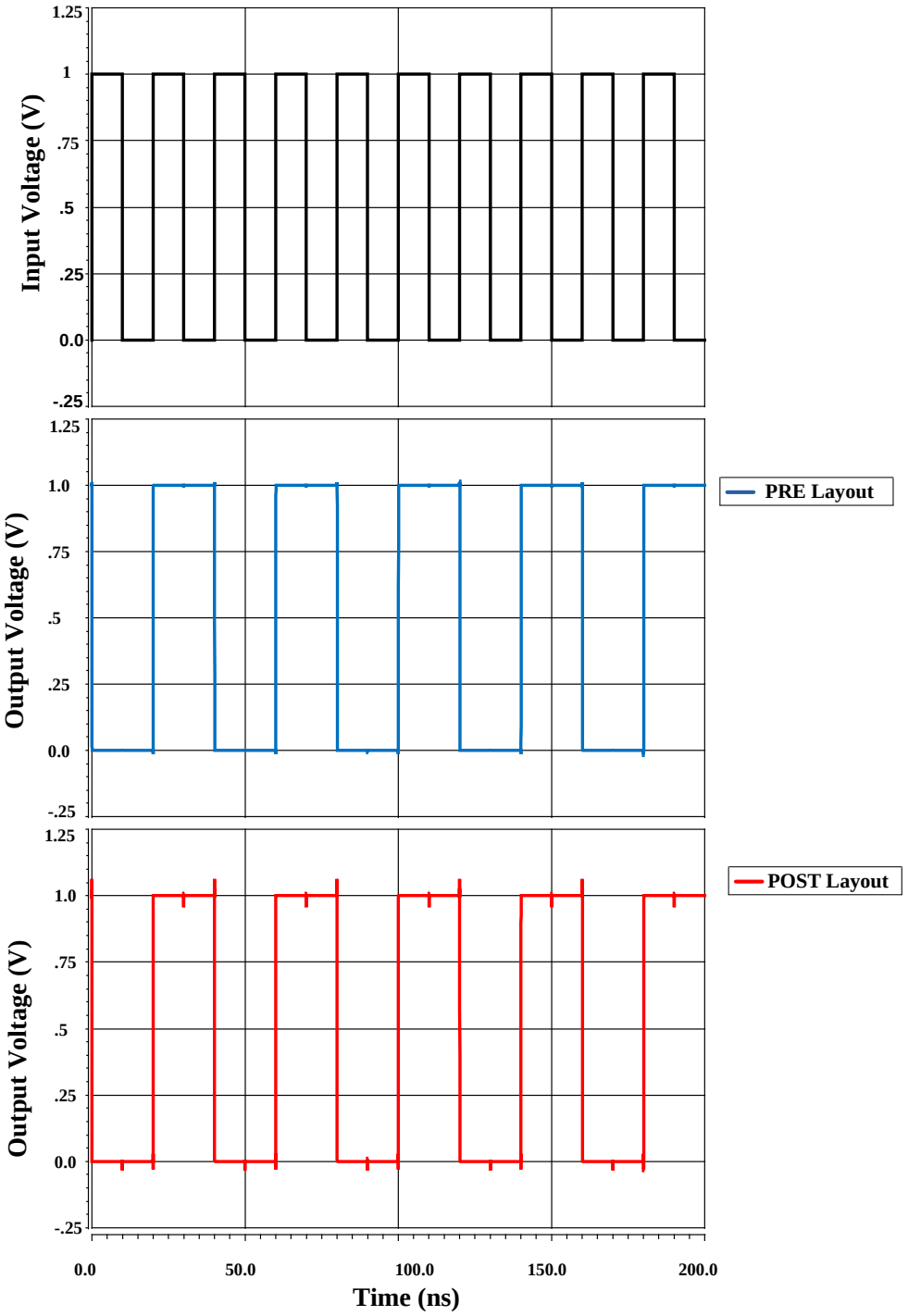

Figure 6.9: Transient response of the FD.

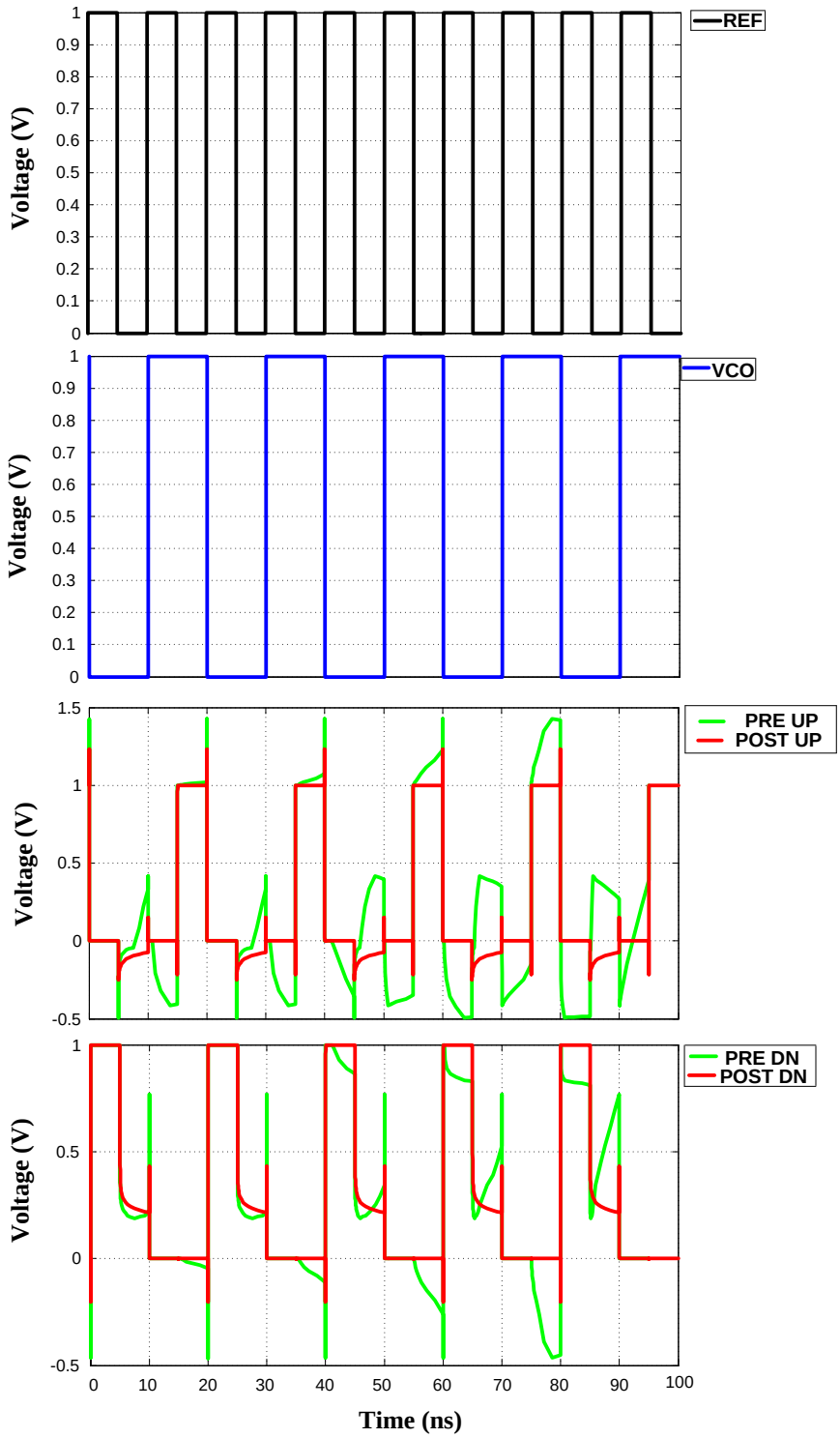

Figure 6.10: Transient response of the PFD.

6.4 Simulation Results

The implemented Frequency Divider and PFD have been simulated in 90nm CMOS process technology within virtuoso cadence environment. For testing the sustainability and robustness of these circuits, temperature sweeping and Process-corner analysis have also been conducted.

6.4.1 Transient response of frequency divider

Transient response of the frequency divider is shown in Figure 6.9. For the square input output is observed and it provides output signal having frequency as the half of the input signal frequency. For schematic simulation there is no noise present where in post layout simulation some noise comes due to the parasitic capacitance, inductance and resistance.

6.4.2 Transient response of PFD

Both the schematic and post layout simulation is done to observe the Transient response of the designed PFD which is illustrated in Figure 6.10. After the post layout simulation performance of the PFD improved. It shows that when VCO signal is high and the REF signal is low UP signal will feed to the charge pump. Again when the REF signal is high and the VCO signal is low DOWN signal will transmit to the charge pump. With this variation of UP and DOWN signal charge pump will produce a constant voltage that will control the output frequency of the VCO.

6.4.3 DC power consumption

DC Power consumption is one of the major performance parameters in any analog design. The total power consumed by frequency divider is $153.89nW$ where in case of PFD it is $2.39fW$. Then the dc power consumption for five different temperature

Table 6.4: DC power Consumption of FD at different temperature.

Temp(°C)	Power Consumption Pre Layout	Power Consumption Post Layout
-50	$8.94851\mu W$	$8.94465\mu W$
-25	$1.44796\mu W$	$1.44782\mu W$
0	$300.462nW$	$300.417nW$
25	$155.89nW$	$155.889nW$
50	$159.157nW$	$159.154nW$

Table 6.5: DC power consumption of FD at different corners.

PVT	Power Consumption Pre Layout	Power Consumption Post Layout
SS	$64.8085nW$	$64.8086nW$
SF	$445.104nW$	$445.078nW$
FS	$172.683nW$	$172.681nW$
FF	$365.755nW$	$365.715nW$

Table 6.6: DC power consumption of PFD at different temperature.

Temp(°C)	Power Consumption Pre Layout	Power Consumption Post Layout
-50	$1.17018 \times 10^{-22}W$	$2.9734fW$
-25	$8.29958 \times 10^{-20}W$	$8.4222 \times 10^{-20}W$
0	$18.4408aW$	$18.729aW$
25	$1.71655fW$	$1.564fW$
50	$81.6463fW$	$62.3495fW$

Table 6.7: DC power consumption of PFD at different corners.

PVT	Power Consumption Pre Layout	Power Consumption Post Layout
SS	$2.39122fW$	$1.9468fW$
SF	$2.39122fW$	$1.94877fW$
FS	$2.39122fW$	$2.3147fW$
FF	$2.39122fW$	$2.3188fW$

ranges from $-50°C$ to $50°C$ with interval of $25°C$ has been calculated through temperature sweep analysis. The simulated data are tabulated in Table 6.4, 6.5, 6.6 and 6.7 for the both the circuits. For PFD and FD, schematic simulation and layout simulation both are done to observe the actual performance. In both cases, the variation in DC power consumption is very small.

6.5 Layout of Frequency Divider and Phase Frequency Detector

Layout had been done to measure the area of the FD and PFD. It was performed in virtuoso cadence environment in Layout XL where only Metal1, Metal2 and Poly-Silicon were used for layout purpose. Next, the layout had been passed through DRC checker to ensure that the layout follows proper design rules. After that LVS checking was executed to ensure that the layout is perfectly matched with the schematic. Layout of frequency divider and the PFD are presented in Figure 6.11 and Figure 6.12 respectively. Area consumption by the FD and PFD are $101.74\mu m^2$ and $26.95\mu m^2$ respectively, which is a very low area compared to the state of the art.

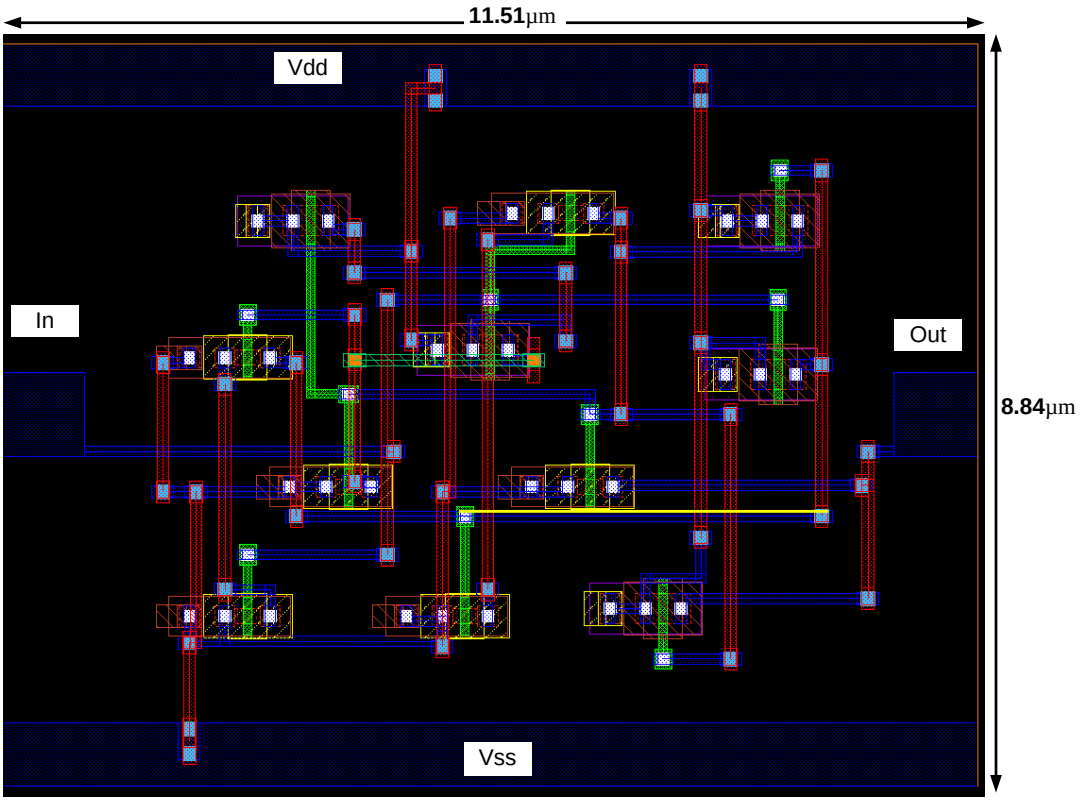

Figure 6.11: Layout of FD.

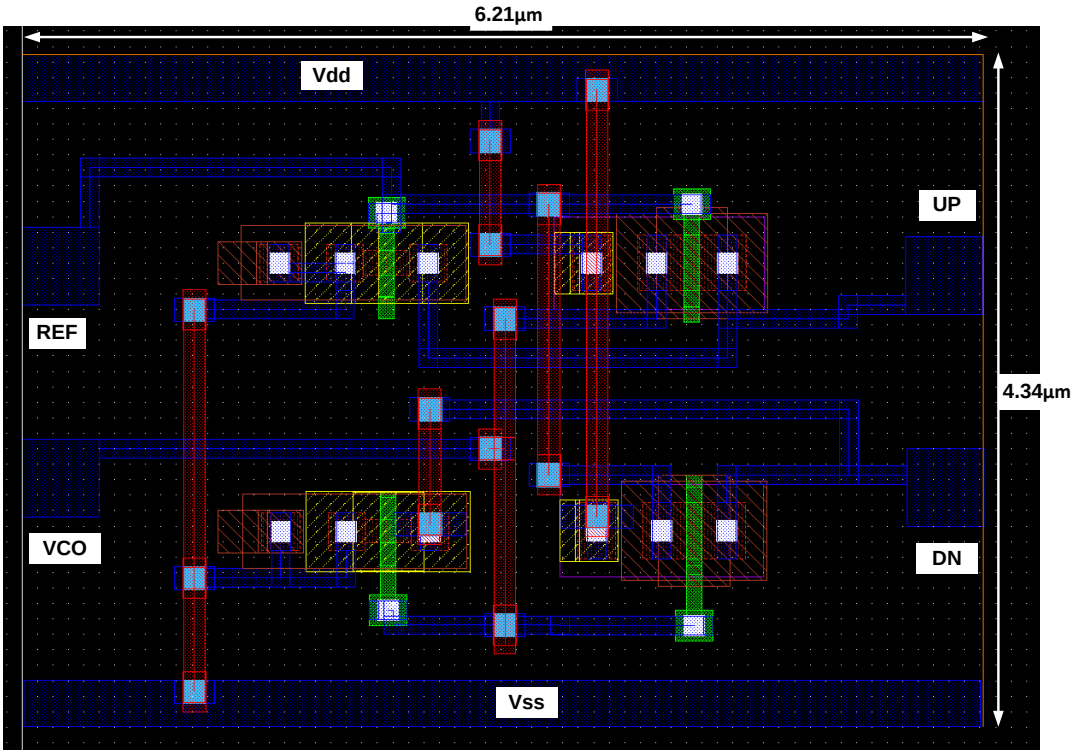

Figure 6.12: Layout of PFD.

6.6 Performance Comparison

The overall performance of the proposed FD and PFD is analyzed and compared with some other published works are shown in Table 6.8 and Table 6.9.

Table 6.8: Performance comparison of implemented FD with reported work.

References	Ref. [67]	Ref. [68]	**This work**
Technology	90 nm CMOS	28 nm CMOS	**90 nm CMOS**
Supply Voltage (V)	0.5	0.9	**1**
Power Dissipation (W)	3 m	0.18 m	**153.893 n**
No of transistors	-	-	**11**
Layout Area(μm^2)	$0.1364mm^2$	480	**101.74**

Table 6.9: Performance comparison of implemented PFD with other reported work.

References	Ref. [69]	Ref. [70]	**This work**
Technology	0.18m CMOS	180 nm CMOS	**90 nm CMOS**
Supply Voltage (V)	1.8	1.8	**1**
Power Dissipation (W)	172.670 p	27μ	**2.39122 f**
No of transistors	16	18	**4**
Layout Area (μm^2)	-	209	**26.95**

6.7 Chapter Summary

A simplified area efficient design of FD and PFD is proposed in this chapter which is implemented in gpdk 90nm CMOS process technology. Presented circuits consume less power $153.893nW$ and $2.39122fW$ respectively from 1V power supply. With that from the layout, it is observed that the simulated circuit achieved less area to implement comparing with others reported works.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1 Conclusions

The aim of this research work is to present, the developed an area efficient, low noise, low power frequency synthesizer for PLL application. In general, a performance efficient frequency synthesizer can be accomplished from the collaborative performance contribution of major individual blocks. VCO, charge pump with the low pass filter, PFD and FD are components on which the PLL's quantitative features mostly depend. In this presented research, different typologies, techniques involving the major blocks are adopted to achieve maximal throughput along with the optimum balance between the positive and negative performance parameters.

7.2 Major Contribution

The research's initial focus was the component VCO, an inevitable element of the PLL. An high throughput LC VCO having transistor capacitance based tuning capability has been proposed in chapter 3. The proposed VCO consumes a low power $(2.82 - 2.96)$ mW, whereas outputs a high FOM (-188.67 dBc/Hz), high frequency (163.25 GHz to 172.77 GHz). As transistor capacitance is exploited for tuning purpose, extra silicon area due to additional separate varactor is lessened. Finally, a comparison table has been presented to portray the outstanding performance of the proposed LC VCO with respect to other published works.

The different chapter contains brief discussion and proposal of a cascode based charge pump circuit which has been applied further development of PLL. Firstly, a broad literature review and CP's typologies have been discussed. Cadence simulation

of the proposed cascode CP shows that it consumes $34.096\mu W$ power from 1V power supply and achieves phase noise $-126.9dBc/Hz$ at 10 MHz offset. The noteworthy outcome is its extremely low area consumption $275.28\mu m^2$ due to its simple structure.

Besides, Charge Pump is fed by the block PFD which generates an error signal from input reference signal and the VCO output signal which comes through the frequency divider. In this research dissertation two GDI cells based simple PFD circuit along with its simulation result has been presented.This simple structured PFD dissipates layout area of $101.74\mu m^2$. In addition, it consumes DC power of $2.391fW$. The implemented PFD's performance parameters have also been compared with other designs. The comparison concludes that PFD precedes the referred designs with respect to layout area and power consumption.

Moreover, a Basic divide-by-2 frequency divider has also been shown which is constructed based on dynamic logic D Flip Flop. Dynamic D FF aids to work the divider circuit faster. This FD's the consumed layout area and DC power are $26.95\mu m^2$ and $153.893nW$ respectively.

Finally, the performance and substantial analysis of VCO, CP, PFD and FD suggested that VCO, CP, PFD and FD would have low area, efficient power consumption and high figure of merits, which would contribute to the development of an efficient and complete structure PLL.

7.3 Recommendations for Future Works

In this work the simulation based results had been analyzed. However, more further can be extended for analyzing and testing, which is necessary before commercial services and launching this kind of circuits. Several performance measurements should be carried out practically in order to achieve statistically significant results. Some of the further ways to improve the design are discussed bellow:

a. Passive Inductor is the main element in the LC tank of VCO which take a large area for designing VCO in IC. If this passive inductor can replaced by active inductor further, the proposed VCO will be more area efficient.

b. In this thesis, one simple charge pump is proposed and analyzed which has a small range of current mismatch. So further research can be carried out on this circuit to improve the current mismatch range of this Charge Pump.

c. With the improvement of technology transistor sizing is becoming smaller to smaller day by day. If all the transistor proposed in this research work can resize using advanced technology like gpdk 14 nm CMOS technology and simulate, the over all performance of the PLL will certainly improve.

LIST OF PUBLICATIONS

Conference Papers:

1. N. Akhter, and M.T. Amin, "An area efficient low power Phase-Frequency Detector for PLL Applications," *2nd International Conference on Advanced Information and Communication Technology (ICAICT)*, Dhaka, Bangladesh, IEEE, 2020.

2. N. Akhter, M.T. Amin, and O. Faruqe, "A High Figure of Merit Low Power LC VCO for D Band Applications," *22nd International Conference on Computer and Information Technology (ICCIT)*, Dhaka, Bangladesh, IEEE, 2019, pp. 1-6.

3. N. Akhter, M.T. Amin, and O. Faruqe, "An Area Efficient Low Phase Noise Charge Pump for PLL Applications in 90nm CMOS," *4th International Conference on Electrical Information and Communication Technology (EICT)*, Khulna, Bangladesh, IEEE, 2019, pp. 1-6.

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